Recommendation T/CD 01-12 E (Cannes 1983)

CONCERNING THE SPECIFICATION OF ENGINEERING REQUIREMENTS FOR THREE TYPES OF PLUG-IN DCE'S OPERATING WITH A USER DATA SIGNALLING RATE OF 2,400 BIT/S

Recommendation proposed by Working Group T/GT 10 "Data Communications" (CD)

Text of the Recommendation adopted by the "Telecommunications" Commission:

"The Conference of European Post and Telecommunications Administrations,

Considering

— that the CEPT Recommendation T/CD 01-01 contains the text of the specification of the general engineering requirements for Data Circuit-Terminating Equipment for use on voice-band, base-band and group-band circuits;

— that GT/CD has studied the harmonization of DCE's under the auspices of Question CD7.

Recommends

that the attached specification of engineering requirements for three types of built-in versions of DCE's as contained in the Annex to this Recommendation should apply when such equipment is being considered by CEPT Administrations for a particular application."

This Recommendation is to be seen as the first step of harmonizing the built-in DCE. This Recommendation includes a number of national requirements, as several networks have already been in operation and changes could not be made to these without considerable penalties in delays and costs.

A harmonization project that will take into account future development of components, software, etc., is to be formed as the second step of this work.

Note 1: It should be noted that this Recommendation may be revised from time to time.

Note 2: The Annex is an integral part of the Recommendation.

PART III (Type III) Pages 1 to 24

Section A. Common requirements

Section B. Network dependent requirements

Section C. Optional requirements

1. SCOPE

This document specifies 3 versions of a DCE, which is a physical unit intended to be accommodated within a DTE by plug-in means. Where a higher degree of integration is envisaged, offering the same functionality (e.g. total integration of DTE and DCE), those requirements that are not relevant to that degree of integration need not be taken into account (e.g. interfaces, construction).

The specification consists of 3 parts, each of them describing one of the versions of the DCE for different usage:

Type I: Plug-in version of a DCE for user classes 4 and 8 (according to CCITT Recommendation X.1) for envelope-structured direct access (8+2 or 6+2) to a switched data network (see Part I).

Type II: Plug-in version of a DCE for user classes 4 and 8 for non-envelope-structured direct access to a switched data network (see Part II).

Type III: Plug-in version of a DCE at 2,400 bit/s for GSTN or access to a data network via GSTN (see Part III).

Annex 1 summarizes the modulation schemes for all 3 types.

All these plug-in DCE's are potentially relevant to terminal equipment in the data field or in Teletex terminals.

The functions of these plug-in DCE's are the same as those offered by separate DCE's. The network equipment must be able to operate without changes with both plug-in and separate DCE's.

Each part of this Recommendation contains 3 sections:

— Section A: Common requirements.

— Section B: Network dependent requirements.

— Section C: Optional requirements.

Section B describes different solutions which have to be taken into account when developing a DCE or DTE for a certain national network. Section C contains possible optional requirements.

In Parts II and III reference will be made to Part I (and in Part II to Part III) in all cases, whenever possible, in order to avoid repetitions.

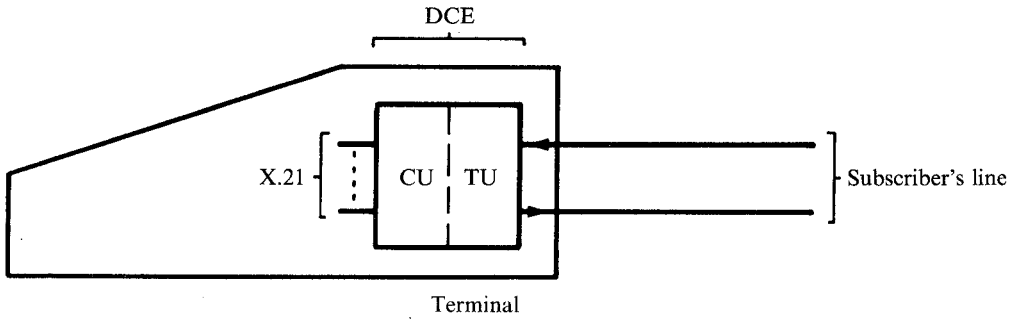
It is intended that each type of plug-in DCE should be capable of occupying the same space within the Terminal Equipment as the other types. In other words, it is intended that all the 3 types should be physically interchangeable.

PART I (TYPE I)

Section A

1. GENERAL

This type I-DCE consists of two functional units, the transmission unit TU (which can be a voice-band modem or a base-band modem) and the conversion unit CU (see Figure 1).



TU Transmission unit.
CU Conversion unit.

Figure 1.

The interface between the CU and the terminal fulfils the logical requirements of the CCITT Recommendation X.21.

2. FUNCTIONAL REQUIREMENTS FOR THE TRANSMISSION UNIT (TU)

Depending on e.g. the length of the subscriber's line, a voice-band modem or a base-band modem can be used as a TU.

2.1. Transmission unit modem (TUM)

The principal characteristics of the TUM are based on CCITT Recommendations V.26 and V.27 (referred to as Alternative A2 in Annex 1).

An example of a block diagram of the TUM is given in Annex 2.

2.1.1. *Data signalling rates*

The data signalling rate for the user shall be 2,400 bit/s ±0.01%.

Depending on the used envelope structure the addition of the framing (or envelope alignment) bits and the status bits results in a

- 33% (8-bit envelope) or
- 25% (10-bit envelope)

increase in data signalling rate, so that the following rates will be used at the digital interface (see 2.1.2.) and in the subscriber's line:

- 3.2 kbit/s (8-bit envelope structure) or
- 3 kbit/s (10-bit envelope structure).

2.1.2. *Digital interface*

Note: The description of the digital interface given in this section is primarily included as a means for describing the functions of the TU. Additionally certain Administrations will have a requirement for a physically identifiable point of demarcation between CU and TU. Such a requirement may stem from the need to gain access for testing purposes, or to allow different types of TU to be associated with the CU. In this case for the electrical characteristics reference is made to Section B, item 8. For the mechanical characteristics an example is given in Section B, item 9.

(a) Interchange circuits

In cases where a physical interface exists between TUM and CU the following Table 1 gives a list of mandatory interchange circuits (see also Annex 2).

Interchange circuit designation	Interchange circuit name	Access point designation CU		TUM
G	Signal ground or common return	G		G
DT	Transmitted data	Do	→	Di
DR	Receiver data	Di	←	Do
RS1	Received signal element timing	RS1i	←	RS1o
RS2	8× or 6× clock of RS1	RS2i	←	RS2o
A	Received line signal detector	Ai	←	Ao

Table 1.

In addition, other circuits may be used for the operation between the TUM and CU. Those circuits have to be specified on a national basis. Examples of such circuits are contained in Section C, item 2.

(b) Definitions of the interchange circuits

Circuit G-Signal ground or common return
This conductor establishes the signal common return for unbalanced interchange circuits.

Circuit DT – Transmitted data
The data signals to be transmitted via a data channel to the remote data station, or to be passed to the TU for maintenance test purposes under control of the CU or DTE, are transferred on this circuit to the TU.

Circuit DR – Received data
The data signals generated by the TU, in response to data channel line signals received from the remote data station, or in response to the CU or DTE maintenance test signals, are transferred on this circuit to the CU.

Circuit RS1 – Receiver signal element timing
Signals on this circuit provide the CU with signal element timing information. The condition of this circuit shall be ON and OFF for nominally equal periods of time, and a transition from the On to OFF condition shall nominally indicate the centre of each signal element on circuit DR.

Circuit RS2 – 8× or 6× clock of RS1
The number of transitions from ON to OFF on this circuit should be 8× higher than on circuit RS for a 10-bit envelope structure and 6× higher for an 8-bit envelope structure. Each transition from ON to OFF of RS1 corresponds also with an ON to OFF transition of RS2.

Circuit A – Received line signal detector
Signals on this circuit indicate whether the received data channel line signal is within appropriate limits. The ON condition indicates that the received signal is within appropriate limits. The OFF condition indicates that the received signal is not within appropriate limits.

(c) Electrical characteristics and significant levels (see Section B, item 8).

2.1.3. *Modulation and coding*

The TUM uses a 4-phase differential modulation scheme with main characteristics according to CCITT Recommendation V.26.

(a) Carrier frequency according to V.26.

(b) Modulation rate:
1,500 bauds (if the 10-bit envelope structure is used)
1,600 bauds (if the 8-bit envelope structure is used).

(c) The data stream to be transmitted is divided into pairs of consecutive bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element according to V.26.

2.1.4. *Scrambling*

A self-synchronizing scrambler/descrambler is used having the generating polynomial:

$$1+x^{-6}+x^{-7}.$$

The coefficients of the quotient of this division, arranged in descending order, represent the bit sequence to be coded and transmitted.

At the discretion of the Administration the scrambler may or may not have a guard circuitry, in which the transmitted bit sequence will be controlled over a range of 23 bits for the occurrence of a bit sequence of the form.

$$p(x) = \sum_{i=o}^{16} a_i x^i$$

where

$a_i = 1$ or 0, and
$a_i = a_{i+7}$.

If such a bit sequence has been detected, the next following bit must be inverted before being transmitted.

Annex 3 shows the basic circuit diagram of the scrambler.

The descrambler at the receive side is equivalent to the scrambler at the transmit side.

2.1.5. *Timing*

The TUM has an internal clock source which under normal conditions is synchronized by the received data signal.

The free running accuracy of the internal clock shall be at least ±0.01%.

The signal which is given to the interchange circuit RS1 (receiver signal element timing) is a square wave signal with a frequency of 3,000 Hz or 3,200 Hz.

A deviation from the nominal value shall not exceed $\frac{T}{100} \cdot 4$ where T is the length of one cycle of RS1.

The phase relationship between transmitted and received data (DT, DR) and the signal element timing RS1 is given in Figure 2 (including tolerances) and Annex 4.

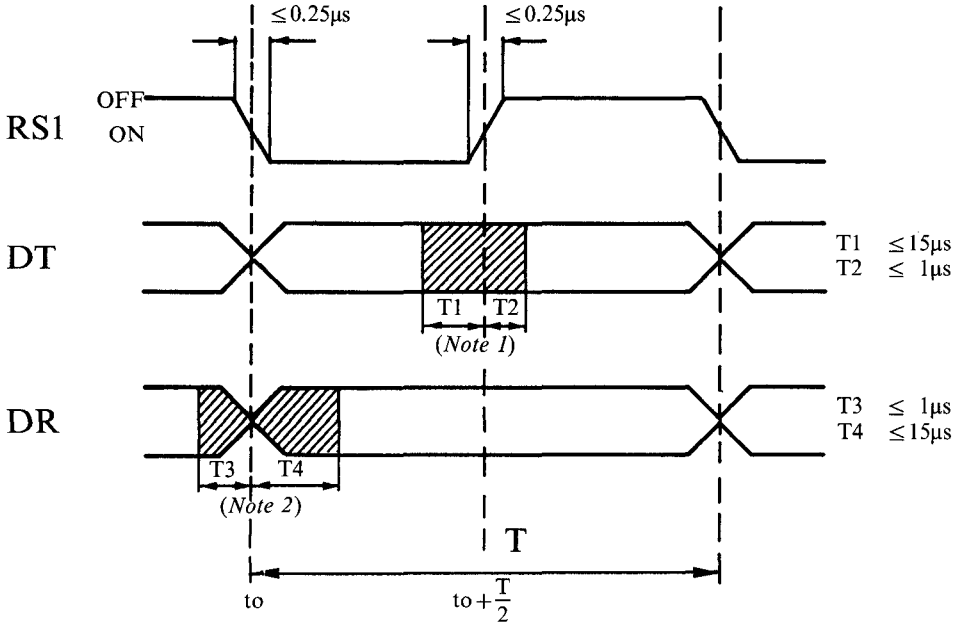


Figure 2.

Note 1: The state on the interchange circuit DT has to be valid within the range of T1+T2 referring to the centre of the positive timing edge.

Note 2: A change of the state on the interchange circuit DR is only allowed within the range of T3+T4 referring to the centre of the negative timing edge.

Note 3: The phase relationship as specified here is not necessarily applicable in cases where the physical interface is not identifiable.

RS2 (8× or 6× clock of RS1) is also a square wave signal with a duty cycle of 50% which corresponds to RS1 in the following way:

The transition from OFF to ON of RS2 shall occur in the range of ±5 µs around the transition of RS1.

Note 4: If maintenance loop 3a is activated, the internal transmit clock of the DCE must be switched to "master operation".

2.1.6. *Line interface*

The requirements of Recommendation T/CD 01-01 shall apply.

2.1.6.1. Transmit side

(a) Transmit signal level
The requirements of Recommendation T/CD 01-01 shall apply.

(b) Phase distortion limits
The transmitted line signal spectrum should have linear phase characteristics (to be obtained by means of filters or equalizers or digital means). The deviation of this linear phase characteristic should not exceed the limits specified in Figure 3.

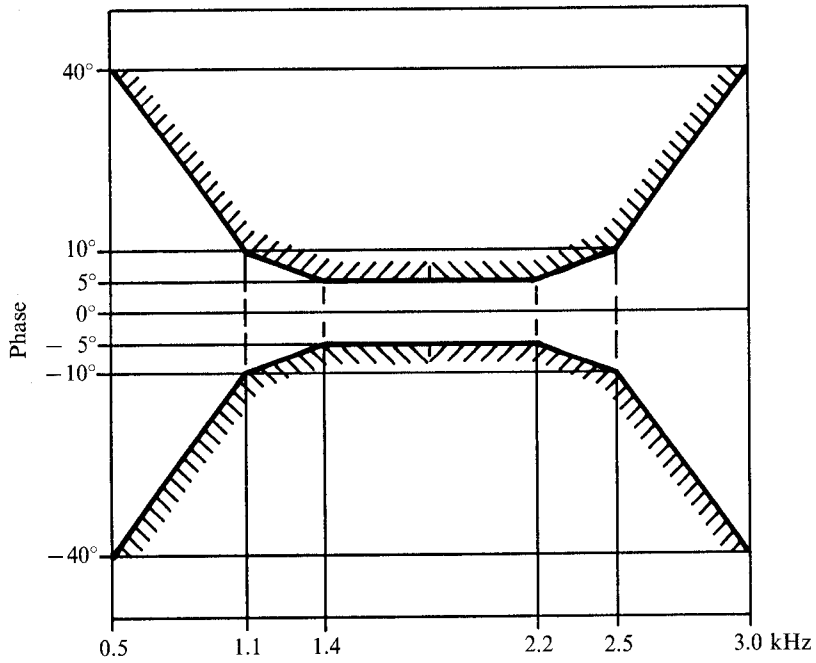


Figure 3. Tolerance limit for phase distortion of the signal transmitted to the line.

(c) Amplitude distortion limits
Power distribution of the signal spectrum originating when the 511-bit pseudo-random data sequences according to V.52 are applied to the circuit "Data input" (DI), shall be within the limits specified in Figure 4, and shall be of a raised cosine type with a roll-off factor of 50-60% equality divided between transmitter and receiver.

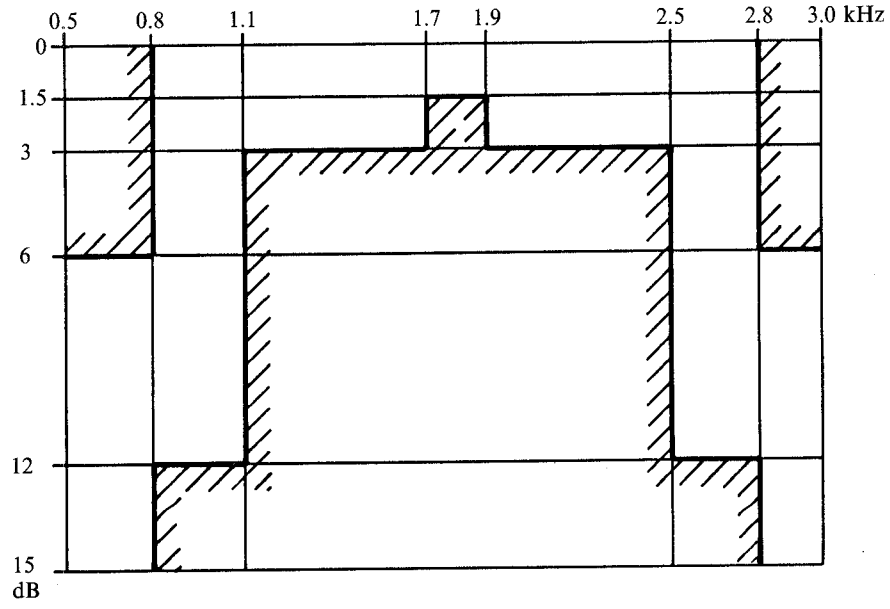


Figure 4. Tolerance limit for power distribution of the signal spectrum transmitted to the line.

2.1.6.2. Receive side

(a) Received signal frequency tolerance
Noting that the carrier frequency tolerance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the TUMs, then the receiver must be able to accept errors or at least ± 7 Hz in the received frequencies.

(b) Threshold of received line signal detector
Levels of received line signal:
greater than −26 dBm circuit A "ON"
less than −31 dBm circuit A "OFF".

The condition of circuit A (received line signal detector) for levels between the above levels is not specified except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF-to-ON transition occurs is at least 2 dB greater than that for the ON-to-OFF transition.

(c) Response times of circuit A (received line signal detector)
A fall in level of the incoming line signal to −31 dBm or lower for more than 10 ± 5 ms will cause circuit A to be turned OFF.

An increase in level to −26 dBm or higher will, within 10 ± 5 ms, turn this circuit ON.

(d) Clamping to binary condition 1 of circuit DR (data output, received data)
Circuit DR is held in a marking condition (binary 1), when circuit A is in the OFF condition.

When this condition does not exist, the clamp is removed and circuit DR can respond to the input signals of the TUM.

2.1.7. *Protection against higher voltages*

The requirements of Recommendation T/CD 01-01 shall apply.

2.1.8. *Performance requirements*

The requirements of Recommendation T/CD 01-01 shall apply.

2.2. **Transmission unit base-band (TUB)**

2.2.1. *Data signalling rate*

Same requirements as for the TUM apply.

2.2.2. *Digital interface*

Same requirements as for the TUM apply.

2.2.3. *Timing*

Same requirements as for the TUM apply.

2.2.4. *Protection against higher voltages* [1]

The requirements of Recommendation T/CD 01-01 shall apply.

2.2.5. Additional requirements are given in Section B, item 2.

3. FUNCTIONAL REQUIREMENTS FOR THE CONVERSION UNIT (CU)

3.1. General

The CU shall contain functions for formatting the terminal data to the network and in some cases (see Section B, item 7) character alignment. The CU shall also contain circuits for line supervision as well as for operation and maintenance (see Section B, item 3). All control signalling to and from the network will normally take place between the terminal itself and the network in accordance with CCITT Recommendation X.21.

This means that all signalling, except during testing and alarm states, takes place between the terminal and network without the participation of the plug-in DCE.

An example of a block diagram is given in Annex 5.

3.2. Interface between the CU and the terminal

3.2.1. *General*

The interface towards the terminal shall for the CU conform to the CCITT Recommendation X.21 for the functional requirement, X.24 for the definitions and item 3.2.3. for the electrical characteristics of the interchange circuits.

3.2.2. *Interchange circuits*

The interchange circuits to be provided at the interface are (see Table 2):

Interchange circuit designation	Interchange circuit name	Direction from CU	Direction to CU
G	Signal ground or common return (*Note 1*)		
T	Transmit		X
R	Receive	X	
C	Control		X
I	Indication	X	
S	Signal element timing	X	

Note 1: This interchange circuit is identical with power supply common return.

Table 2.

3.2.3. *Electrical characteristics and significant levels*

The electrical characteristics shall be as follows (see Figure 5):

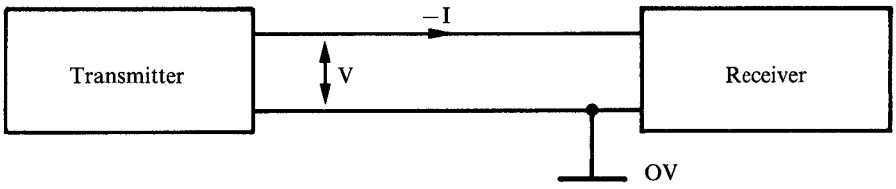


Figure 5.

TRANSMITTER:

"binary 1" or "OFF" $\geq$4.0 V with load current −40 μA
"binary 0" or "ON" $\leq$0.4 V with load current 0.4 mA

RECEIVER:

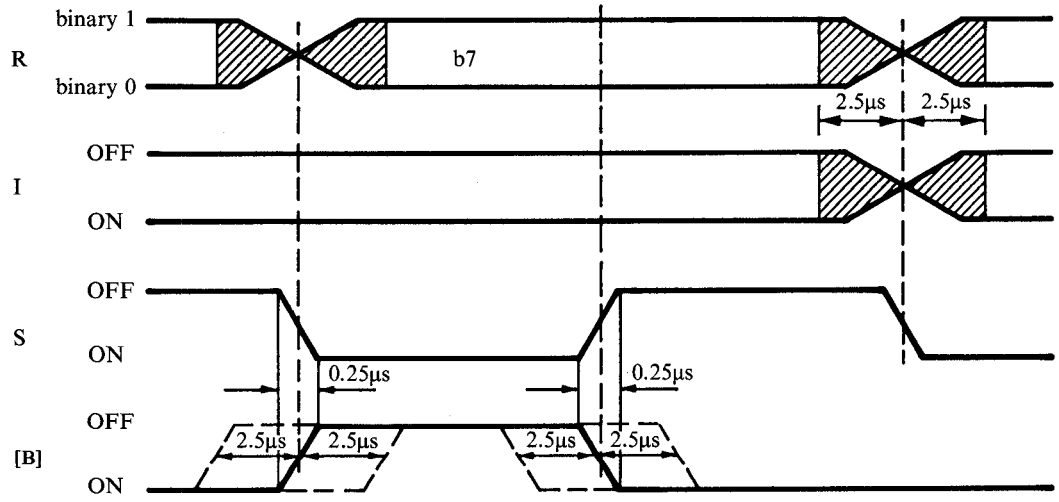
Thresholds
"binary 1" or "OFF" $\geq +3.6$ V
"binary 0" or "ON" $\leq +0.7$ V

Load
"binary 1" or "OFF" −40 μA at 4 V
"binary 0" or "ON" 0.4 mA at 0.4 V

Permissible input voltage range: $-0.5 \ldots +5.5$ V.

3.2.4. *Relationship between the interchange circuits*

The phase relationship between the interchange circuits is given in Figure 6 (including the max. tolerances) and in Annex 4.



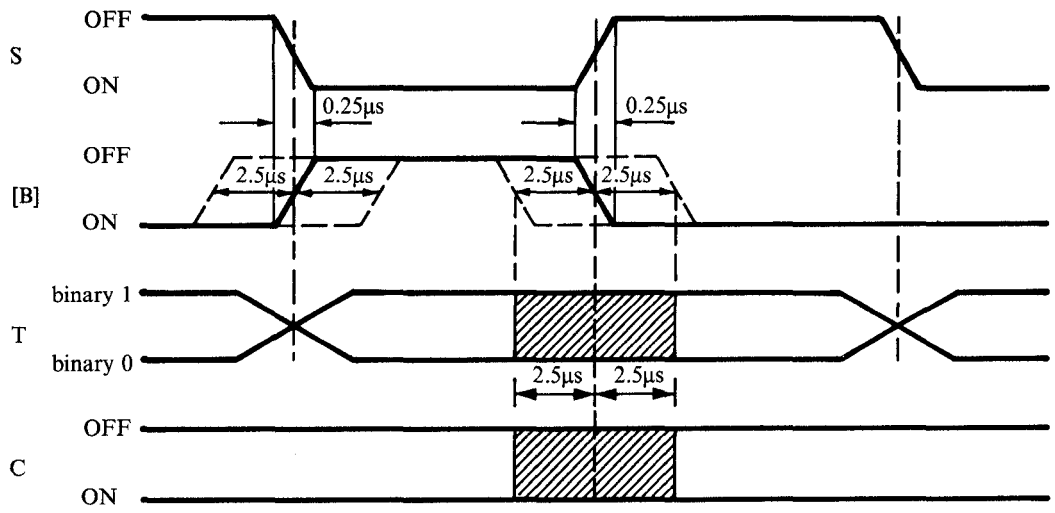


Figure 6.

3.3. **Envelope function**

In the CU the data to be exchanged across the interchange circuits T and R are grouped/regrouped in envelopes. As for the forming of the envelope see CEPT Recommendation T/CD 02-01 (based on CCITT Recommendation X.50 = 6+2) and CEPT Recommendation T/CD 02-02 (based on CCITT Recommendation X.51 = 8+2).

3.3.1. *Status bit*

The condition on the circuits C and I are conveyed by means of the status bit of the envelope with the following relation:

Status bit 0 = OFF condition on circuits C and I
1 = ON condition on circuits C and I.

Transmit side	C = OFF	S = 0
	C = ON	S = 1
Receive side	S = 0	I = OFF
	S = 1	I = ON

3.3.2. *Envelope alignment strategy*

In the envelope alignment strategy four states and three criteria for transfer from one state to another can be recognized.

For state diagram see Figure 7.

(a) Criteria

Alignment Error (AE):
2, 3 or 4 contiguous envelope alignment bits with the same digital value.

In alignment (IA):
Absence of Alignement Errors in envelope alignment bits for the period of minimal 7 envelopes.

New Alignment (NA):
The identification of one unique bit position carrying the alignment pattern.

(b) States

(I) System in synchronization
DCE or the tributary channel is in alignment with network.

(II) Verification of synchronization
The alignment bits are supervised according to the IA criterium. Criterium IA transfers the system to State I. If the criterium IA is not found the system transfers to State III. State II may include the Time-Out for the elimination of the influence of short line breaks.

(III) Search
New Alignment criterium is searched in the received bit stream.

Note 1: Verification of synchronization and search of new alignment may be simultaneous processes. In this case the system returns to State II if NA is not found.

(IV) Reframing
Reframing of the system takes place if the NA criterium is fulfilled. A transfer to State II takes place.

(c) Alarms
The alarm "Loss of envelope alignment" (as used in the part "Fault conditions and consecutive actions" occurs, if T seconds after the criterium AE the criterium IA will not be received.

(d) Performance
1. The frame-alignment recovery time, after a slip and in absence of bit errors should be less than 50 envelopes, with 95% probability.
2. A random error rate of 1 in 10^4 shall not cause any frame-alignment recovery action.

State diagram

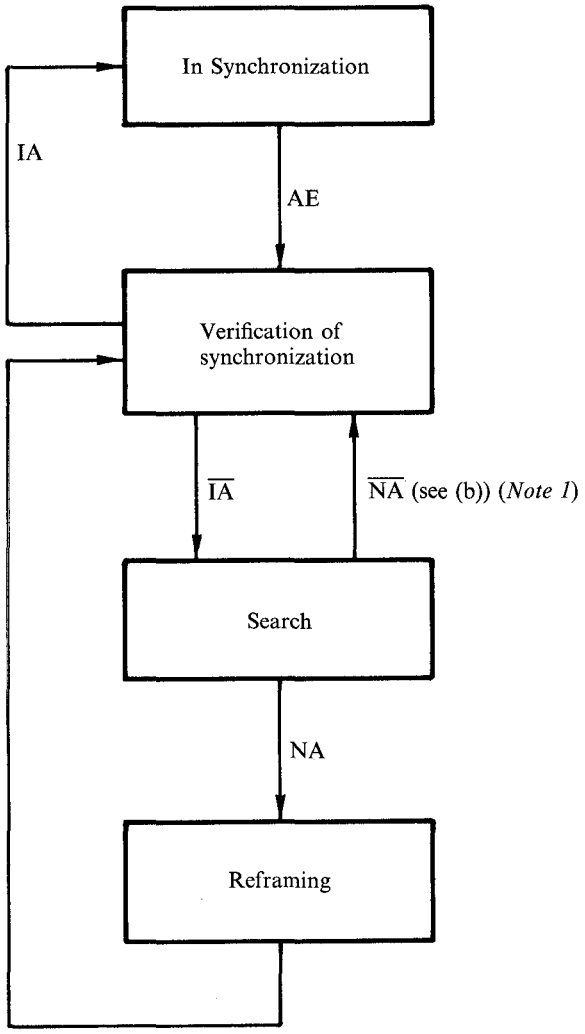


Figure 7.

3.4. Alarms and consecutive actions

Four groups of possible failures are considered:
— Failures occurring in the terminal (fault condition a)
— Failures on the subscriber's line (fault condition b)
— Failures in another equipment of the network which has an impact on the DCE (fault conditions c, d)
— Failures within the DCE itself (fault condition e).

In Annex 6 a state diagram, definitions of signals and abbreviations are given which are mentioned in the following text.

3.4.1. *Fault condition a:* Failure of the power supply or the main power of the terminal

Option 1: No action will be taken towards the network (Annex 6, state NPS).

Option 2: Power failure of the DCE will be indicated to the network by a special signal, see Section B, item 6 (Annex 6, state NPS).

3.4.2. *Fault condition b:* Loss of carrier

At loss of carrier, the TU detects this situation after a time of 10 ± 5 ms and clamps the circuit DR to binary "1" (see 2.1.6.2. (c), (d)).

Depending on the interchange circuit A = OFF (received line signal detector) immediately a "Hold signal 1" (H1) will be sent to the terminal (Annex 6, state A1).

The terminal can transmit within the range of 2-3 s (action delay time). Afterwards two options are possible (Annex 6, state A2):

Option 3: AIS will be sent to the network.

Option 4: The CU will prevent the TU from transmitting an outgoing carrier.

3.4.3. *Fault conditions c and d:* Loss of envelope alignment

Condition c: If the network loses envelope alignment, an AIS signal will be received by the DCE. The CU detects this situation after a time T = 1 s (Annex 6, state LEA1).

Condition d: The detection of LEA can also occur, if the incoming data are strongly disturbed (Annex 6, state LEA1).

The consecutive actions towards the terminal in both cases are: 2-3 s action delay time.

"Hold signal 1" will be sent to the terminal.

The terminal can transmit during this range of 2-3 s.

If envelope alignment is not re-established during the action delay time, DNR will be sent to the terminal and AIS to the network (Annex 6, LEA2).

When envelope alignment in the DCE is re-established, through-connection of the DCE takes place (Annex 6, state DT).

3.4.4. *Fault condition e:* DCE faults

If any hardware failure occurs and can be detected, AIS shall be sent, if possible, and DNR shall be sent towards the terminal, if possible (Annex 6, state LEA2).

4. TEST LOOPS

The definitions of the loops are set out in CCITT Recommendation X.150.

4.1. Local test loop – loop 3

In order to assist the test of the DTE, test loop 3 is provided in the DCE. The precise implementation is network dependent and indicated in Section B, item 3.1.

4.2. Network test loop – loop 2a/2b

For maintenance purpose, a loop 2a/2b is implemented in the DCE. This loop is activated within the test call procedure, see Section B, item 3.2. (alternatives A to D).

If the loop towards the network is activated, the DCE will signal "DCE not ready" towards the terminal.

4.3. **Additional loops may be provided**, see Section B, item 3.1.

5. POWER CONSUMPTION

The power required by the plug-in DCE will be supplied by the terminal (see Annex 2 and Annex 5).

The following voltages and the relevant max. values of current are available:

+12 V ±5% max. 150 mA
−12 V ±5% max. 150 mA
+ 5 V ±5% max. 1,100 mA

The max. noise voltage to be excepted on these suplies is:
10 mV RMS and 30 mV peak-to-peak for the + & −12 V supplies
10 mV RMS and 100 mV peak-to-peak for the +5 V supply

The total power consumption of the DCE shall not exceed 8 watts.

Note: Power consumption in excess of 5 watts may require special precautions in the terminal equipment.

6. CONSTRUCTION

For the time being, mechanical arrangements are only specified for typewriter-type terminals.

Taking into account the rapid developments in the field of DCE's, it is not, at the present time, convenient to specify the construction part for other applications. This will be a point for further study when these applications are defined.

Where the DCE is accommodated on a single card, for typewriter-type terminals this card must be accommodated within the dimensions specified in item 6.1.1. and the connector to the DTE must be in accordance with item 6.1.3.

Future study at the second step of harmonization will concentrate in a single solution taking into account the various requirements of the Administrations and future technologies.

6.1. Construction of typewriter-type terminals

6.1.1. *Dimensions of the plug-in DCE*

The dimensions of the plug-in DCE to be used in typewriter-type terminals must be no larger than the following:

Alternative A	–	depth	195 mm
	–	width	74 mm
	–	height	120 mm
Alternative B	–	depth	195 mm
	–	width	90 mm
	–	height	120 mm

It is up to each Administration to decide which of the two alternatives applies.

6.1.2. *Cabinet*

Where a number of separate modules comprise the DCE (e.g. when the two functional blocks, CU and TU, are realized separately) the preferred method of housing the modules is the use of a cabinet as specified in Figure 8. More details of this are given in Annex 7.

6.1.3. *Connector (DTE to DCE)*

The equipment is electrically connected (digital interface, power supplies) to the terminal by means of a connector in accordance with Figures 9 and 10. The mechanical characteristics of this connector shall be as defined in standard VG 95324, part 3, connector for printed circuit, blade and socket connectors, 32 pin, grid 2.54 mm (for further details see Annex 8).

Figure 9 shows the general connector arrangements with two options for connecting the DCE to the DTE:

(a) a female connector mounted in a fixed position in the DTE (where a cabinet is used to house the DCE, Figure 8 shows the positioning of the connector at the DCE),

(b) a female connector on a flexible cable. Figure 10 shows the allocation of the connector rows and the pin numbering scheme.

The pin assignment for the interface connector is given in Annex 9.

6.1.4. *Connector (CU to TU)*

This connector is not specified, however an example is given in Section B, item 9.

6.1.5. *Connector (DCE to transmission line)*

The transmission line cord shall be fixed within the DCE or connected by a connector at the front of the DCE (see e.g. Figure 9).

7. ENVIRONMENTAL REQUIREMENTS

The full performance of the plug-in DCE shall be maintained when operating in an environment of ambient temperature and relative humidity as described in Annex 10.

Climatogram for operation. Annex 10, Figure a
Climatogram for transport. Annex 10, Figure b
Climatogram for warehousing. Annex 10, Figure c

Annex 10, Figures b and c are identical with the requirements of the Recommendation T/TR 02-03 concerning equipments for telecommunication centres.

Note 1: It could be necessary to protect the plug-in DCE against electrical and magnetical disturbances caused by the terminal.

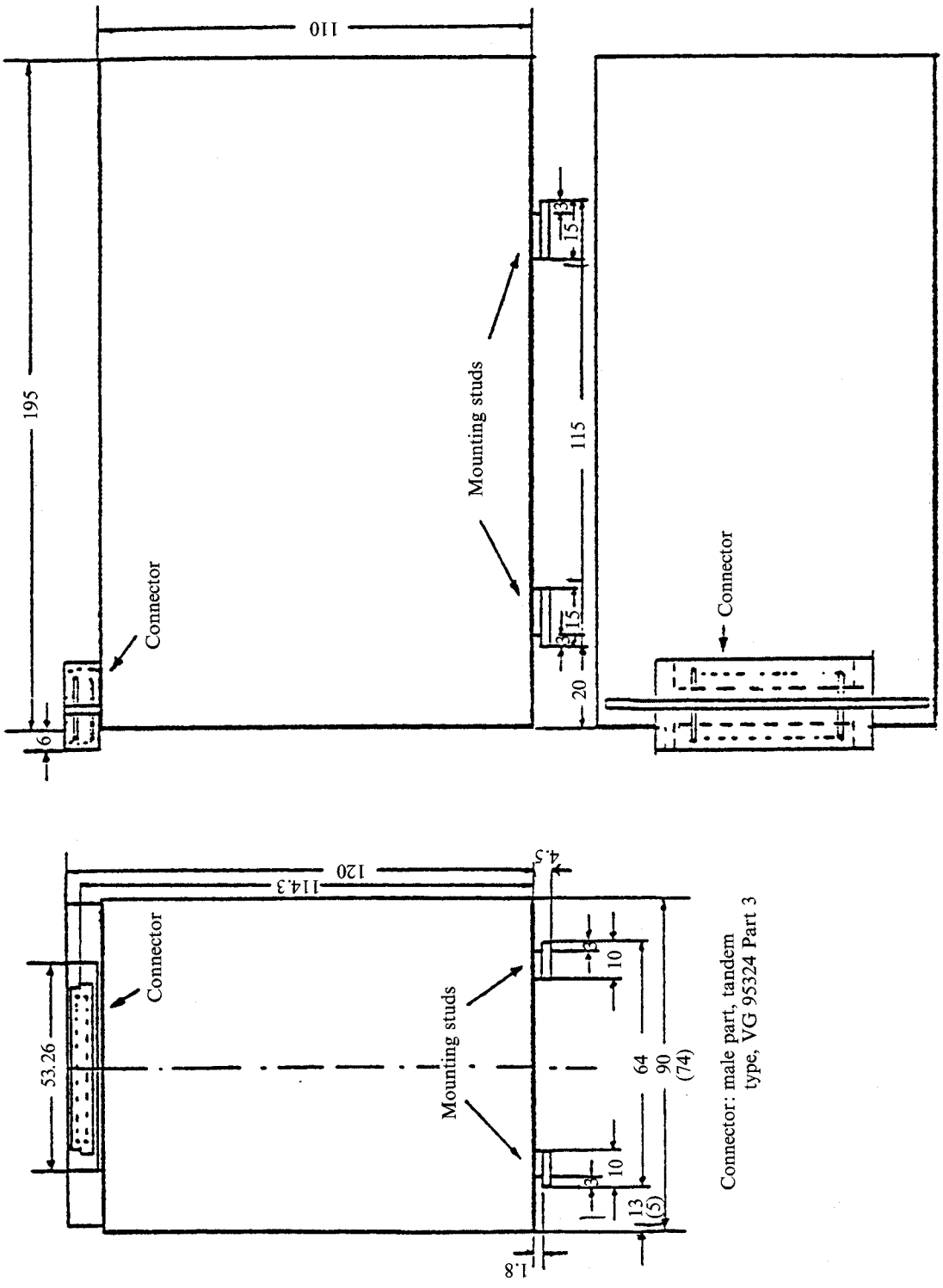


Figure 8. Overall dimensions of the cabinet used for housing the built-in DCE, and positioning of the connector.

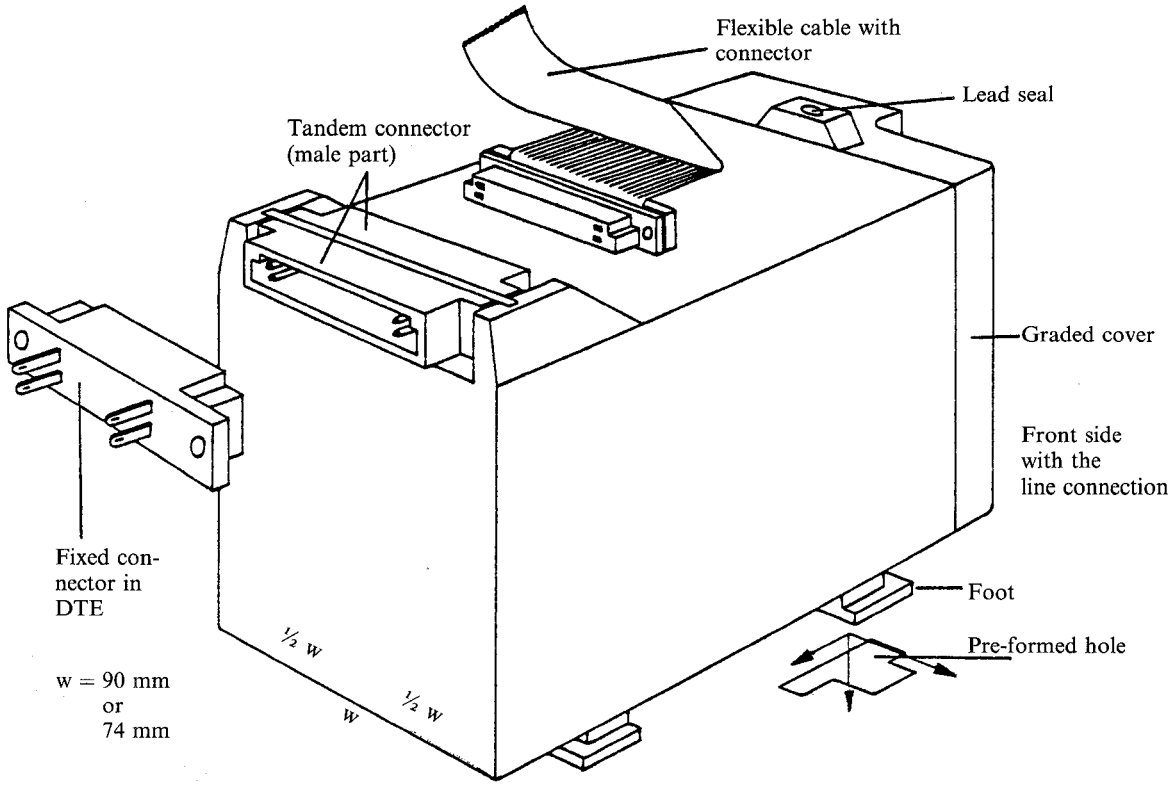


Figure 9. Connector arrangement.

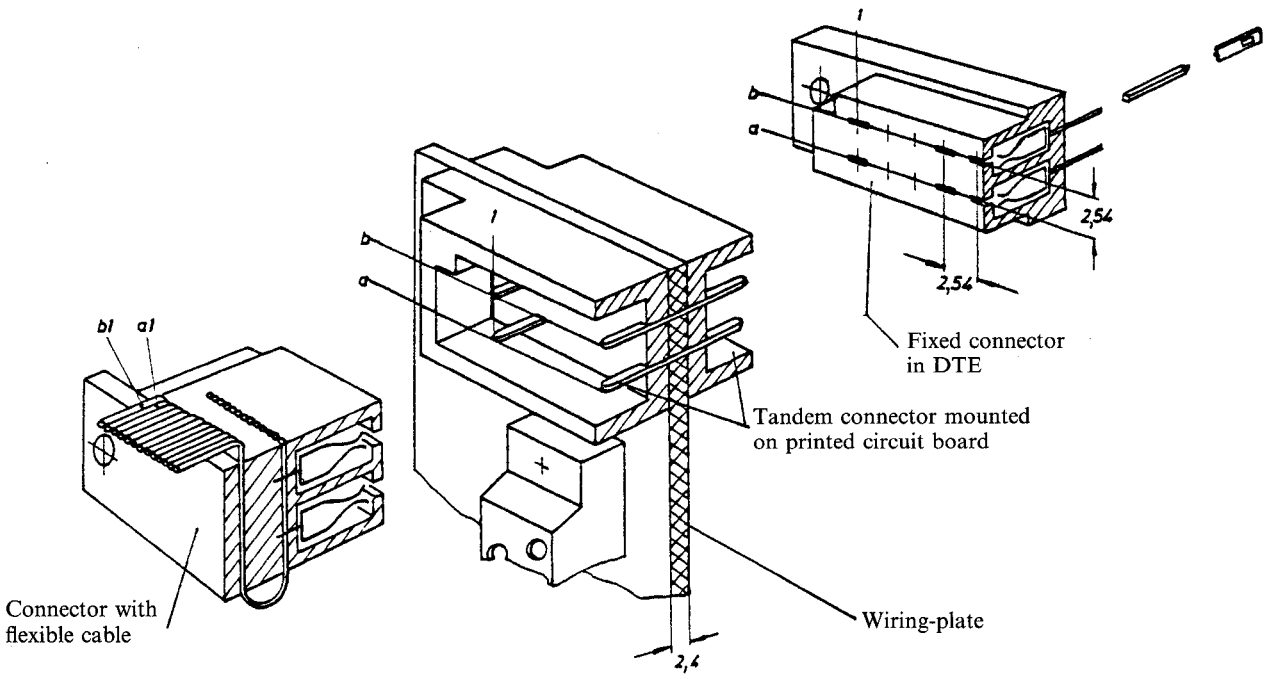


Figure 10. Allocation of connector rows and counting scheme.

Section B

1. GENERAL

This section specifies national network dependent requirements which may be included in a plug-in DCE at the discretion of the Administration concerned.

2. TRANSMISSION UNIT BASE BAND (TUB)

In addition to the following network dependent requirements, the common requirements of Section A, item 2.2. shall apply.

2.1. Alternative C1 (British Telecom)

2.1.1. *Modulation and coding*

(a) All timing signals for the modulator shall be derived from the receive line signal.

(b) The modulation system shall be a modified form of diphase transmission known as Wal_2 carrier transmission. This consists of phase reversals of a rectangular carrier signal whose fundamental frequency in Hz is nominally equal to the line bit rate in bit/s. The carrier will be such taht its transitions occur at $t = t_o + \frac{T}{4}$ and $t = t_o + \frac{3T}{4}$, where T = one line data element period and the period of one carrier cycle, and $t = t_o$ is the time of the start of a transmitted data element. The two basic elements of the unfiltered Wal_2 signal are shown in Figure 11.

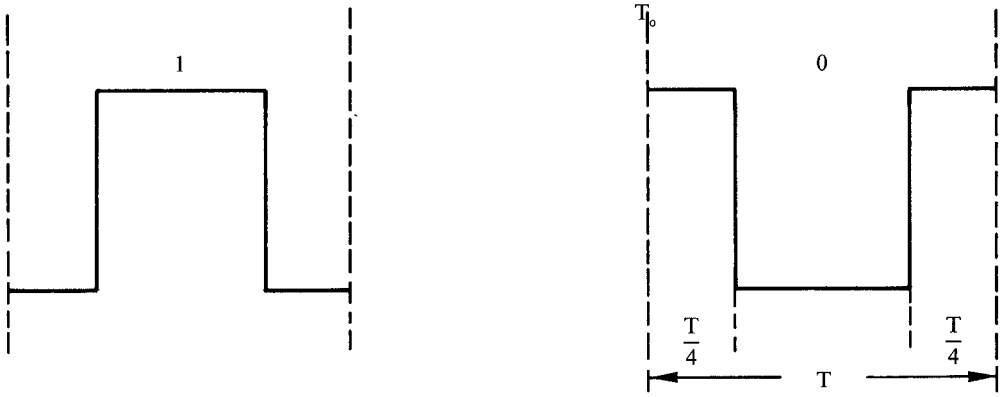


Figure 11. Wal_2 basic elements.

(c) The TUB shall be designed to demodulate satisfactorily a line signal generated as described in item 2.1.1.b above, and will be recovered via an unamplified line having an insertion loss of up to 45 dB at a frequency equal to that of the carrier signal.

The line will be standard local line plant and no adjustment facilities shall be required to accommodate line characteristics.

2.1.2. *Scrambling*

The data received on the data input interconnecting circuit shall be scrambled and differentially encoded before being modulated and transmitted to line. Similarly the demodulated data shall be differentially decoded and descrambled before being presented on the data output interconnecting circuit.

The scrambling and descrambling process shall be as described in CCITT Recommendation V.35 Appendix 1, i.e. the generating polynomial is:

$$1 + x^{-3} + x^{-20}$$

The differential encoding and decoding shall be a scrambling and descrambling process with generating polynomial:

$$1 + x^{-1}$$

2.1.3. *Line interface*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The TUB shall be capable of carrying a wetting current of magnitude in the range 5 to 8 mA.

(c) Failure of the DTE power supply shall cause a change in direction of flow of the wetting current in the second pair of the 4-wire circuit (see Figure 12).

(d) The use of a line wetting current shall not degrade the performance of the TUB.

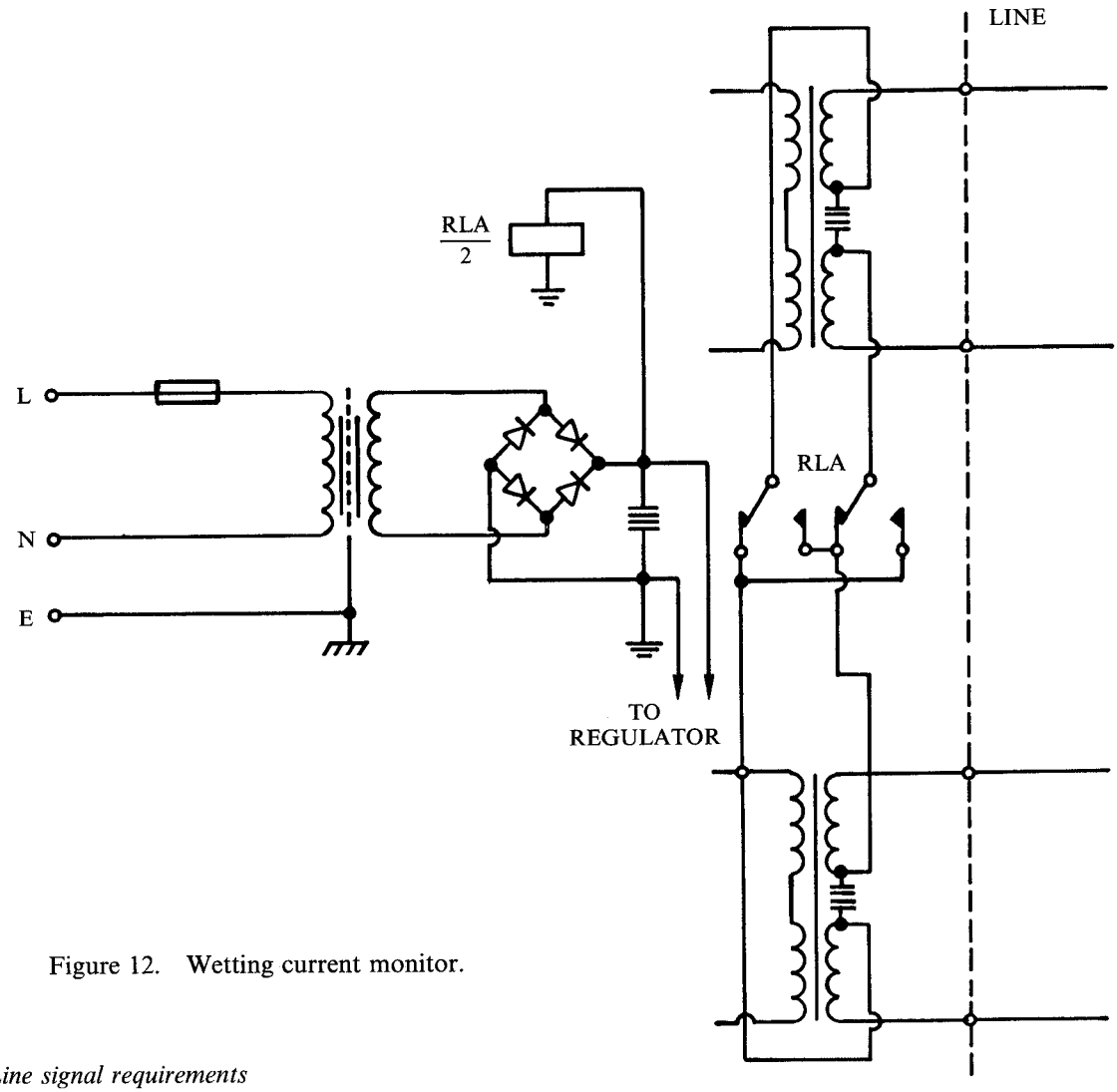


Figure 12. Wetting current monitor.

2.1.4. *Line signal requirements*

(a) The requirements of Recommendation T/CD 01-01 shall apply.

(b) If the level of the signal at the receive line terminals is below −48 dBm, then the TUB shall take the following action:
— Clamp data on the data output interconnecting circuit to a constant binary 1.
— Present a binary 0 condition on the Received Line Signal Detector interconnecting circuit.

The TUB shall not resume normal operation until the level of the signal at the receive line terminals is above −45 dBm.

2.1.5. *Equalization*

The shape of the Wal_2 modulated line spectrum is such that it can be considered as having pre-equalization, thus a requirement for an equalizer in the receiver is not envisaged.

2.2. **Alternative C2 (Austrian PTT)**

2.2.1. *Coding*

The coding process produces a raised cosine pseudo ternary line signal
(Ist order, base band—alternative mark inversion)
See Figure 13.

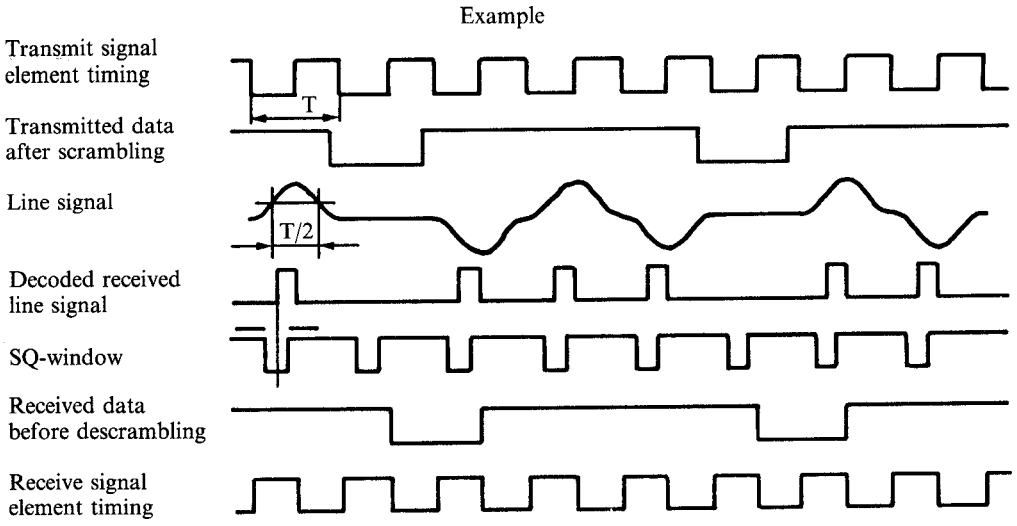


Figure 13.

2.2.2. *Timing*

All timing signals for the modulator shall be derived from the received line signal.

2.2.3. *Scrambling*

The same scrambler is used as in Section A, item 2.1.4. However, the guard circuitry shown in Annex 3 is mandatory.

2.2.4. *Line interface*

(a) The requirements of Recommendation T/CD 01-01 shall apply.

(b) The TUB shall be capable of carrying a wetting current of 3 mA maximum.

(c) The use of the wetting current shall not degrade the performance of the TUB.

2.2.5. *Line signal requirements*

(a) The requirements of Recommendation T/CD 01-01 shall apply.

(b) Threshold of received line signal detector.
Levels of received line signal:
greater than −40 dBm circuit A "ON"
less than −41 dBm circuit A "OFF".

(c) Response time of circuit A
A fall in level of the incoming line signal to −41 dBm or lower for more than 10 ± 5 ms will cause circuit A to be turned OFF.
An increase in level to −40 dBm or higher will, within 10 ± 5 ms, turn this circuit ON.

(d) Clamping to binary 1 condition of circuit DR (data output, received data)
Circuit DR is held in a marking condition (binary 1), when circuit A is in the OFF condition.
When this condition does not exist, the clamp is removed and circuit DR can respond to the input signals of the TUB.

2.2.6. *Equalization*

(a) In most applications, no manual adjustment of the equalizer shall be required.

(b) For exceptional cases, a manual fine adjustment of the equalization shall be possible to achieve optimum signal quality, particularly with longer subscriber lines. The manual adjustment would also be needed if, for any reason, a higher transmit level were used (3 dB is suggested in cases of severe electrical noise).

2.3. **Alternative C3 (Deutsche Bundespost)**

2.3.1. *Coding*

The coding process produces a raised cosine half-bauded pseudo-ternary line signal (alternate mark inversion code AMI). The wave shaping is depicted below (Figure 14).

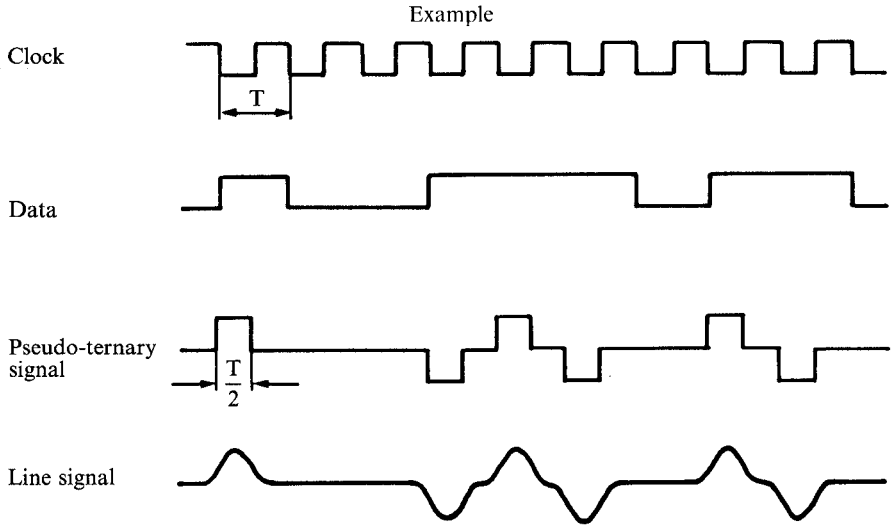


Figure 14.

2.3.2. *Timing*

All timing signals for the modulator shall be derived from the received line signal except for the case of a test loop 3a being activated, in which case the TUB has to maintain all necessary timing signals towards the CU with a frequency tolerance of ±0.01% from nominal value.

2.3.3. *Scrambling*

The same scrambler is used as described in Section A, 2.1.5. The guard circuitry shown in Annex 3 is mandatory.

2.3.4. *Line interface*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The nominal impedance shall be jumper-selectable: either 150 ohms or 1,000 ohms.

2.3.5. *Line signal requirements*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The peak-to-peak line signal voltage shall be 1.4 Vp-p with tolerances of +10%/−20% measured with an 150 ohms non-inductive load resistance.

(c) If the voltage of the received signal is below 7 mVp-p, than the TUB shall take the following actions:
— Clamp data on interchange access point Do to a constant binary 1.
— Present an OFF condition on interchange access point Ao.

The TUB shall not resume normal operation until the voltage of the received signal is above 14 mVp-p.

2.3.6. *Equalization*

The TUB shall be equipped with an automatic adaptive equalizer which shall cater for both the equalization of the attenuation distortion of unloaded cables and the attenuation and phase distortion of loaded cables. The phase equalizer may be switched in manually.

2.4. Alternative C4 (NPDN)

2.4.1. *Modulation and coding*

(a) All timing signals for the modulator shall be derived from the received line signal.

(b) The modulation system is based on differential biphase modulation (biphase-space) of a square wave carrier with fundamental frequency in Hz nominally equal to the data signalling rate in bit/s.

The line signal shall consist of a two-level signal with the following transitions:
"1" transition at $t = t_o$
"0" transition at $t = t_o + \frac{T}{2}$ and $t = t_o$,
where T signifies the period of one data element, and t_o is the time at which a data element begins (see Figure 15).

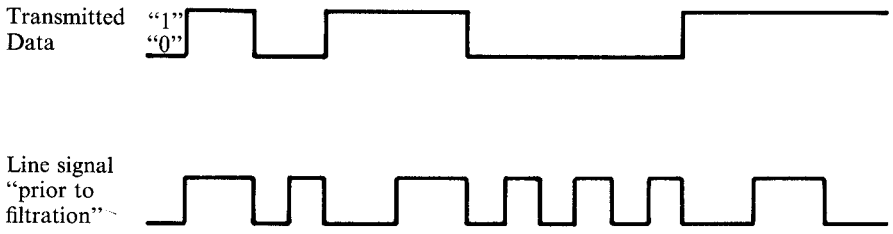


Figure 15.

(c) The following maintenance functions shall be included. If the received line signal detector is in the OFF condition, transmission in the opposite direction shall cease either after a time delay of 2.5 seconds or alternatively controlled by the CU via the use of interchange circuit LEA.

(d) The TUB shall be designed to demodulate satisfactorily a line signal generated as described in item 2.4.1.c) above and transmitted via an unamplified line having an insertion loss of 40 dB at a frequency equal to that of the carrier signal.

The received line signal detector shall have a hysteresis of a least 2 dB.

2.4.2. *Scrambling*

Data scrambling is not employed.

2.4.3. *Line interface*

(a) In addition to the following requirements the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The TUB shall be capable of carrying a wetting current of magnitude in the range 5-15 mA.

(c) The use of a line wetting current shall not degrade the performance of the TUB.

(d) When a timer within the TUB is used to control the "transmit inhibit" function specified in item 2.4.1.c) above this function shall be implemented in such a way that the MTBF for all the circuitry of concern for this function is at least one magnitude greater than the MTBF for the whole TUB.

(e) The TUB shall be provided with a "power-off" generator with the characteristics described in Section B, item 6. The generator shall be powered from the wetting current in the receiver line.

2.4.4. *Line signal requirements*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The transmit level shall be 0 dBm or −6 dBm (strappable) when measured with pseudo-random (511-bit pattern) data against a resistive impedance of 600 ohms.
Tolerance at nominal level: ± 1 dB.

(c) If the received line signal detector is in the OFF condition, then the TUB shall clamp data in the data output interconnecting circuit to a constant binary 1.

2.4.5. *Equalization*

The TUB should be preferably equipped with an adaptive equalizer in the receiver.

2.4.6. *Performance*

(a) The receiver clock in the TUB shall maintain its phase and frequency for at least 500 ms in order to avoid resynchronization in case of short breaks on the line. This also implies that the TUB shall not produce a bit slip when the line signal returns after a short break on the line.

(b) Amplitude hits on the line of up to 10 V and with a duration of up to 15-bit lengths shall not cause any bit slip in the TUB.

2.5. **Alternative C5 (Italian PTT)**

2.5.1. *Modulation and coding*

(a) All timing signals for the modulator shall be derived from the received line signal.

(b) The modulation system is based on differential diphase modulation of a square wave carrier with fundamental frequency in Hz nominally equal to the data rate in bit/s.

The following relation is forecast:
Digit 0 – No phase inversion
Digit 1 – Inversion of the phase.

(c) The TUB shall be designed to demodulate satisfactorily a line signal generated as described above, and will be recovered via an unloaded line having an insertion loss of up to 40 dB at the frequency equal to the data rate.

2.5.2. *Scrambling*

Data scrambling is not employed.

2.5.3. *Line interface*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The TUB shall be capable of carrying a wetting current of 3 mA maximum, without decreasing the performance of the TUB.

2.5.4. *Line signal requirements*

(a) The requirements of Recommendation T/CD 01-01 shall apply.

(b) If the level of the signal at the receive line terminals is 6-12 dB below the minimum level, the TUB shall take the following action:
— Clamp data on the data output interconnecting circuits to a constant binary 1.
— Present a binary 0 condition on the received Line-Signal-Detector interconnecting circuit.

The TUB shall not resume normal operation until the level of the signal at the receive line terminals is 6 dB above the minimum level.

The minimum level is the level received at the output of an artificial line (Figures 16 and 17) having an attenuation loss of 40 dB at the frequency equal to the data rate, the transmitted signal shall be +6 dBm with a pseudo-random sequence of 511-bits.

2.5.5. *Equalization*

A simple amplitude equalizer is used without manual adjustment.

2.6. **Alternative D1 (Deutsche Bundespost)**

Alternative D1 is a 2-wire duplex TUB using the echo cancellation technique.

2.6.1. *Coding*

The same coding is used as for alternative C3 (item 2.3.1.).

2.6.2. *Timing*

The same requirements as for alternative C3 apply (item 2.3.2.).

2.6.3. *Scrambling*

The scrambling and descrambling process shall be as described in CCITT Recommendation V.35, Appendix 1, i.e. the generating polynomial is:

$$1+x^{-3}+x^{-20}$$

2.6.4. *Line interface*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The nominal impedance of the line interface shall be 150 ohms.

2.6.5. *Line signal requirements*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The peak-to-peak line signal voltage shall be 1.0 Vp-p with a tolerance of ± 15%, measured with an 150 ohms non-inductive load resistance.

(c) If the voltage of the received signal is below 40 mVp-p, then the TUB shall take the following action:
— Clamp-data on interchange access point Do to constant binary 1.
— Present on OFF condition on interchange access point A0.

The TUB shall not resume normal operation until the voltage of the received signal is above 60 mVp-p.

2.6.6. *Equalization*

The TUB shall be equipped with an automatic adaptive equalizer capable of equalizing the attenuation distortion of unloaded cables.

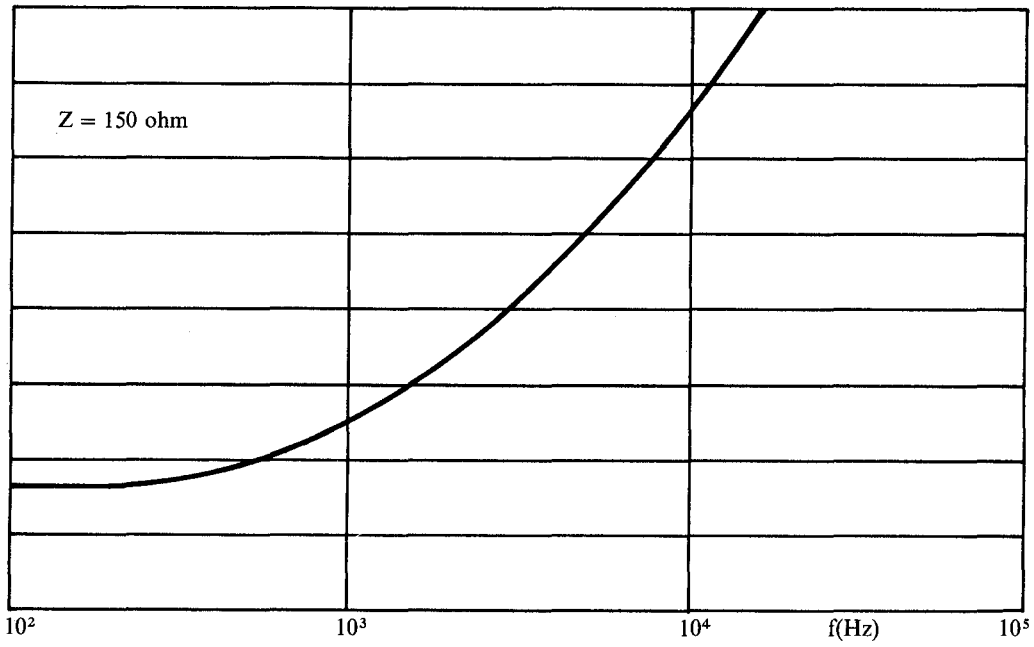
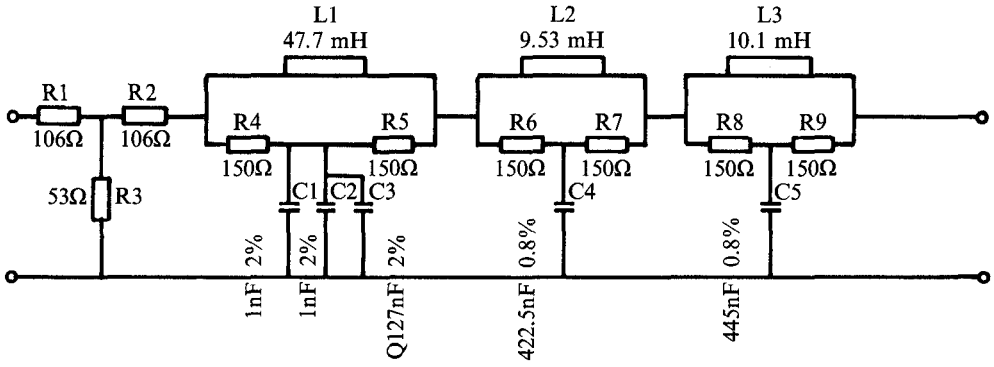


Figure 16. Artificial network.



Tolerance of resistance $\leq 0.5\%$

Figure 17. Electric scheme.

2.7. Alternative D2 (Norway)

2.7.1. *Modulation and coding*

(a) The 2-wire duplex TUB uses the echo cancellation method.

(b) All timing signals for the modulation shall be derived from the line signal.

(c) The modulation system is based on differential biphase modulation (biphase-space) of a square wave carrier.

The line signal shall consist of a two-level signal with the following transitions:
"1" transition at $t = t_o$
"0" transition at $t = t_o + \frac{T}{2}$ and $t = t_o$,
where T signifies the period of one data element and t_o is the time at which the data element begins (see Figure 18).

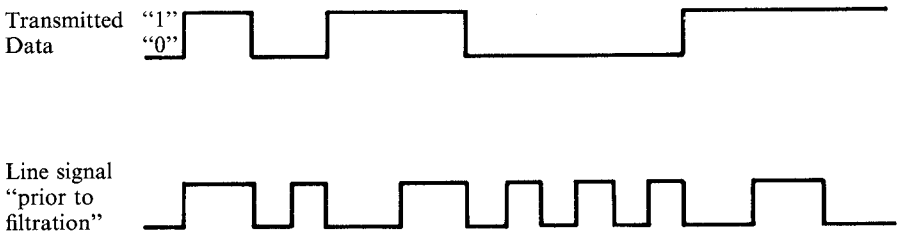


Figure 18.

(d) The signalling rate on the line is fixed at 12 kbit/s.
To convert the original 3,000 bit/s envelope structured bit stream into the 12,000 bit/s bit stream, each bit of the original bit stream is transmitted 4 times.

(e) The following maintenance functions shall be included. If the received line signal detector is in the OFF condition, transmission in the opposite direction shall cease either after a time delay of 2.5 seconds or be alternatively controlled by the CU via the use of interchange circuit LEA (loss of envelope alignment).

(f) The TUB shall be designed to demodulate satisfactorily a line signal generated as in item 2.7.1.c) above and transmitted via an unamplified line having an insertion loss of 40 dB at a frequency equal to that of the carrier signal.
The received line signal detector shall have a hysteresis of at least 2 dB.

2.7.2. *Scrambling*

The TUB will require scrambling of the line signals using scrambler polynoms of different lengths for the two transmission directions.

Scrambler in the transmitter is characterizer by:

Polynom: $1+x^{-6}+x^{-7}$

Scrambler in the receiver is characterized by:

Polynom: $1+x^{-3}+x^{-5}$

2.7.3. *Line interface*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The TUB shall be capable of carrying a wetting current of magnitude in the range 5-15 mA.

(c) The use of line wetting current shall not degrade the performance of the TUB.

(d) When a timer within the TUB is used to control the "transmit inhibit" function specified in item 2.7.1.e) above this function shall be implemented in such a way that the MTBF for all the circuitry of concern for this function is at least one magnitude greater than the MTBF for the whole TUB.

(e) The TUB shall be provided with a "power-off" generator with the characteristics described in Section B, item 6. The generator shall be powered from the wetting current in the line.

2.7.4. *Line Signal Requirements*

(a) In addition to the following requirements, the general requirements of Recommendation T/CD 01-01 shall apply.

(b) The transmit level shall be 0 dBm or −6 dBm (strappable) when measured with pseudo-random (511-bit pattern) data against the nominal impedance. The tolerance is ± 1 dB.

(c) The nominal impedance consists of a resistor of 120 ohms connected in cascade with a 820 ohm resistor. The 820 ohm resistor is shunted with a 110 nF capacitor.

(d) If the received line signal detector is in the OFF condition then the TUB shall clamp data on the data output interconnecting circuit to a constant binary 1.

2.7.5. *Equalization*

The TUB should be equipped with an adaptive equalizer in the receiver.

2.7.6. *Receiver clock requirement*

The receiver clock in the TUB shall maintain its phase and frequency for at least 100 ms in order to avoid resynchronization. This also implies that the TUB shall not produce a bit slip when the line signal returns after a short break on the line.

3. TESTING AND MEASURING REQUIREMENTS

3.1. **Test loops** (see Figure 19)

The definitions of the loops are set out in CCITT Recommendation X.150.

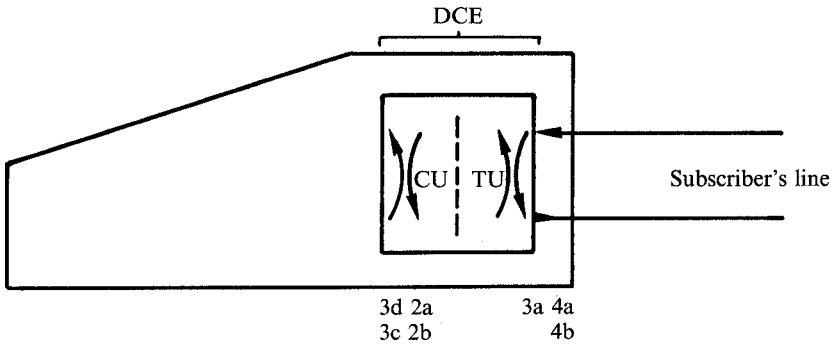


Figure 19.

Two types of additional test loops (in addition to loop 2a/2b, see Section A, item 4) shall be provided in the DCE:

(a) Test loop towards the DTE
Loop 3a: this loop is automatically activated, locally controlled (see also Section A, item 2.1.5., *Note 4*);
Loop 3c/3d: this loop is manually or automatically activated, locally controlled.

(b) Test loops towards the network
Loop 4a or 4b: this loop is manually activated, locally controlled.
If the loop is activated, the DCE will signal "DCE not ready" towards the terminal.

The following Table 3 gives the various additional test loop which are used in the different networks as identified so far:

Network	Test loops 3a	3c/3d	4b
FRG	X		
I		X	X
NPDN		X	
A		X	
UK	X[1)]	X	

[1)]Administration use only.

Table 3.

3.2. **Test-call facility**

3.2.1. *Alternative A (NPDN)*

3.2.1.1. Test call from the DCE (loops 3d and 2a) (see Annex 11).

Test initiation

The test is initiated by pressing the TEST key on the DCE, whereupon 3 envelopes of CLEAR are sent to the network. Thereafter READY (at least 3 envelopes) is sent to the network until the DCE receives READY from the network. The DCE sends this sequence of CLEAR followed by READY to guarantee that the DCE, including the subscriber's circuit, changes to READY state, i.e. that any encapsulations are cancelled.

When the DCE has detected READY from the network, it proceeds automatically to send TEST CALL T1 to the network. The network answers the test call by sending T2.

When the DCE has detected T2, loop 2a is closed to the network. The loop is placed in the interface to the terminal and includes also the interface generators and receivers towards the terminal. The loop implies that the interchange circuits Receive and Transmit as well as the circuits Control and Indication are interconnected.

Loop test

For the DCE's which are strapped for SYN-synchronization to the terminal the looped information is displaced 1 bit relative to the network. The 1-bit displacement continues until SYN-synchronization has occurred in the DCE. The SYN-synchronization circuits were activated when the DCE detected T2. The exchange can now test the SYN-synchronization circuits by sending SYN to the DCE, whereupon the bit displacement from the DCE will no longer be performed.

The loop test continues by sending 1, ON (READY FOR DATA) from the network. When the network detects 1, ON from the DCE, the network sends two envelopes of SYN′, ON (SYN′ is SYN displaced 1 bit relative to the envelope) and then changes to 0, ON.

If the network then detects these envelopes of SYN′, ON followed by 0, ON, the network will send 1, OFF to the DCE. When these are returned and detected by the network, the loop test is complete. It has then been tested that the SYN-synchronization circuits are not activated in data phase, and that status bits and data bits are transmitted without distortion.

For the DCE's which are strapped for byte timing synchronization, no displacement of the returned test call character takes place on closure of the loop.

After the network has tested the loop, the loop connection is deactivated by sending CLEAR to the DCE, whereupon the DCE sends the test call character T1 to the network.

If no fault has been detected in the loop test, the network sends from special envelopes which is interpreted by the DCE as TEST OK. When this signal from the network is detected by the DCE, this is indicated by flashing of the TEST lamp as long as the TEST key is depressed. If the test to the network fails, the TEST lamp will glow steadily as long as the TEST key is depressed. Test call character T1 is sent to the network as long as the TEST key is pressed.

The subscriber connection will be encapsulated until the TEST key is depressed and READY state exists.

When the TEST key is depressed, the DCE sends the test call character T1 to the network for another 100 ms before the actual through-connection in the DCE takes place in order to avoid generation of a false call to the network by contact bounce or the like.

3.2.1.2. Test call from the network (loop 2b)
See Annex 12

As for the test from the DCE, this test can be initiated regardless of the original state of the DCE or DTE. A test will, however, never be initiated to a subscriber who is already engaged in a call to the network.

The test is initiated by the network sending four envelopes of CLEAR (0/OFF) followed by test indication T2, whereupon the loop 2b is closed in the DCE.

On closure of the test loop, the test of the DCE follows the same procedure as when the test is initiated from the DCE.

The test from the network terminates with opening of the test loop by sending of CLEAR to the DCE. No TEST OK is sent to the DCE. The test is interrupted when a fault in the procedure or the signal is detected by the network. This results in encapsulation of the subscriber connection.

During the test Receive and Indication are set to 0 and OFF respectively.

3.2.2. *Alternative B (Austrian PTT)*

3.2.2.1. Test call from the subscriber to the network (loop 2a and 3d)

A test key in the terminal is used to initiate the test call by controlling the interchange circuit TA (test activation) to ON. (ON will be maintained as long as the TEST key is depressed.)

If the network is able to accept a call (that means that the state "DCE Ready" is given), the interchange circuit TI1 (test indication) is set to ON and the terminal shall indicate by means of a TEST lamp that a test is in progress.

If the TA is ON (and TI1 is ON), the DCE automatically dials a certain number (standardized for the whole country, e.g. 3,000) in order to get a connection with a TEST-equipment (see Figure 20).

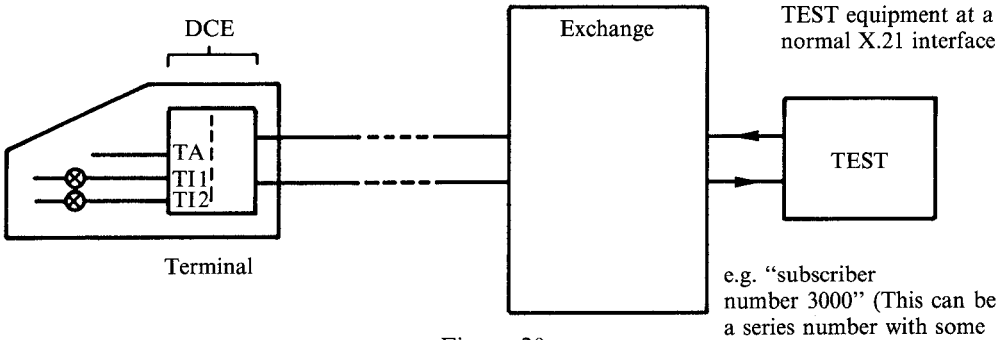


Figure 20.

After the connection is established, the DCE transmits a TEST word W (a special envelope, status bit is set to "0").

If 8 TEST words W are received by the TEST-equipment, this equipment transmits a TEST word W′ (status bit is set to 0 and TEST word W is incremented by 1) as long as the TEST key is depressed.

The CU detects the TEST words W′ and controls the interchange circuit TI2 to ON. If one of the received TEST words is wrong, the CU controls the interchange circuit TI2 to OFF and holds this state for 0.5 s, independent of the fact whether right words have been received during this time or not.

The terminal shall indicate the situation "TEST OK" by means of a second TEST lamp depending on the state of interchange circuit TI2 (see Figure 20).

While the test is in progress, DNR will be sent to the terminal.

When the TEST key is released, the test is interrupted and the DCE clears the call automatically.

3.2.2.2. Test between 2 subscribers

This test is only possible, if the "testing DTE" is able to generate a test pattern in a certain format, synchronized with the byte timing, and is able to interpret the receiving test pattern.

The test will be initiated after the connection is established to the "tested DTE".

The following test pattern will be transmitted while C = OFF:

b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
1	0	0	1	0	0	1	1

The DCE of the "tested DTE" will send back the following test pattern, if the DCE has received 8 test patterns from the "testing DTE" without failures:

b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
0	1	0	1	0	0	1	1

If transmission errors are detected, another test pattern will be sent back:

b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
1	1	0	1	0	0	1	1

If the DCE of the "tested DTE" cannot find a valid test pattern in 4 consecutively received bytes, it will go back to state 13 (Data transfer).

The test period is limited to 1 s (After this time the connection will be cleared by the "testing DCE".) During the test, loop 3 of the "tested DCE" will be activated.

3.2.2.3. Test call from the network

From a TEST-equipment in the exchange a test call can be initiated.

(a) At first by manual dialling a connection to the relevant subscriber has to be established.

Afterwards the TEST word W with status bit "0" will be sent to the subscriber, in order to be able to distinguish between TEST pattern and normal data in the data phase of a connection.

If 8 TEST words W are received by the CU, the CU checks if during this time the interchange circuit SQ (signal quality, *Note 1*) is set to ON (if a certain threshold of quality for all received bits is given).

— If this is the case, the TEST word W′ is sent back (loop 2a) to the network.

— If this is not the case, the TEST word W″ (status bit is set to "0", TEST word W is incremented by 2) is sent back (loop 2a) to the network.

— If during the test the CU detects a wrong TEST word W, a TEST word W‴ (status bit is set to "0", TEST word W is incremented by 3) is sent back (loop 2a) to the network.

The TEST-equipment interprets the incoming signals.

(b) If the connection to the relevant subscriber cannot be established by dialling, another TEST-equipment can be directly connected to the subscriber's line, and the same tests as described in item a) can be made.

While the test is in progress, from the DCE DNR will be sent to the terminal, and the interchange circuit TI1 is set to ON.

Note 1: The signal quality is regarded as unsatisfactory, if—in the case of a TUM—the phase deviation is greater than 22.5° for a period of at least 5-20 ms. The signal quality is regarded as satisfactory if the phase deviation is less than 22.5° for a period of at least 40-100 ms.

If a TUB is used, the signal quality is regarded as unsatisfactory, if the "decoded received line-signal" is more than T/4 too early or too late with respect to the nominal position. The signal quality is regarded as satisfactory, if a least 1,000 consecutive bits are within the "time window of T/2".

3.2.3. *Alternative C (Deutsche Bundespost)*

3.2.3.1. General

Besides other means of network maintenance, provision for a transparent loop 2b is made in the IDN of the DBP. This loop may be activated at any time during the data transfer phase of a data connection.

Note 1: In this respect, "data connection" is also to be understood in conjunction with a connection established to or from a network test center.

3.2.3.2. Loop activation

The DTE wishing to activate loop 2b, in the far-end DCE transmits the loop command

t = 001100..
c = OFF

By detecting the incoming loop command pattern in an 8+2-envelope

S-bit = 0
data bits = 001100..

the remote DCE closes its loop 2b thus reflecting the loop command to the initiating station. This station now has the choice of either making the loop transparent by turning ct. C from OFF to ON or letting time-out T_{2b} expire which, after 0.5 s, will automatically cause the loop 2b to open.

In the other case, c = ON (≙ S-bit = 1) will keep the loop 2b closed until it is released by incoming envelopes with S-bit = 0 (≙ c = OFF in the initiating station).

Figure 21 illustrates the loop activation procedure.

3.2.4. *Alternative D (Italian Administration)*

(a) Loop activation

The DTE wishing to activate loop 2b in the far-end DCE transmits the loop command

c = OFF
t = 111100

The DCE detecting the incoming loop pattern in a 6+2-envelope

S-bit = 0
data bits = 111100

for a minimum of 8 envelopes (when the loop is activated from the network, 32 envelopes will be transmitted) closes its loop 2b (see Figure 22).

(b) Test phase

A maximum of 7 test characters continuously can be transmitted. When the loop is activated from the network, a sequence of 2 test characters and 2 loop characters will be transmitted.

(c) Termination phase

At least a sequence of 8 characters different by loop character must be transmitted.

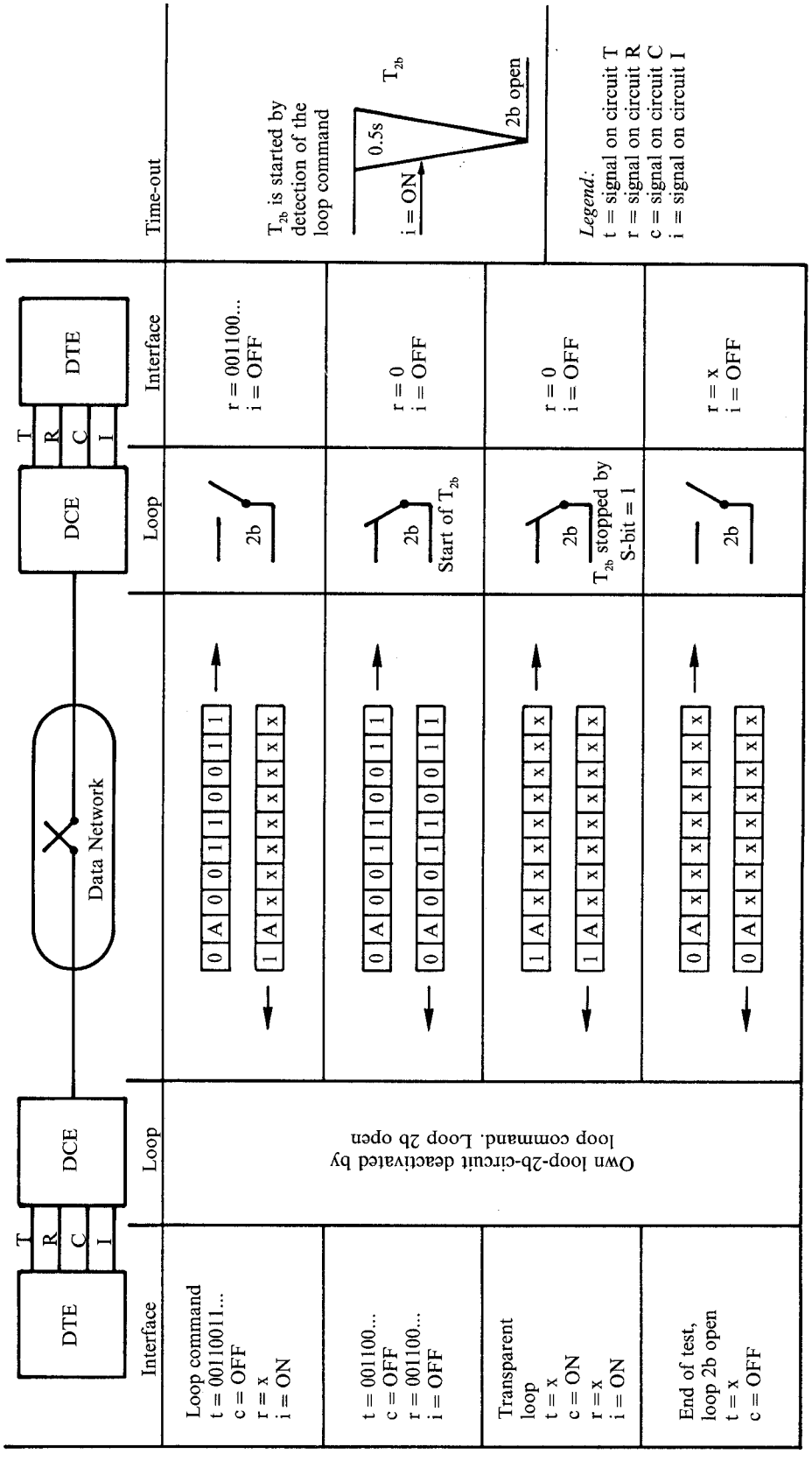


Figure 21. Remote control of loop 2b in the PDN of the Deutsche Bundespost.

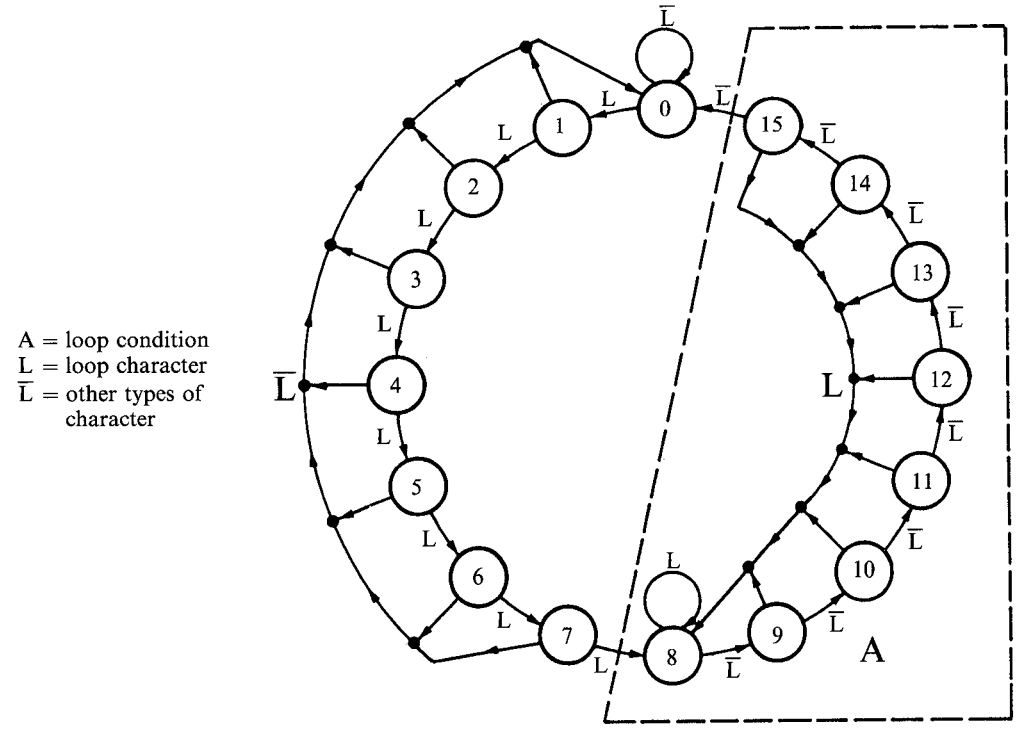


Figure 22.

4. EQUALIZER TO BE PROVIDED IN THE TUM

A compromise equalizer or manually adjustable equalizers shall be provided which are capable of equalizing the following line conditions:
1 to 3 carrier links
0 to 5 km unloaded cable
0 to 30 km loaded cable (different national loading rules apply).

If a compromise equalizer will be used, this equalizer shall always be located at the receiver side.

If manually adjustable equalizers will be used, there are 2 possibilities of location:

(a) In order to minimize unit cost on manually adjustable equalizer shall be located in each receiver. Both ends of a links must be adjusted during installation.
For the unloaded cable a compromise equalizer will be used also at the receiving side only.

(b) In order to have the possibility of equalizing both directions of transmissions at one side 2 manually justable equalizers shall be provided in each unit. Both can be involved in one link at a time.
For the unloaded cable a compromise equalizer will be used at the receiving side only.

The following Table 4 gives the various kinds of equalizing which are used in different networks:

Network	Only compromise equalizer	Manually adjustable equalizer one (a)	two (b)
A		X	
FRG	X		
I	X		
NPDN			X

Table 4.

5. LINE WETTING

From the network side a wetting current will be injected on each pair of the 4-wire line to the TU, according to the following table. Besides preventing corrosion in contacts, the wetting current can be used to supply a "Power-off" generator in the DCE-TU.

The following requirements related to the wetting current arrangement apply (see Table 5).

Network	Max. line wetting current
A	3 mA
I	3 mA
NPDN	15 mA

Table 5.

— the DC-resistance of the line transformers shall be less than 300 ohms (less than 400 ohms can be accepted if the 1,600-ohm line impedance option at the network side is applicable);
— the absence of wetting current shall not have any influence on the performance of the TU.

6. **DCE POWER-OFF SIGNAL** (used in the NPDN for the purpose of causing the appropriate call progress signal (47) to the calling DTE)

The TU shall be provided with a "Power-off" generator which shall be connected to the line, if one or more of the power supply voltages fail(s) for more than 30 ms.
When the power-off generator is activated, a square wave oscillator shall be switched on and connected to the line, transmitting a signal with the frequency 1,000 ± 100 Hz for the TUB and 1,800 ± 200 Hz for the TUM. This signal shall be modulated with a square wave of the frequency 1.7-3 Hz, so that the signal is ON 35-65% of the time, and OFF 65-35% of the time. The modulation shall always start with an OFF-period longer than 100 ms. The transmit level shall be the same as with the data signal.
The power-off generator shall be able to work with a current supply of 5-15 mA. The power-off generator will be powered either from accumulators situated in the DCE or from the wetting current on the receiver line. When powered from the accumulators these shall be able to power the power-off generator for at least 70 continuous hours. When powered from the wetting current in the receiver line, it shall be independent of the branch polarities. The TU shall function properly until the power-off generator is turned ON. The voltage drop over the power-off generator shall be within the range 5-8 V.

7. **CHARACTER ALIGNMENT** (applies only if character alignment is established in the DCE)
(Used in the NPDN)

The DCE synchronizes on the first SYN-character from the DTE with control = ON after passing clearing and having detected READY (data = 1 and the status bit = 0 in one envelope) in both directions. All SYN-characters are sent to the network. If the DCE has synchronized on a SYN-character, the DTE can take place until READY has been redetected in both directions after clearing.
When tested, the DCE synchronizes on the first SYN-character occurring after initiation of the test.
As long as the DCE regards itself as being in data transfer phase, no synchronization on SYN-characters takes place. The DTE will then be responsible for establishing its own alignment, e.g. by using the byte timing or by SYN-characters.
When the DCE detects an envelope with data = 1 and status = 1 in both directions to and from the DCE, the DCE is regarded as being in data transfer phase.
When the DCE detects CLEAR from the network (data and status = 0 in two envelopes) or CLEAR from the DTE, or receives time-out after loss of envelope alignment, the DCE is regarded as no longer being in data transfer phase.

8. **ELECTRICAL CHARACTERISTICS AND SIGNIFICANT LEVELS** of the interchange circuits between the TU and the CU (see also the note under Section A, item 2.1.2.).

8.1. **Possibility A**

The same electrical characteristics and significant levels are used as for the interface between the CU and the terminal (see Section A, item 3.2.3.).

8.2. **Possibility B (Deutsche Bundespost)**

For the IDN a particular set of characteristics for an unbalanced single-current interface was developed and is described below (the so-called EDS-A-interface).

8.2.1. *Generator characteristics*

The generator in an interchange circuit shall withstand an open circuit and a short circuit condition between itself and any other interchange circuit (including generators and loads) without sustaining damage to itself or its associated equipment.

The open circuit voltage (U_O) shall be

for the OFF/ZERO condition	$U_O = 0\ V\ ^{+0.5\ V}_{-1.5\ V}$
for the ON/ONE condition	$U_O = 5\ V\ ^{+1.5\ V}_{-0.5\ V}$
The generator impedance is	$R_A = 100$ ohms $\pm 10\%$
The maximum generator shunt capacitance is	$C_{A\,max} = 2$ nF
The rise time shall be	$S \geq 0.2$ V/µs within the range $U_A = +1.2$ V ... $+2.8$ V

(When terminated with the nominal load as defined in 8.2.2.)

8.2.2. *Load characteristics*

The load circuitry recognizes

the OFF/ZERO condition at an input voltage $U_E \triangleq +1.2$ V

the ON/ONE condition at an input voltage $U_E \geq +2.8$ V

The region between $+1.2$ V and $+2.8$ V is defined as the transition region. The maximum tolerable input voltage is ± 8 V.

The load impedance is	$R_E = 400$ ohms $^{+10\%}_{-40\%}$
The load shunt capacitance is	$C_E = 10$ nF $\pm 25\%$

A power-off condition at the input of the load shall be recognized as OFF/ZERO condition.

8.2.3. *Positions of the Timing Signal Transitions*

For the EDS-A-interface the relationship between either timing signal and the corresponding data signal is such that a transition from the OFF to ON conditions of the timing signal shall nominally indicate the centre of each signal element of the data stream.

Note: This is contrary to the regulation in CCITT Recommendation V.24.

9. CONNECTOR (CU TO TU) USED BY THE DEUTSCHE BUNDESPOST

The connector is a 31-pin connector according to DIN 41617. The pin assignment is given in Table 6.

Pin No.	Access point designation	Circuit name
1	G	Signal ground or common return
2	+5 V	Power supply circuit
3	Di	Transmitted data
4	G	Signal ground or common return
5	TS1i	Transmitter signal element timing (CU)
6	G	Signal ground or common return
7	Do	Receiver Data
8	G	Signal ground or common return
9	RS1o	Receiver signal element timing
10	G	Signal ground or common return
11	Ao	Received line signal detector
12	LA1i	Loop 3a activation
13	TS2o	Transmitter signal element timing (TU)
14	G	Signal ground or common return
15	—	
16	+12 V	Power supply circuit
17	(RS1i)	(not used)
18	G	Signal ground or common return
19	RS2o	8× or 6× clock of RS1
20	—	
21	—	
22	TS3o	8× or 6× clock of TS2
23	—	
24	Lo a (La)	Line outgoing a-wire (Line a-wire for 2-wire TUB)
25	Lo b (Lb)	Line outgoing b-wire (Line b-wire for 2-wire TUB)
26	G	Signal ground or common return
27	Li a	Line incoming a-wire
28	Li b	Line incoming b-wire
29	G	Signal ground or common return
30	G	Signal ground or common return
31	−12 V	Power supply circuit

Table 6.

10. TRANSMIT INHIBIT FUNCTION

The following maintenance function shall be included. If the received line signal detector is in the OFF condition, transmission in the opposite direction shall cease either after a time delay of 2.5 seconds or be alternatively controlled by the CU via the use of interchange circuit LEA. When a timer within the modem is used to control the transmit inhibit function, this function shall be implemented in such a way that the MTBF for all the circuitry of concern for this function is at least one magnitude greater than the MTBF for the whole modem.

Section C

1. GENERAL

This section specifies optional requirements which may be included in a plug-in DCE.

2. OPTIONAL INTERCHANGE CIRCUITS

2.1. Interface between TU and CU

(a) The following Table 7 gives a list of optional circuits for the interface between TU and CU.

Circuit designation	Circuit name	Access point designation CU	TU
DT_2	Transmitted data (line receiver)	$Do_2 \rightarrow Di_2$	
DR_2	Received data (line driver)	$Di_2 \leftarrow Do_2$	
$RS1_2$	Receiver signal element timing	$RS1i_2 \leftarrow RS1o_2$	
$RS2_2$	8× or 6× clock of RS1	$RS2i_2 \leftarrow RS2o_2$	
TS1	Transmitter signal element timing (CU) (*Note 1*)	TS1o→TS1i	
TS2	Transmitter signal element timing (TU) (*Notes 1 and 2*)	TS2i←TS2o	
TS3	8× or 6× clock of TS2 (*Notes 1, 2*)	TS3i←TS3o	
MC	Master clock	MCo→MCi or MCi←MCo	or
SQ	Signal quality	SQi←SQo	
RC	Relais control (*Note 1*)	RCo→RCi	
LEA	Loss of envelope alignment	LEAo→LEAi	
LA1	Loop 3a activation	LA1o→LA1i	
−12 V	Power supply circuit	−12	−12
+12 V	Power supply circuit	+12	+12
+ 5 V	Power supply circuit	+ 5	+ 5

Table 7.

Note 1: The electrical characteristics of Section B, item 8 may not be relevant to this circuit.

Note 2: If maintenance loop 3a is activated, the internal transmit clock of the DCE must be switched to "master operation".

(b) Definitions of the optional circuits

Circuit DT_2, DR_2, $RS1_2$, $RS2_2$
The purpose of these circuits is the same as for DT, DR, RS1 and RS2 (see Section A, item 2.1.2.(b)). The difference is that the electrical characteristics of these circuits may be different.

Circuit TS1 – Transmitter signal element timing (CU)
Signals on this circuit provide the TU with signal element timing information. The condition on this circuit shall be ON and OFF for nominally equal periods of time, and the transition from the ON to OFF condition shall nominally indicate the centre of each signal elements on circuit DT.

Circuit TS2 – Transmitter signal element timing (TU)
Signals on this circuit provide the CU with signal element timing information. The condition on this circuit shall be ON and OFF for nominally equal periods of time. The CU shall present a data signal on circuit DT in which the transitions between signal elements nominally occur at the time of the transition from the OFF to ON condition of circuit TS2.

Circuit TS3 – 8× or 6× clock of TS2
The number of transitions from ON to OFF on this circuit should be 8× higher than on circuit TS2 for a 10-bit envelope structure and 6× higher for an 8-bit envelope structure. Each transition from ON to OFF of TS2 corresponds also with an ON to OFF transition of TS3.

Circuit MC – Master clock
Signals on this circuit provide either in one direction the TU or in the other direction the CU with the master clock (e.g. processor clock) which is not further specified here.

Circuit SQ – Signal quality
Signals on this circuit indicate whether there is a reasonable probability of an error in the data received on the data channel. The ON condition indicates that there is no reason to believe that an error has occurred. The OFF condition indicates that there is a reasonable probability of an error.

Circuit RC – Relay control
Signals on this circuit (from the power supply) control whether the "Power OFF" generator shall be connected to the line or not. A high voltage disconnects the "Power OFF" generator from the line and a low voltage connects the "Power OFF" generator to the line.

Circuit LEA – Loss of envelope alignment
Signals on this circuit indicate whether there is a loss of envelope alignment. The ON condition indicates that there is a loss of envelope alignment, the OFF condition indicates that there is no loss of envelope alignment.

Circuit LA1 – Loop 3a activation
Signals on this circuit are used to control the loop 3a test condition in the local TU. The ON condition of circuit LA1 causes the establishment of the loop 3a test condition, the OFF condition causes the release of the loop 3a test condition.

2.2. Interface between CU and terminal

The following Table 8 gives a list of optional interchange circuits for the interface between CU and terminal:

Circuit designation	Circuit name	Direction from CU	Direction to CU
B	Byte timing (*Note 1*)	X	
TA	Test activation		X
TI1	Test indication	X	
TI2	Test O.K.	X	
LA2	Loop 2 activation		X
LA3	Loop 3c or 3d activation		X
+12 V	Power supply circuit		X
−12 V	Power supply circuit		X
+ 5 V	Power supply circuit		X

Table 8.

Note 1: The relationship between T, R, S and B is given in Annex 4.

3. TEST POINTS

Appropriate signal monitoring and level measuring test points may be provided in the TU (see Annex 2).
Test access points shall be provided by the DCE at the interface between the DCE and the terminal e.g. for monitoring procedures. These test points shall be easily accessible.

4. CONSTRUCTION

The plug-in DCE may be housed in a closed cabinet. In this case provision shall be made to allow sealing of the cabinet. Opening of the cabinet shall not be possible without breaking the seal.

PART II (TYPE II)

Section A

1. GENERAL

The type II DCE for 2,400 bit/s consists of notionally two functional units, the transmission unit (TU) and the conversion unit (CU). However, these two notional functional units are envisaged as being sufficiently closely integrated so as to dispense with the need to specify an internal digital interface between the CU and the TU. Consequently, in the following items the equipment as a whole is specified and is referred to as the DCE.

1.1. Four types of voice band DCE are specified.

i) Alternative A1 defines a 2,400 bit/s DCE conforming to CCITT Recommendation V.27*bis* — 4-wire duplex

ii) Alternative A2 defines a 2,400 bit/s DCE conforming to CCITT Recommendation V.26 — 4-wire duplex

iii) Alternative B1 defines a 2,400 bit/s DCE conforming to CCITT Recommendation V.26*ter* — 2-wire duplex

iv) Alternative B2 defines a 2,400 bit/s DCE conforming to CCITT Recommendation V.22*bis* — 2-wire duplex

For DCE's using base band transmission techniques see Section B, item 2.

1.2. The requirement in this specification and CEPT specification Recommendation T/CD 01-01 taken together define the facilities for the DCE.

1.3. In the specifications requirements pertaining to 2,400 bit/s are stated first, and the equivalent requirements pertaining to 1,200 bit/s operation, where applicable, are shown in brackets immediately following the 2,400 bit/s requirements, thus 2,400 (1,200).

1.4. **Interchange circuits**

The interchange circuits listed in Table 1 shall be provided. The interface shall conform to the definitions and functional requirements indicated below.

The electrical characteristics of these circuits shall be as defined in Part I, Section A, item 3.2.3.

Interchange circuit designation	Interchange circuit name	Direction from DCE	Direction to DCE
102 (G)	Signal ground or common return *(Note 1)*		
103 (T)	Transmitted data		X
104 (R)	Received data	X	
107	Data set ready	X	
109 (I)	Data channel received line signal detector	X	
114	Transmitter signal element timing	X	
115 (S)	Receiver signal element timing	X	
142	Test indicator		

Note 1: This interchange circuit is identical with power supply common return.

Table 1. Interchange circuits.

1.4.1. *Circuit 103 (T)*

Data signals on circuit 103 (T) are transmitted to the network, whenever the DCE is operational.

Note: DTE manufacturers should be aware that immediately after the "DTE/DCE power-up" data transmitted via circuit 103 (T) may be mutilated in the network.

1.4.2. *Circuit 104 (R)*

The DCE shall present on circuit 104 (R) the data signals received from the network, when circuit 109 (I) is in the ON condition. The signal on circuit 104 (R), when circuit 109 (I) is in the OFF condition, is not specified.

1.4.3. *Circuit 107*

Circuit 107 shall be kept permanently in the ON condition.

1.4.4. *Circuit 109 (I)*

The DCE shall present the OFF condition on circuit 109 (I) when no incoming carrier is detected by the DCE, when an incoming carrier is detected by the DCE but the DCE is not yet synchronized, or when a test loop towards the network is activated.

For the DCE the relation between the level of the incoming carrier and circuit 109 (I) shall be as follows:
greater than −43 dBm circuit 109 (I) ON
less than −48 dBm circuit 109 (I) OFF.

The condition of circuit 109 (I) between the ON and OFF levels is not specified except that the signal detector shall exhibit a histeresis action, such that the level at which the OFF to ON transition occurs shall be at least 2 dB greater than that for he ON-to-OFF transition.

Where transmission conditions are known and allowed, it may be desirable at the time of DCE installation to change these response levels of the received line signal detector to less sensitive values (e.g. −33 dBm and −38 dBm respectively).

In addition, for use over special-quality leased circuits (Ref. Recommendation M1020) the response levels of the received line signal detector shall be:
greater than −26 dBm circuit 109 (I) ON
less than −31 dBm circuit 109 (I) OFF.

The purchasing Administration may specify thresholds different to the above.

1.4.5. *Circuits 114 and 115 (S)*

A timing signal derived from the received data signal is presented on both circuits 114 and 115 (S). The free running accuracy of this timing signal shall be at least ± 0,01%. The period length of this timing signal shall not deviate from the nominal value for more than 4%. The relationship between circuits 103 (T), 104 (R) and 115 (S) is given in the following Figure 1 (including tolerances).

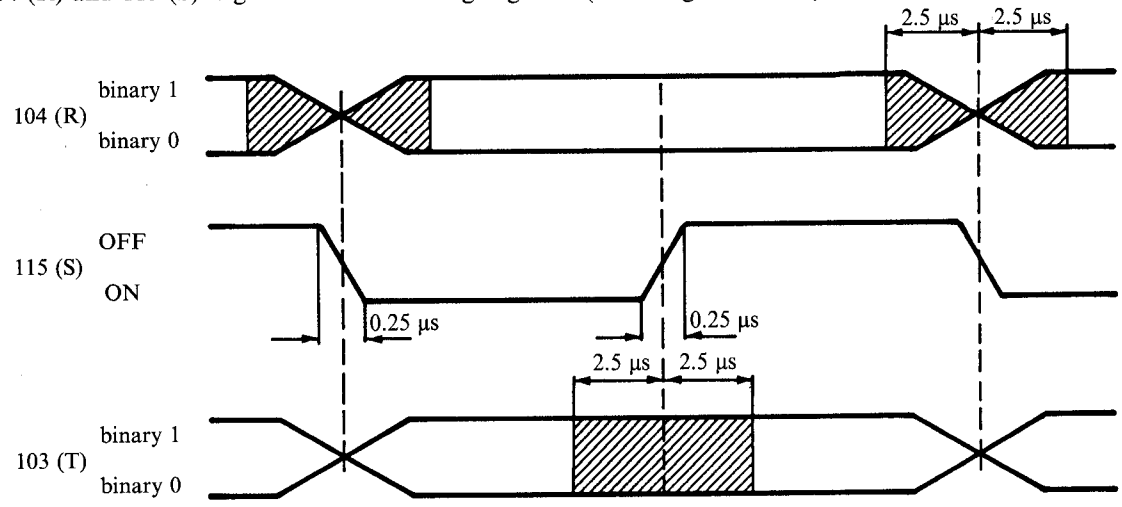


Figure 1.

1.4.6. *Circuit 142*

The DCE will indicate internal test mode with the ON condition on circuit 142.

1.5. **Alarms and consecutive actions**

In Annex 13 a state diagram is given (the same description method is used as in Annex 6).

The state diagram reflects the requirements which are mentioned in Section A, item 1.4.4. (Annex 13, state A1) and Section C, item 3. (Annex 13, state ICS, HF, A2).

2. REQUIREMENTS FOR ALTERNATIVE A1

2.1. Modulation

The modulation is in accordance with CCITT Recommendation V.27*bis*, fall back mode.

2.2. Scrambling

The scrambler is in accordance with CCITT Recommendation V.27*bis*.

2.3. **Operating sequence**

In accordance with CCITT Recommendation V.27*bis*. On a national basis an optional sequence may be introduced.

2.4. **Base-band shaping**

A minimum of 50% raised cosine energy spectrum shaping is equally devided between the receiver and transmitter.

3. REQUIREMENTS FOR ALTERNATIVE A2

3.1. **Modulation**

The modulation is in accordance with CCITT Recommendation V.26 type A and/or B.

3.2. **Scrambling**

On a national basis a strappable V.27 scrambler or a scrambler as described in Part I, Section A, item 2.1.4. may be introduced.

3.3. **Base-band shaping**

A 100% raised cosine amplitude spectrum shaping is divided in the following way: 1/3 emitter, 2/3 receiver.

4. REQUIREMENTS FOR ALTERNATIVE B1

The characteristics of the DCE are in general defined in Part III, Section A, item 4. However, scrambler/descrambler allocation, data signalling rate selection and call mode/answer mode designation on point-to-point based circuits will be determined by bilateral agreement between users.

5. REQUIREMENTS FOR ALTERNATIVE B2

The characteristics of the DCE are in general defined in Part III, Section A, item 5. However, channel allocation and signalling mode selection on point-to-point based circuits will be determined by bilateral agreement between users.

Also operation of point-to-point based circuits will be "constant carrier" in both directions, the operating sequences being in accordance with Part III, Section A, items 5.4, 5.5.

6. TEST LOOPS

The definitions of the loops are set out in CCITT Recommendation X.150.

6.1. **Local test loop – loop 3**

In order to assist the testing of the DCE, test loop 3 is provided in the DCE. The precise implementation is network dependent and indicated in Section B, item 3.1.

6.2. **Network test loop – loop 2b**

For maintenance purposes, a loop 2b is implemented in the DCE. This loop is activated within the test procedure (see Section B, item 3.2.).

If the loop towards the network is activated, the DCE will signal "DCE not ready" (109 (I) is OFF, 104 (R) not specified) towards the terminal and apply an ON condition to circuit 142.

6.3. **Additional loops may be provided,** see Section B, item 3.1.

7. POWER CONSUMPTION

Ref. to Part I, Section A, item 5.

8. CONSTRUCTION

Ref. to Part I, Section A, item 6.

9. ENVIRONMENTAL REQUIREMENTS

Ref. to Part I, Section A, item 7.

Section B

1. **GENERAL**

This section specifies national network-dependent requirements which have to be included in a plug-in DCE at the discretion of the Administrations.

2. **BASE AND DCE's**

2.1. **Alternative C1 (British Telecom)**

(See Part I, Section B, item 2.1.)

2.2. **Alternative C3 (Deutsche Bundespost)**

(See Part I, Section B, item 2.3.)

2.3. **Alternative C6 (France)**

2.3.1. *Modulation and coding*

The coding method shall be the differential diphase transmission. This consists in a phase reversal from the previous basic element when a binary ONE is transmitted, and in no phase reversal from the previous basic element when a binary ZERO is applied.

The two basic elements of the unfiltered differential signal are shown in Figure 2.

Figure 2. Differential diphase basic elements.

These elements are sent at a frequency corresponding to the data signalling rate.

2.3.2. *Scrambling*

Data scrambling is not used.

2.3.3. *Line interface*

(a) The nominal input and output impedances shall be 600 ohms.

(b) The return loss shall be 20% in the bandwidth occupied by the spectrum of data signals.

2.3.4. *Line signal requirements*

(a) The requirements of Recommendation T/CD 01-01 shall apply.

(b) The transmit level shall be 6 volts peak-to-peak at a resistive impedance of 600 ohms.

(c) The receiver shall be designed to recover a line signal transmitted via an unamplified line having an insertion loss of up to 40 dB at a frequency corresponding to the data signalling rate.

The attenuation distortion in dB is proportional to the square root of the frequency.

The signal detector shall have a hysteresis of at least 2 dB and check coding patterns.

2.3.5. *Equalization*

An adaptive equalizer shall be included.

2.3.6. *Synchronization time*

The time that elapses between the OFF-to-ON transition of circuit 105 at one end and the reception of the first ten error free bits at the other end must be within 64-bit intervals assuming zero propagation delay.

2.4. **Alternative D1 (Deutsche Bundespost)**

(See Part I, Section B, item 2.6.)

2.5. **Alternative D3 (France)**

Alternative D3 is a two-wire duplex base-band DCE using the echo cancellation technique.

2.5.2. *Scrambler and descrambler*

Each transmission direction uses a different scrambler.

A self-synchronizing scrambler/descrambler shall be included in the DCE.

According to the direction of transmission the generating polynomial is:

$$GPC = 1 + X^{-6} + X^{-7}$$

or

$$GPA = 1 + X^{-1} + X^{-7}$$

2.5.3. *Line interface*

The same requirements as for Alternative C6.

2.5.4. *Line signal requirements*

The same requirements as for Alternative C6.

2.5.5. *Equalization*

The same requirements as for Alternative C6.

2.5.6. *Synchronization time*

The time that elapses between the OFF-to-ON transition of circuit 105 at one end and the reception of the first ten error free bits at the other end must be within 2,000 to 3,000-bit intervals assuming a zero propagation delay.

3. TESTING AND MEASURING REQUIREMENTS

3.1. **Test loops** (see Figure 3)

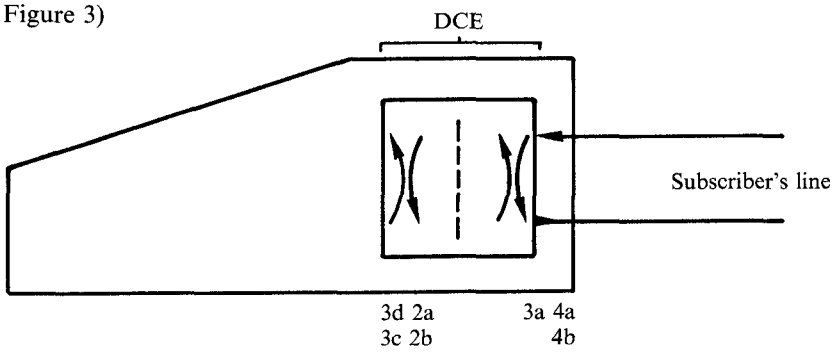


Figure 3.

Two further types of test loops in addition to loop 2b (see Section A, item 6) may be provided in the DCE:

(a) Test loops towards the DTE
  loop 3a/3b: this loop is automatically activated, locally controlled (see Part I, Section A, 2.1.5., *Note 4*)
  loop 3c/3d: this loop is manually or automatically activated, locally controlled.

(b) Test loops towards the network
  loop 4a/4b: this loop is manually activated, locally controlled.

If the loop is activated, the DCE will signal "DCE not ready" (109 (I) = OFF, 104 (R) = not specified) towards the terminal.

The following Table 2 gives the various additional test loops which are used in different networks as identified so far:

Network	Test loops				
	3a	3b	3c/3d	4a	4b
F		X		X *(Note 1)*	X *(Note 2)*
NL			X	X	
UK	X				

Note 1: for TUB.

Note 2: for TUM.

Table 2.

3.2. **Test procedure**

A test loop 2 is controlled by the network or by the remote DCE. The signalling to the DCE is in line with Recommendation V.54 except for 2-wire Alternative B2 DCE's.

Section C

1. GENERAL

This section specifies optional requirements which may be included in a plug-in DCE.

2. OPTIONAL INTERCHANGE CIRCUITS

The following Table 3 gives a list of optional interchange circuits for the interface between DCE and terminal:

Interchange circuit designation	Interchange circuit name	Direction from DCE	Direction to DCE
105 (C)	Request to send		X
106	Ready for sending	X	
108/2	Data terminal ready		X
111	Data signalling rate selector (DTE source)		X
112	Data signalling rate selector (DCE source)	X	
113	Transmitter signal element timing (DTE source)		X
140	Loopback/maintenance test		X
141	Local loopback		X

Table 3.

3. FUNCTIONAL REQUIREMENTS OF THE INTERFACE BETWEEN DCE AND TERMINAL

3.1. The DCE will present circuit 109 (I) in the OFF condition when receiving more than 64 contiguous binary ones from the network.

3.2. If possible, the DCE will present circuit 109 (I) in the OFF condition when detecting internal malfunctioning.

3.3. The DCE will prevent a transmission of an outgoing carrier when no incoming carrier is received for a period longer than 2-3 s.

3.4. It shall be possible to provide an independent timing signal on circuit 114, which controls data on circuit 103 (T).

3.5. Circuit 105 (C) may or may not control the transmission of the carrier towards the network.
Data signals on circuit 103 (T) are transmitted to the network when circuit 105 (C) is in the ON condition and when the data link is synchronized.
In the continuous carrier mode, continuous "I" is transmitted towards the network when circuit 105 (C) is in the OFF condition.

3.6. Circuit 106 response times depend on the DCE specifications and are defined in the appropriate sections (see Section A, item 1.1.).

4. OPTIONAL MODES OF OPERATION

See Part III, Section C, item 4.

5. TEST POINTS

See Part I, Section C, item 3.

6. CONSTRUCTION

See Part I, Section C, item 3.

PART III (TYPE III)

Section A

1. GENERAL

1.1. Four types of DCE's are specified:

(a) Alternative A1 defines a 2,400 bit/s half duplex DCE conforming to CCITT Recommendation V.27*ter*.

(b) Alternative A2 defines a 2,400 bit/s half duplex DCE conforming to CCITT Recommendation V.26*bis*.

(c) Alternative B1 defines a 2,400 bit/s duplex DCE conforming to CCITT Recommendation V.26*ter*.

(d) Alternative B2 defines a 2,400 bit/s duplex DCE conforming to CCITT Recommendation V.22*bis*.

1.2. The requirements of this specification and CEPT specification Recommendation T/CD 01-01 taken together define the facilities for the DCE.

1.3. In this specification, requirements pertaining to 2,400 bit/s are stated first and the equivalent requirements pertaining to 1,200 bit/s operation are shown in brackets immediately following the 2,400 bit/s requirements, thus −2,400 (1,200) bit/s.

1.4. **Interchange circuits**

The interchange circuits listed in Table 1 shall be provided. The interface shall conform to CCITT Recommendation V.24 for the definitions and functional requirements. The electrical characteristics of these circuits shall be as defined in Part I, Section A, item 3.2.3.

Interchange circuit designation	Interchange circuit (name)	Direction from CU	Direction to CU
102	Signal ground or common return		
103	Transmitted data		X
104	Receive data	X	
105	Request to send		X
106	Ready for sending	X	
107	Data set ready	X	
108/1	Connect data set to line		X
108/2	Data terminal ready		X
109	Data channel received line signal detector	X	
111	Data signalling race selector (DTE source)		X
113	Transmitted signal element timing (DTE source)		X
114	Transmitted signal element timing (DCE source)	X	
115	Receive signal element timing (DCE source)	X	
125	Calling indicator		X
140	Loopback/Maintenance test		X
141	Local loopback		X
142	Test indicator	X	
+12 V	Power supply circuit		X
−12 V	Power supply circuit		X
+ 5 V	Power supply circuit		X

Table 1.

1.4.1. *Circuit 108*

This circuit shall be capable of operating like circuit 108/1 or 108/2, depending on its use. For automatic calling it shall be used as 108/2 only.

1.4.2. *Circuit 109*

Circuit 109 thresholds shall be:
Greater than −43 dBm circuit 109 ON
Less than −48 dBm circuit 109 OFF.

The condition of circuit 109 between the ON and OFF levels is not specified except that the signal detector shall exhibit such a hysteresis action that the level at which the OFF-to-ON transition occurs shall be at least 2 dB greater than that for the ON-to-OFF transition.

Circuit 109 thresholds are specified at the input to the DCE when receiving scrambled binary 1.

The purchasing Administration may specify thresholds different to the above.

1.4.3. *Circuit 111*

The ON condition of circuit 111 shall select 2,400 bit/s operation and the OFF condition shall select 1,200 bit/s operation.

1.4.4. *Circuit 114*

When circuit 114 is used, the timing on this circuit shall be derived from an internal clock source or alternatively from received signal element timing.

2. REQUIREMENTS FOR ALTERNATIVE A1

See Part II, Section A, item 2.

3. REQUIREMENTS FOR ALTERNATIVE 2

See Part II, Section A, item 3.

4. REQUIREMENTS FOR ALTERNATIVE B1

The principal characteristics of this DCE are as follows:

(a) Duplex mode of operation.
(b) Channel separation by echo cancellation.
(c) Differential phase shift modulation for each channel with synchronous line transmission at 1,200 baud (nominal).
(d) Inclusion of a scrambler.
(e) Inclusion of a compromise or adaptive equalizer.
(f) Inclusion of test facilities.
(g) Operation with data terminal equipment (DTE) in the following modes:
2,400 bit/s synchronous;
1,200 bit/s synchronous (fall-back rate).
(h) Inclusion of an operating sequence intended to allow interworking with 2-wire duplex 4,800 bit/s DCE (this DCE is for further study).

4.1. Data signalling rate

The data rate transmitted to line shall be 2,400 (1,200) bit/s ±0.01% with a modulation rate of 1,200 baud ±0.01%.

4.2. Interchange circuits

4.2.1. *Circuit 106 response times* (see Table 2)

Circuit 106 response times vary with the application of an ON or OFF condition on circuit 105. See also item 4.3.6. for conditions of circuit 106 during the operating sequence.

	Constant carrier	Controlled carrier	
		2,400 bit/s	1,200 bit/s
OFF to ON	≤2 ms	60±7 ms	120±14 ms
ON to OFF	≤2 ms	≤2 ms	≤2 ms

Table 2.

4.2.2. *Circuit 109 response times*

Circuit 109 must turn ON after synchronizing is completed and prior to user data appearing on circuit 104.

The ON-to-OFF response time of circuit 109 is 5 ms to 15 ms (see also item 2.3.6.2. for condition of circuit 109 during the operating sequence).

Following a drop-out after the initial handshake, circuit 109 shall be turned ON 40 to 50 ms after the level of the receiver signal appearing at the line terminal of the modem exceeds the relevant threshold defined in item 1.4.2.

4.2.3. *Timing arrangement*

Clocks shall be included in the DCE to provide the data terminal equipment with transmitter element timing, circuit 114, and receiver signal element timing, circuit 115. The transmitter element timing may be originated in the data terminal equipment and be transferred to the DCE via the appropriate interchange circuit, circuit 113.

4.3. **Modulation and coding**

The principal characteristics of the DCE are channel separation by echo cancellation and differential phase shift modulation for each channel with synchronous line transmission at 1,200 baud (nominal).

4.3.1. *Carrier frequency*

The carrier frequency is to be 1,800 ± 1 Hz.
No separate pilot tones are provided.

4.3.2. *Line signal encoding*

4.3.2.1. 2,400 bit/s

At 2,400 bit/s the data stream is divided into groups of two bits (dibits). Each dibit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 3). At the receiver, the dibits are decoded and reassembled in the correct order. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

Dibit values	Phase change (see *Note 1*)
00	0°
01	90°
11	180°
10	270°

Table 3. Line encoding at 2,400 bit/s.

4.3.2.2. 1,200 bit/s

At 1,200 bit/s each bit shall be encoded as a phase change relative to the phase of the preceding signal element (see Table 4).

Bit values	Phase change (see *Note 1*)
0	0°
1	180°

Table 4. Line encoding at 1,200 bit/s.

Note 1: The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

4.3.3. *Spectrum and group delay characteristic*

A 100% raised cosine amplitude spectrum shaping is equally divided between the receiver and transmitter. The energy density at 1,200 Hz and 2,400 Hz shall be attenuated 3.0 dB ± 2.0 dB with respect to the maximum energy density between 1,200 Hz and 2,400 Hz.

The group delay of the transmit filters shall be within ± 100 microseconds over the frequency range 1,200-2,400 Hz.

4.3.4. *Received signal frequency tolerance*

Noting that the frequency tolerance of the transmitted carriers is ± 1 Hz or less, and assuming a maximum shift of ± 6 Hz in the connection, the receiver shall meet the specified performance requirements with a received frequency offset of ± 7 Hz.

4.3.5. *Equalizer*

If a fixed compromise equalizer is used, it shall be incorporated in the receiver. The characteristics of this equalizer may be selected by Administrations.

Possibility of producing a compromise equalizer characteristic for international connections is for further study.

If an adaptive equalizer is used, it shall be able to converge to data signals at 2,400 bit/s without a training sequence.

4.3.6. *Operating sequences*

4.3.6.1. Scrambler/descrambler allocation and data signalling rate selection

In the general switched telephone network the DCE at the calling data station shall use the scrambler with GPC generating polynomial and the descrambler with GPA generating polynomial (Call Mode). The DCE at the answering data station shall use the scrambler with GPA generating polynomial and the descrambler with GPC generating polynomial (Answer Mode).

In some situations, however, when e.g. calls are established on the GSTN by operators, bilateral agreement on call mode/answer mode allocations will be necessary.

The calling and answering DCE's automatically condition themselves to operate at the correct data signalling rate by exchanging rate patterns at the bit rate of 1,200 bit/s during the operating sequences, as defined in paragraph 4.3.6.5.

4.3.6.2. Rate patterns

The rate pattern is a scrambled sequence of a particular repeated octet transmitted 32 times.

Out of the possible 256 binary numbers, the 34 following hexadecimal numbers are selected:
01–03–05–07–09–0B–0D–0F–11–13–15–17–19–1B–1D–1F–25–27–
2B–2D–2F–33–35–37–3B–3D–3F–55–57–
5B–5F–6F–77–7F.

Each of the numbers listed above may be replaced by one of its rotations.

The transmission of an octet begins by the least significant bit.

Table 5 shows the relationship between an octet value and one or two (see *Note 2*) bit rates enabled in a DCE.

Octet (*Note 1*)		Bit rate (bit/s)		
Hexa-decimal	Binary (LSB)	1,200	2,400 (*Note 2*)	4,800
01	0 0 0 0 0 0 0 1	X		
03	0 0 0 0 0 0 1 1		X	
05	0 0 0 0 0 1 0 1			X
07	0 0 0 0 0 1 1 1	X	X	
09	0 0 0 0 1 0 0 1		X	X

Table 5. Rate pattern octet coding.

Note 1: In case of an interface according to Recommendation V.24, only two rates can be selected by circuits 111 and 112. A new kind of interface under study may enlarge the possibility.

Note 2: These octet assignments are provisional.

4.3.6.3. Synchronizing signals

The synchronizing signals are used in operating sequence.

The synchronizing signals, for both data signalling rates, are divided into two segments as follows:

4.3.6.3.1. The composition of segment 1 is continuous 180° phase reversals for 32 symbol intervals.

4.3.6.3.2. Segment 2 is a pattern derived from scrambling binary ones with the scramblers defined in item 4.4. The length of the pattern is 64 bits (32 symbol intervals) for 2,400 bit/s, and 64 bits (64 symbol intervals) for 1,200 bit/s; the patterns are defined in Table 6.

Data signal-ling rate	Scrambler	Segment 2 Phase changes (c)
2,400 bit/s	GPC	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 0, 90, 180, 0, ...
2,400 bit/s	GPA	0, 180, 180, 180, 180, 0, 0, 0, 0, 180, 180, 270, 90, 180, 0, 180, 270, 270, 0, ...
1,200 bit/s	GPC	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180 180, 0, 0, 180, 180, 180, 0, 0, 0, 0, 0, 180, 180, 180, ...
1,200 bit/s	GPA	0, 0, 180, 180, 180, 180, 180, 180, 180, 180, 0, 0, 0, 0, 0, 0, 0, 0, 180, 180, 180, 180, 180, 0, 0, 180, 180, 180, 0, 0, 180, 180, 180, 0, 180, 0, ...

Table 6.

4.3.6.4. V.25 Automatic answering sequence

The V.25 automatic answering sequence shall be transmitted from the answer mode DCE on international GSTN connections. The transmission of the sequence may be omitted on point-to-point leased circuits or on national connections on the GSTN, where permitted by the Administration.

4.3.6.5. Operating protocol

The means of achieving automatic bit rate selection, initial echo cancellation and synchronism between the call mode and the answer mode DCE's on international GSTN connections and leased lines are shown in Figure 1.

The automatic bit rate selection, initial echo cancellation and synchronizing signals are based on a half-duplex procedure. After this procedure, both DCE's shall continue to operate adaptive echo cancellation during duplex data transmission.

The operating sequence is divided into three sequences A, B and C (see *Note*).

The sequence A is the answering sequence according to Recommendation V.25.

The sequence B is the data bit rate selection sequence, operated at 1,200 bit/s.

The sequence C is the echo cancelling procedure operated at the selected bit rate.

At the end of these three sequences, the DCE has to be able to transmit and receive data.

Note: Manufacturers should note that the impedance of the DCE's as seen from the telephone line connection should not be varied throughout the duration of the connection.

4.3.6.5.1. Sequence A (answering sequence)

— Call mode DCE

(a) On connection to line, it shall condition the scrambler and the descrambler in accordance with item 4.3.6.1.

(b) In accordance with Recommendation V.25, after the detection of the 2,100 Hz tone and a silent period of 75 ± 20 ms, the DCE shall apply an ON condition to circuit 107.

— Answer mode DCE

(a) On connection to line, it shall condition the scrambler and the descrambler in accordance with item 4.3.6.1.

(b) In accordance with Recommendation V.25, the DCE is silent during 2.15 ± 35 s, and sends a $2{,}100 \pm 15$ Hz tone for 3.3 ± 7 s, then remains silent for 75 ± 20 ms.

(c) In accordance with Recommendation V.25 after the silent period, it shall apply an ON condition to circuit 107.

4.3.6.5.2. Sequence B (data bit rate selection sequence)

The call and the answer mode DCE's are conditioned to transmit and receive at 1,200 bit/s in a half-duplex mode.

— Call mode DCE

(a) The DCE waits until it detects at least 4 consecutive error-free octets of the rate pattern (*Note 1*). The calling DCE selects the maximum rate compatible with the answering DCE or the maximum rate it can transmit.

(b) Then that it transmits it remains silent during 250 ± 5 ms.

(c) After the synchronization sequence followed by 256 bits of a rate pattern corresponding to the selected bit rate in accordance with item 4.3.6.2. (*Note 1*).

(d) Then it applies the appropriate condition to circuit 112 (if used).

— Answer mode DCE

(a) The DCE transmits the receiver synchronization signals followed by 250 bits of the rate pattern which indicates the set of rates available for the answering DCE in accordance with item 4.3.6.2.

(b) The DCE remains silent until it detects at least 4 consecutive error-free octets of a rate pattern. If a rate pattern is not detected within 2 s following the end of the rate pattern transmitted by the answering DCE, it shall resume the operating sequence at the beginning of sequence B.
If the rate pattern indicates a rate not available the DCE is disconnected from the line.
If the rate pattern indicates an available rate, the DCE applies the appropriate condition to circuit 112 (if used).

(c) Then it remains silent again during 250 ± 5 ms.

(d) In accordance with Recommendation G.164, the DCE transmits a $2{,}100 \pm 15$ Hz tone for 500 ± 50 ms to disable echo suppressors, then remains silent for 75 ± 20 ms.

4.3.6.5.3. Sequence C (echo cancelling procedure)

The call and the answer mode DCE's are conditioned to transmit, to receive and to cancel the echo at the selected data bit rate.

— Call mode DCE

(a) The DCE remains silent until 64 consecutively received scrambled binary ZERO's are detected. The DCE shall then transmit the echo cancellation sequence (*Notes 2* and *3*) as long as the sufficient degree of echo cancellation is not locally available.

(b) At the end of this sequence the DCE shall be silent during 25 ± 3 ms and then transmit the receiver synchronization signals followed by scrambled binary ZERO's.

(c) After detection of scrambled binary ZERO's, refinement of echo cancellation and detection of consecutively received scrambled binary ONE's (*Note 4*) during a period of 64 bits, the calling DCE shall apply the ON condition to circuit 109 and transmit scrambled binary ONE's during a fixed period of 128 bits.

(d) Then, the circuit 106 is enabled to respond to the condition of circuit 105 (*Notes 5* and *6*).

— Answer mode DCE

(a) The DCE transmits the echo cancellation sequence (*Note 2*) as long as the sufficient degree of echo cancellation is not available locally (*Note 3*).

(b) After this sequence, the DCE is silent during 25 ± 3 ms and then transmits the receiver synchronization signals followed by scrambled binary ZERO's.

(c) After detection of a signal transmitted by the calling DCE during a period of 50 ± 5 ms, the answering DCE keeps silent.

(d) After detection of 64 consecutively received scrambled binary ZERO's the DCE transmits the receiver synchronization signals followed by scrambled binary ZERO's.

(e) After refinement of echo cancellation and detection of 64 consecutively received scrambled binary ZERO's the DCE transmits scrambled binary ONE's.

(f) After detection of 64 consecutively received scrambled ONE's the DCE applies an ON condition to circuit 109 and enables circuit 106 to respond to the condition of circuit 105 (*Notes 5* and *6*).

Note 1: The echo cancellation sequence must not contain more than 32 consecutive unscrambled or scrambled binary ZERO's.

Note 2: When circuit 106 is in the OFF condition, circuit 103 shall be clamped to the binary ONE condition.

Note 3: If 4 consecutive error-free octets of the rate pattern are not detected, the DCE remains silent.

Note 4: Manufacturers are cautioned that the time duration of the echo cancellation sequence has to be at least 650 ms when operating with network echo cancellers in accordance with Recommendation G.165.

Note 5: The detection of scrambled binary ONE's or ZERO's should start only after the synchronization signals are completed.

Note 6: Users may wish to note that if in the DTE a timeout exists between the ON conditions of circuit 107 and circuit 106, this timeout shall be greater than 15 s.

4.4. Scrambler and descrambler

Each transmission direction uses a different scrambler. The way to allocate the scramblers/descramblers is described in item 4.3.6.1.

A self-synchronizing scrambler/descrambler shall be included in the DCE. According to the direction of transmission (see item 4.3.6.1.) the generating polynomial is:

$$GPC = 1 + X^{-18} + X^{-23}$$

or

$$GPA = (1 + X^{-5} + X^{-23}).$$

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence; and at the receiver the received polynomial, of which the received data sequence represents the coefficient in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described as follows.

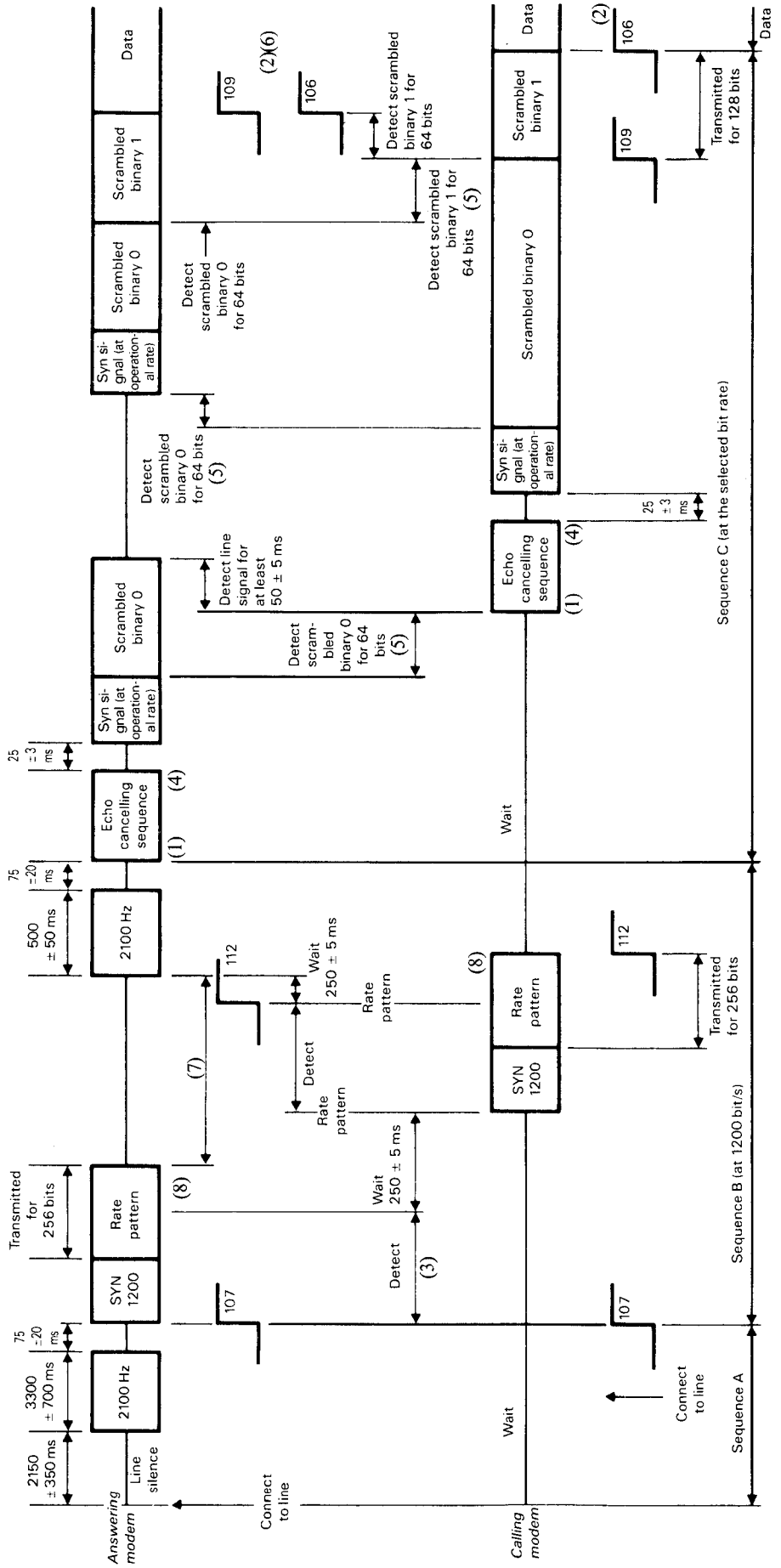


Figure 1. Operating sequences.

Notes:
(1) to (6): see Notes (1) to (6) in item 4.3.6.5.3.
(7) If 4 consecutive octets of rate pattern are not detected with in 2 seconds; the DCE resumes Sequence B.
(8) Rate pattern is defined in item 4.3.6.2.
(9) Sequence C is defined for operation at 2,400 bit/s and 1,200 bit/s and is under study for higher bit rate (4,800 bit/s).

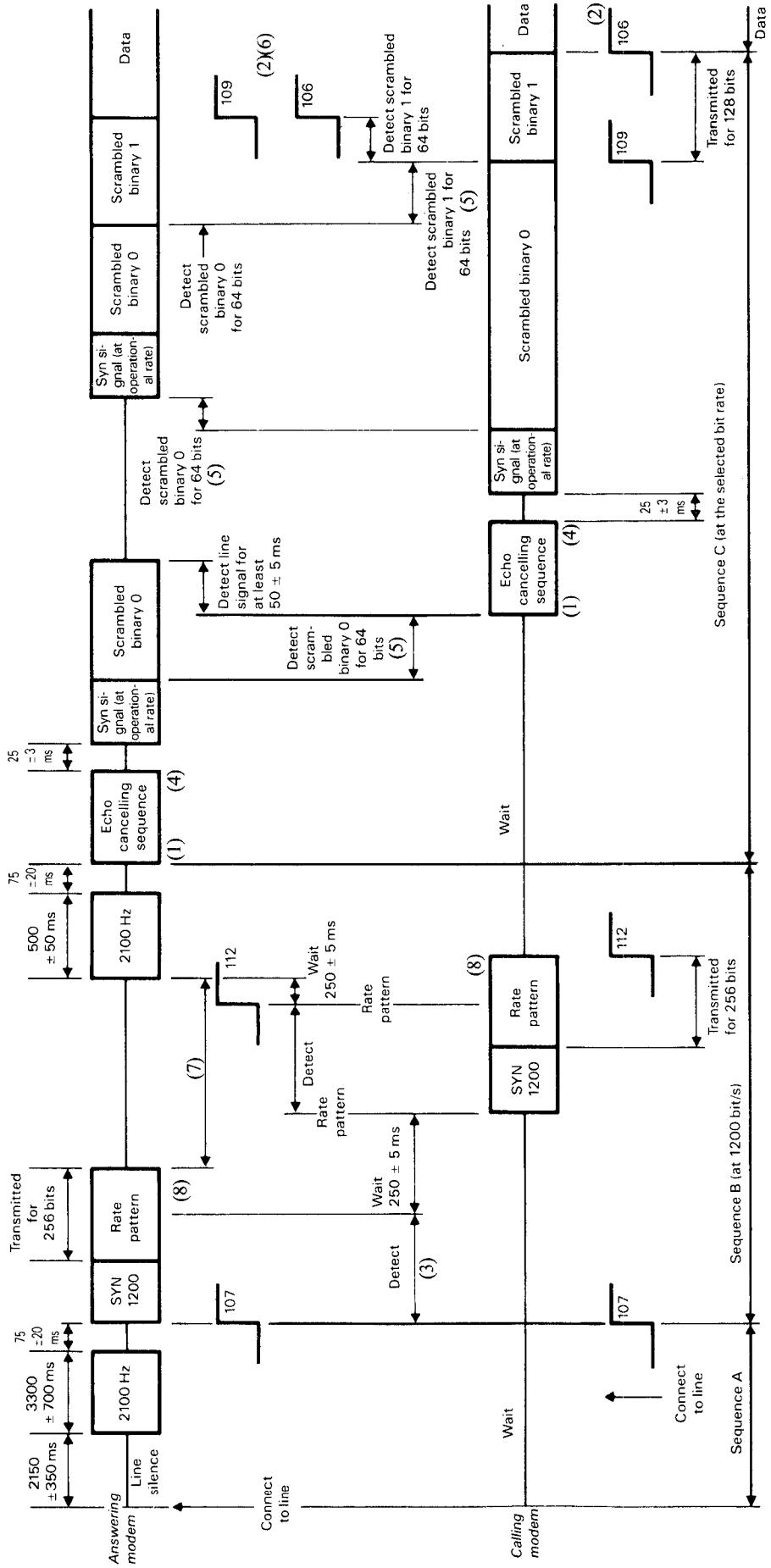


Figure 1. Operating sequences.

Notes:
(1) to (6): see Notes (1) to (6) in item 4.3.6.5.3.
(7) If 4 consecutive octets of rate pattern are not detected with in 2 seconds; the DCE resumes Sequence B.
(8) Rate pattern is defined in item 4.3.6.2.
(9) Sequence C is defined for operation at 2,400 bit/s and 1,200 bit/s and is under study for higher bit rate (4,800 bit/s).

4.4.1. *Scrambling*

The message polynomial is devided by the generating polynomial GPC = $1+X^{-18}+X^{-23}$ or GPA = $(1+X^{-5}+X^{-23})$, see Figures 2 and 3 respectively, according to the transmission direction. The coefficients of the quotient of this division taken in descending order form the data sequence D_s to be transmitted. The expression of this sequence is:

$D_s = D_i + D_s\, x^{-18} + D_s\, x^{-23}$ when the generating polynomial GPC is used,

$D_s = D_i + D_s\, x^{-5} + D_s\, x^{-23}$ when GPA is used.

D_i is the data sequence applied to the scrambler.

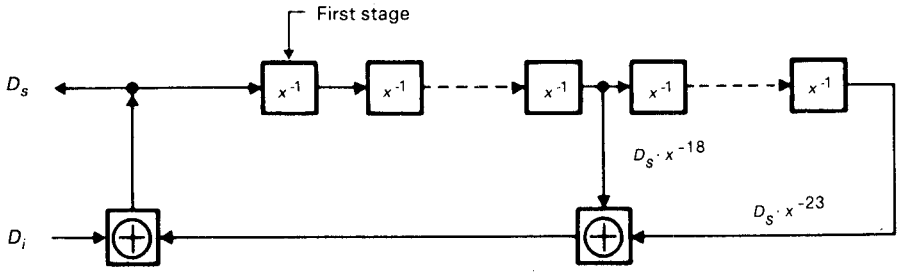


Figure 2. Scrambler with GPC generating polynomial.

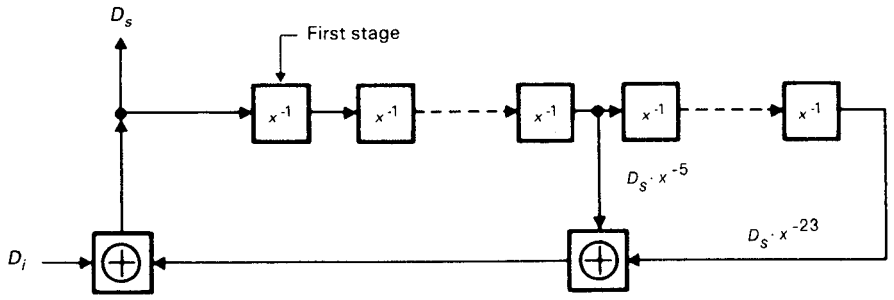


Figure 3. Scrambler with GPA generating polynomial.

Note: The scrambler output patterns required to produce signal segment 2 are as follows for both data rates:

GPC: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 00 01 11 00
↑
First Bit

GPA: 00 11 11 11 11 00 00 00 00 11 11 10 01 11 00 11 10 10 00
↑
First Bit

Scrambler contents immediately preceding the output above are as follows:

GPC: 10 01 11 11 11 11 11 11 00 00 01 1
↑

GPA: 01 10 00 00 11 10 00 00 11 10 00 0 1
↳
First stage of scrambler

4.4.2. *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial GPC or GPA (see Figures 4 and 5 respectively) to form the recovered message polynomial. The coefficients of the recovered polynomial taken in descending order form the output data sequence D_o with the expression:

$D_o = D_s\,(1+X^{-18}+X^{-23})$ for the GPC polynomial

where $D_o = D_s\,(1+X^{-5}+X^{-23})$ for the GPA polynomial.

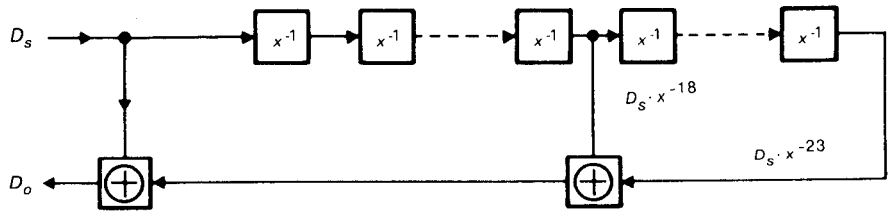


Figure 4. Descrambler with GPC polynomial.

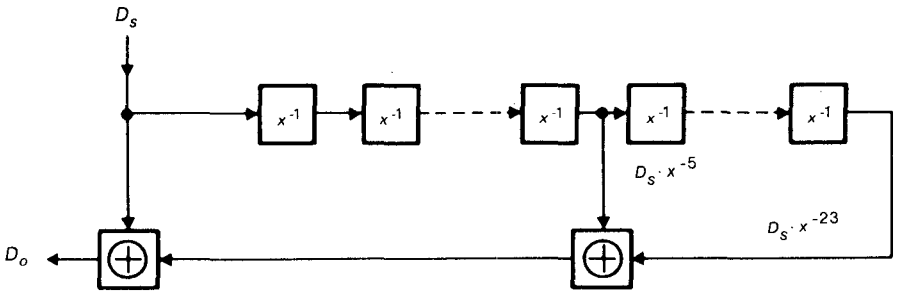


Figure 5. Descrambler with GPA polynomial.

4.5. **Line signal levels**

4.5.1. *Transmitter*

The power levels used will conform to Recommendation T/CD 01-01.

4.6. **Test facilities**

Remote loop 2

Instigation and termination of remote loop 2 shall be in accordance with Recommendation V.54.

5. REQUIREMENTS FOR ALTERNATIVE B2

5.1. **General**

5.1.1. The principal characteristics of the DCE are as follows:

(a) Full duplex operation on 2-wire GSTN circuits.
(b) Channel separation by frequency division.
(c) Quadrature amplitude modulation for each channel with synchronous line transmission at 600 baud (nominal).
(d) Inclusion of an adaptive equalizer and a compromise equalizer.
(e) Inclusion of a scrambler.
(f) Inclusion of test facilities.
(g) Data signalling rates of:
2,400 bit/s synchronous
1,200 bit/s synchronous.
(h) It is compatible with a modem conforming to Recommendation T/CD 01-10 operating at 1,200 bit/s signalling rate and includes automatic rate recognition.

5.2. **Data signalling rates**

The data rate transmitted to the line shall be 2,400 (1,200) bit/s $\pm$ 0.01% with a modulation rate of 600 baud $\pm$ 0.01%, and the DCE shall accept synchronous data at 2,400 (1,200) bit/s $\pm$ 0.01% under the control of circuit 113 or circuit 114.

Fallback signalling rate selection shall be either determined by the handshake procedure when interworking with a DCE conforming to Recommendation T/CD 01-10 or locally controlled via circuit 111.

5.3. **Interchange circuits**

5.3.1. *Circuit 106 and 109 response times*

After the handshake sequence circuit 106 will follow OFF-to-ON or ON-to-OFF transition of circuit 105 within 3.5 ms. The OFF-to-ON transition of circuit 109 is part of the handshake sequence specified in item 5.4.5.3. Circuit 109 shall turn OFF 40 to 65 ms after the level of the received signal appearing at the line terminal of the DCE falls below the relevant threshold defined in item 1.4.2. Following a dropout after the initial handshake, circuit 109 shall turn ON 40 to 65 ms after the level of the received signal appearing at the line terminal of the DCE exceeds the relevant threshold defined in item 1.4.2.

5.3.2. *Timing arrangement*

Clocks shall be included in the DCE to provide the data terminal equipment with transmitter element timing; transmitter element timing may be originated in the data terminal equipment and be transferred to the DCE via the appropriate interchange circuit, circuit 113.

5.4. **Modulation and coding**

The principal characteristics of this DCE are channel separation by frequency division and quadrature amplitude modulation for each channel with synchronous line transmission at 600 baud (nominal).

5.4.1. *Carrier and guard tone frequencies*

The carrier frequencies shall be 1,200 ± 0.5 Hz for the low channel and 2,400 ± 1 Hz for the high channel. A guard tone of 1,800 ± 1 Hz shall be transmitted at all times when the DCE is transmitting in the high channel. The guard tone shall not be transmitted when the DCE is transmitting the low channel.

5.4.2. *Line signal encoding*

5.4.2.1. 2,400 bits per second

The data stream to be transmitted shall be divided into groups of 4 consecutive bits (quadbits). The first and second bits of a quadbit shall be encoded as a phase change relative to the quadrant occupied by the preceding signal element (see Figure 7 and Table 7).

The second and fourth bits of each quadbit define one of 4 signalling elements associated with the new quadrant (see Figure 7). The left-hand bits in Table 7 and Figure 7 are the first of each pair in the data stream as it enters the modulator portion of the modem after the scrambler.

5.4.2.2. 1,200 bits per second

The data stream to be transmitted shall be divided into groups of 2 consecutive bits (dibits). The dibits shall be encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element (see Table 7). The signalling element corresponding to 01 in the signal constellation (Figure 7) shall be transmitted irrespective of the quadrant concerned. This ensures compatibility with a DCE conforming to Recommendation T/CD 01-10.

First two bits in quadbit (2,400 bit/s or dibit valus (1,200 bit/s)	Phase quadrant change	
00	1→2 2→3 3→4 4→1	90°
01	1→1 2→2 3→3 4→4	0°
11	1→4 2→1 3→2 4→3	270°
10	1→3 2→4 3→1 4→2	180°

Table 7. Line encoding.

5.4.3. *Spectrum and group delay characteristic*

The transmitted line signals, excluding the characteristics of the fixed compromise equalizer, shall have a frequency amplitude spectrum equivalent to the square root of raised cosine shaping with 75% roll-off and within the limits shown in Figure 6. Similarly, the group delay of the transmitter output shall be within the range of ± 100 μs, over the frequency ranges 900-1,500 Hz (low channel) and 2,100-2,700 Hz (high channel). These figures are provisional.

5.4.4. *Fixed compromised equalizer*

Fixed compromise equalization shall be incorporated in the DCE transmitter to render the DCE compatible with a DCE conforming to Recommendation T/CD 01-10.

5.4.5. *Operating sequences*

5.4.5.1. Channel allocation

On the General switched telephone network (GSTN), the DCE at the calling data station shall transmit in the low channel and receive in the high channel (call mode). The DCE at the answering data station shall receive in the low channel and transmit in the high channel (answer mode).

Note: Where calls are established on the GSTN by operators, bilateral agreement between users on channel allocation will be necessary.

5.4.5.2. V.25 Automatic answering sequence

The V.25 Auto-answering sequence shall be transmitted from the Answer mode modem on international GSTN connections. The transmission of the sequence may be omitted on national connections on the GSTN, where permitted by the administrations.

5.4.5.3. Handshake sequence on GSTN

The means of achieving synchronism between the calling DCE and the answering DCE on international GSTN connections is shown in Figures 8, 9 and 10. If both calling and answering DCE's are V.22*bis*-DCE's, the handshake will normally condition both DCE's to operate at 2,400 bit/s. If, however, one or both of the DCE's has been set to operate at 1,200 bit/s, either manually or via circuit 111, then the handshake will condition both DCE's to operate at 1,200 bit/s. If either the calling or answering DCE is a DCE conforming to Recommendation T/CD 01-10, the handshake will condition both the V.22*bis*-DCE and the Recommendation T/CD 01-10-DCE to operate at 1,200 bit/s. The signalling rate is communicated to the DTE by a logical condition on circuit 112. The handshake sequence is independent of whether the calling or answering DCE is connected to line first.

5.4.5.3.1. Interworking at 2,400 bit/s

5.4.5.3.1.1. Call-mode DCE

(a) On connection to line the call-mode DCE shall be conditioned to receive signals in the high channel at 1,200 bit/s and transmit signals in the low channel at 1,200 bit/s in accordance with item 5.4.2.2. It shall apply an ON condition to circuit 107 in accordance with Recommendation T/CD 01-01. The DCE shall initially remain silent.

(b) On receipt of unscrambled binary 1 at 1,200 bit/s at level within the range -5 dBm to -48 dBm, and for a continuous duration of 155 ± 10 ms, the DCE shall wait for a period of 456 ± 10 ms, and shall then transmit unscrambled repetitive double dibit pattern of 00 and 11. The signal shall be transmitted for a period of 100 ± 3 ms immediately after which scrambled binary 1 shall be transmitted continuously at 1,200 bit/s.

(c) If the DCE detects scrambled binary 1 in the high channel at 1,200 bit/s for 270 ± 40 ms, the handshake shall continue in accordance with item 5.4.5.3.2.1.(c) and (d). However, if unscrambled repetitive double dibit 00 and 11 at 1,200 bit/s is detected in the high channel then at the end of receipt of this signal the DCE shall apply an ON condition to circuit 112.

(d) 600 ± 10 ms after circuit 112 has been turned ON the DCE shall begin transmitting scrambled binary 1 at 2,400 bit/s, and 450 ± 10 ms after circuit 112 has been turned ON the receiver may begin making 16 way decisions.

(e) Following transmission of scrambled binary 1 at 2,400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the DCE shall be ready to transmit data at 2,400 bit/s.

(f) When 32 consecutive bits of scrambled binary 1 at 2,400 bit/s have been detected in the high channel, the DCE shall be ready to receive data at 2,400 bit/s and shall apply an ON condition to circutranit 109.

5.4.5.3.1.2. Answer-mode DCE

(a) On connection to line the answer-mode DCE shall be conditioned to transmit signals in the high channel at 1,200 bit/s and receive signals in the low channel at 1,200 bit/s in accordance with item 5.4.2.2. Following transmission of the answer sequence in accordance with Recommendation T/CD 01-01. The DCE shall apply an ON condition to circuit 107 and then transmit unscrambled binary 1 at 1,200 bit/s.

(b) If the DCE detects scrambled binary 1 or 0 in the low channel at 1,200 bit/s for 270 ± 40 ms, the handshake shall continue in accordance with items 5.4.5.3.2.2.(b) and (c). However, if unscrambled repetitive double dibit 00 and 11 at 1,200 bit/s is detected in the low channel, at the end of receipt of this signal the DCE shall apply an ON condition to circuit 112 and then transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1,200 bit/s for 100 ± 3 ms. Following these signals the DCE shall transmit scrambled binary 1 at 1,200 bit/s.

(c) 600 ± 10 ms after circuit 112 has been turned ON the DCE shall begin transmitting scrambled binary 1 at 2,400 bit/s, and 450 ± 10 ms after circuit 112 has been turned ON the receiver may begin making 16 way decisions.

(d) Following transmission of scrambled binary 1 at 2,400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the DCE shall be ready to transmit data at 2,400 bit/s.

(e) When 32 consecutive bits of scrambled binary 1 at 2,400 bit/s have been detected in the low channel the DCE shall be ready to receive data at 2,400 bit/s and shall apply an ON condition to circuit 109.

5.4.5.3.2. Interworking at 1,200 bit/s

This handshake is identical to the handshake sequence in Recommendation T/CD 01-10.

5.4.5.3.2.1. Call-mode DCE

(a) On connection to line the call-mode DCE shall be conditioned to receive signals in the high channel at 1,200 bit/s and transmit signals in the low channel at 1,200 bit/s. It shall apply an ON condition to circuit 107 in accordance with Recommendation T/CD 01-01. The DCE shall initially remain silent.

(b) After 155 ± 10 ms of unscrambled binary 1 has been detected the DCE shall remain silent for further 456 ± 10 ms then transmit scrambled binary 1 at 1,200 bit/s (a preceding V.22*bis* signal, as shown in Figure 8, would not affect the operation of a Recommendation T/CD 01-10 answering DCE).

(c) On detection of scrambled binary 1 in the high channel at 1,200 bit/s for 270 ± 40 ms the DCE shall be ready to receive data at 1,200 bit/s and shall apply an ON condition to circuit 109 and OFF condition to circuit 112.

(d) 765 ± 10 ms after circuit 109 has been turned ON, circuit 106 shall be conditioned to respond to circuit 105 and the DCE shall be ready to transmit data at 1,200 bit/s.

5.4.5.3.2.2. Answer-mode DCE

(a) On connection to line the answer-mode DCE shall be conditioned to transmit signals in the high channel at 1,200 bit/s and receive signals in the low channel at 1,200 bit/s. Following transmission of the answer sequence in accordance with Recommendation T/CD 01-01, the DCE shall apply an ON condition to circuit 107 and then transmit unscrambled binary 1 at 1,200 bit/s.

(b) On detection of scrambled binary 1 or 0 in the low channel at 1,200 bit/s for 270 ± 40 ms, the DCE shall apply an OFF condition to circuit 112 and shall then transmit scrambled binary 1 at 1,200 bit/s.

(c) After scrambled binary 1 has been transmitted at 1,200 bit/s for 765 ± 10 ms, the DCE shall be ready to transmit and receive data at 1,200 bit/s, shall condition circuit 106 to respond to circuit 105 and shall apply an ON condition to circuit 109.

5.4.5.4. Retrain sequence (2,400 bit/s operation)

A retrain may be initiated during data transmission between two DCE's conforming to CCITT Recommendation V.22*bis* if either DCE incorporates a means of detecting loss of equalization.

Transmission of a retrain sequence shall be initiated either by detection of loss of equalization or by detection of unscrambled repetitive double dibit 00 and 11 at 1,200 bit/s from the distant DCE.

The following sequence of events shall take place during the retrain:

(a) Following detection of loss of equalization or the end of detection of unscrambled repetitive double dibit 00 and 11 at 1,200 bit/s from the distant DCE OFF conditions shall be applied to circuits 106 and 109, and the DCE shall transmit an unscrambled repetitive double dibit pattern of 00 and 11 at 1,200 bit/s for 100 ± 3 ms. Following this signal the DCE shall transmit scrambled binary 1 at 1,200 bit/s.

(b) 600 ± 10 ms after the end of detection of unscrambled repetitive double dibit 00 and 11 at 1,200 bit/s from the distant DCE, the DCE shall begin transmitting scrambled binary 1 at 2,400 bit/s, and 450 ± 10 ms after the end of this detection the receiver may begin 16 way decisions.

(c) Following transmission of scrambled binary 1 at 2,400 bit/s for 200 ± 10 ms, circuit 106 shall be conditioned to respond to circuit 105 and the DCE shall be ready to transmit data at 2,400 bit/s.

(d) When 32 consecutive bits of scrambled binary 1 at 2,400 bit/s have been detected from the remote DCE, the DCE shall be ready to receive data at 2,400 bit/s and shall apply an ON condition to circuit 109.

A retrain between two DCE's is shown in Figure 11. Clocks presented on circuits 114 and 115 shall remain 2,400 bit/s during the entire retrain sequence.

If a DCE has transmitted a retrain signal and has not received unscrambled repetitive double dibit 00 and 11 at 1,200 bit/s immediately prior, during, or within a time interval equal to the maximum expected 2-way propagation delay, the DCE shall return to the beginning of the retrain signal as defined above and repeat the procedure until unscrambled repetitive double dibit 00 and 11 is received from the remove DCE. A time interval of 1.2 seconds is recommended for the maximum expected 2-way propagation delay.

If the DCE fails to synchronize on the received retrain sequence, the DCE shall transmit another retrain signal.

5.4.5.5. Operation after loss of line signal

When the DCE detects loss received line signal (as specified in items 1.4.2. and 5.3.1.) it shall turn off circuit 109 and shall clamp circuit 104 to binary 1. If received line signal is then detected (as specified in items 1.4.2. and 5.3.1.), the DCE shall turn on circuit 109 but shall leave 104 circuit clamped to binary 1. If during the next 100 ms the DCE detects a retrain sequence it shall proceed according to 5.4.5.4. above. If the DCE has not detected a retrain sequence by the end of the same 100 ms, it shall remove clamp from circuit 104. If at any time after turning on circuit 109, following a drop out, the DCE detects loss of equalization, it shall proceed according to item 5.4.5.4. above.

5.4.5.6. Fallback from 2,400 bit/s to 1,200 bit/s working

Will be specified later.

5.5. Scrambler and descrambler

5.5.1. *Scrambler*

A self-synchronizing scrambler having the generating polynomial $1+X^{-14}+X^{-17}$ shall be included in the DCE transmitter. The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler output data sequence

$D_s = D_i + D_s \cdot X^{-14} + D_s \cdot X^{-17}$

where D_s = the data sequence at the output of the scrambler

D_i = the data sequence applied to the scrambler

$+$ = denotes modulo 2 addition

$\cdot$ = denotes binary multiplication

Figure 12 shows a suitable implementation.

In addition, a sequence of 64 consecutive binary 1's at the scrambler output (D_s) shall cause the next bit input to the scrambler (D_i) to be inverted. This inversion shall not occur during the handshaking sequence or during the instigation of remote loop 2.

5.5.2. *Descrambler*

A self-synchronizing descrambler having the polynomial $1+X^{-14}+X^{-17}$ shall be provided in the DCE receiver. The message data sequence produced after demodulation shall be effectively multiplied by the generating polynomial $1+X^{-14}+X^{-17}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by:

$D_o = D_s\,(1+X^{-14}+X^{-17})$

where the notation is as defined in item 5.5.1.

Circuitry may be included to detect a sequence of 64 consecutive 1's at the input to the descrambler (D_s) and, if detected, invert the next output from the descrambler (D_o). This detector should not begin operating until the handshaking sequence is complete. Detection of the initiation signal described in item 5.1.1. (unscrambled binary 1's) should be performed at the point (D_o).

Figure 13 shows a suitable implementation.

5.6. Line signal levels

5.6.1. *Transmitter*

The 1,800 Hz guard tone shall be at a level of 6 ± 1 dB below the level of the data power in the high channel. The total power transmitted to line shall be the same for transmission in either channel. Because of the 1,800 Hz guard tone, the power level of data signals in the high channel will be approximately 1 dB lower than data signals in the low channel.

5.6.2. *Receiver*

Circuit 109 (I) shall not respond to the 1,800 Hz guard tone, the 550 Hz optional guard tone specified in T/CD 01-10 or the 2,100 Hz (nominal) answer tone during the handshake sequence.

5.7. Test facilities

5.7.1. *Instigation of remote loop 2*

Signals controlling the application of remote loop 2 may only be transmitted after the synchronizing handshake has been completed.

As in specification T/CD 01-01, the DCE's are referred to as DCE A and DCE B.

When DCE A is instructed to instigate remote loop 2, the DCE shall transmit an initiation signal of unscrambled binary 1. DCE B shall detect 154-231 ms of the initiation signal, and the transmit to DCE A scrambled alternate binary 1 s and 0 s (reversals) at 2,400 (1,200) bit/s.

DCE A shall detect 231-308 ms of scrambled reversals, cease transmission of the initiation signal, and then transmit scrambled binary 1 at 2,400 (1,200) bit/s.

DCE B shall detect the loss of initiation signal and activate loop 2 within DCE B.

DCE A, upon receiving 231-308 ms of scrambled binary 1, shall indicate to the DTE that it may begin sending test messages.

5.7.2. *Termination of remote loop 2*

When DCE A is instructed to terminate a remote loop 2, the line signal shall be suppressed for a period of 77 ± 10 ms, after which transmission shall be restored.

DCE B detects the loss of line signal in 17 ± 7 ms and detects the re-appearance of the signal within 155 ± 50 ms, after which it returns to normal operation.

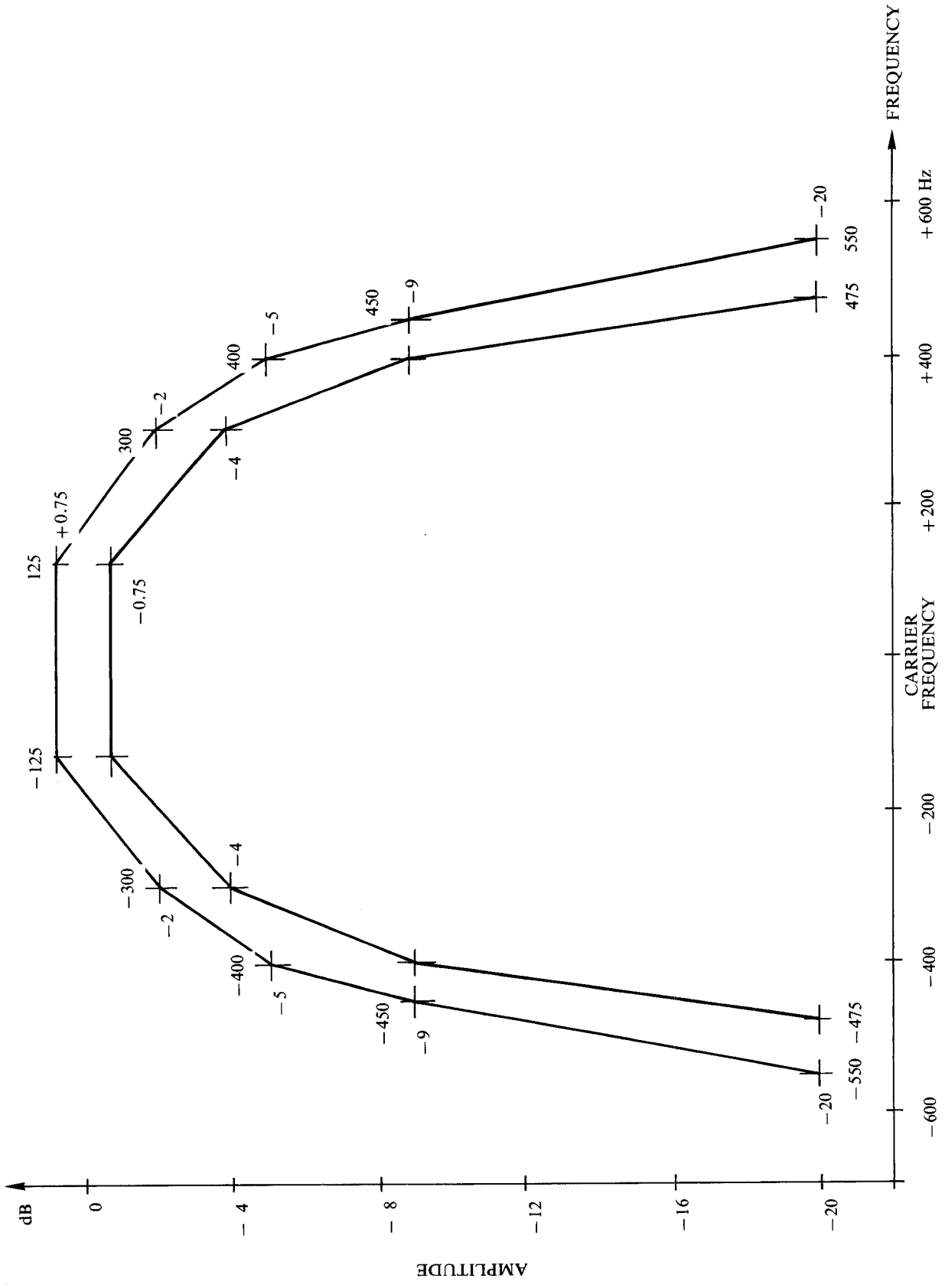


Figure 6. Amplitude limits for transmitted line signal (unequalized).

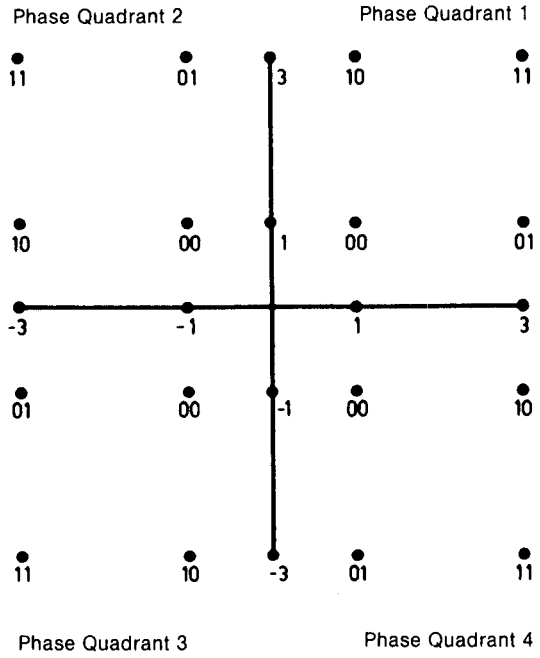
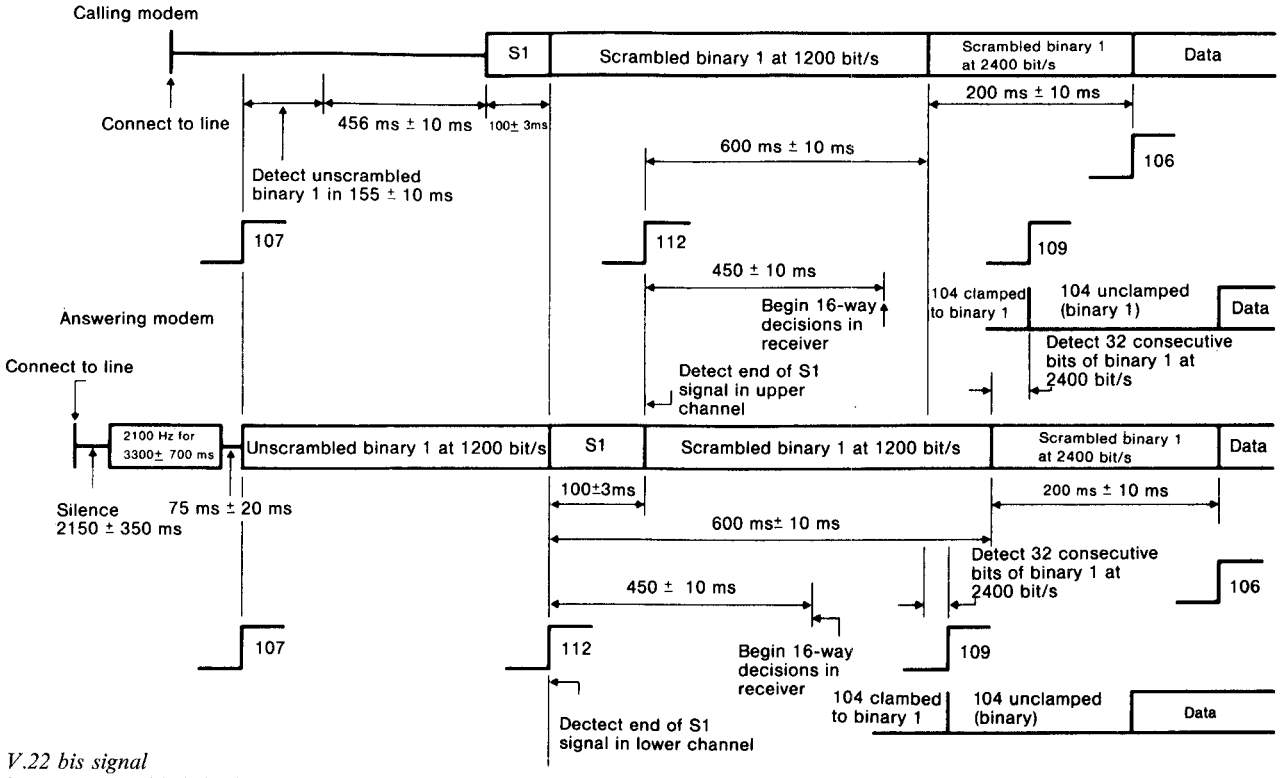


Figure 7. Signal constellation.



V.22 bis signal

S1 = Unscrambled double dibit 00 and 11 at 1,200 bit/s for 100 ms+3 ms.

Figure 8. Handshake sequence at 2,400 (with V.25 auto-answering).

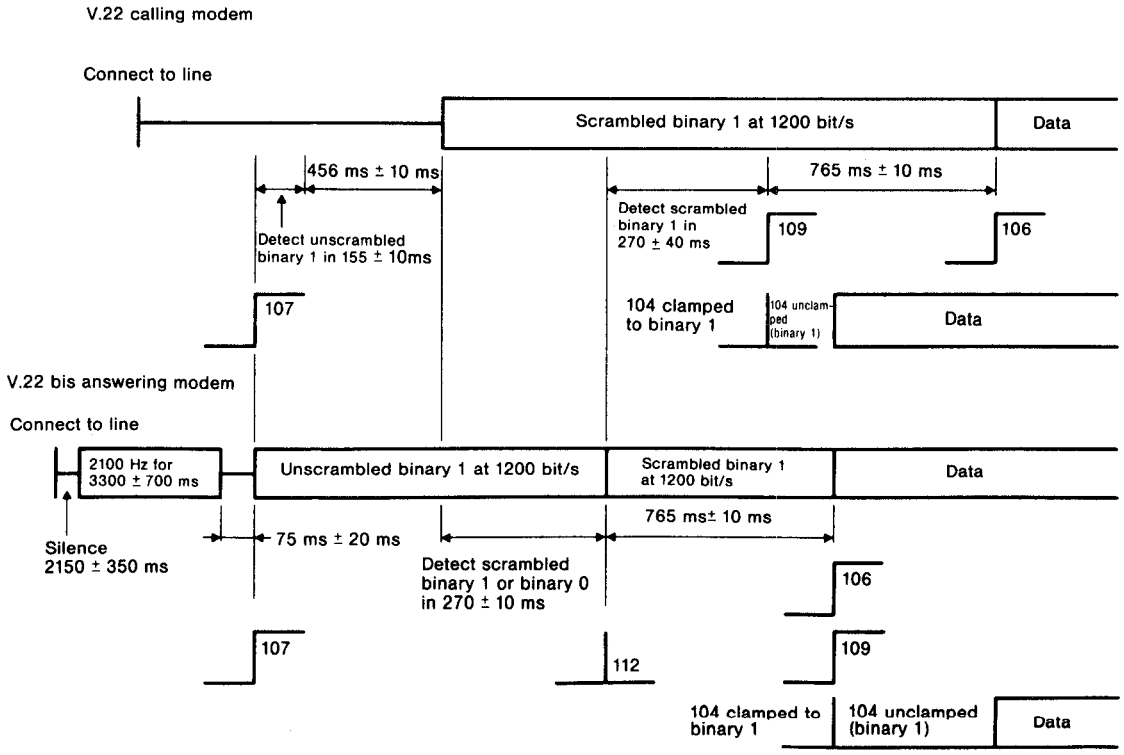
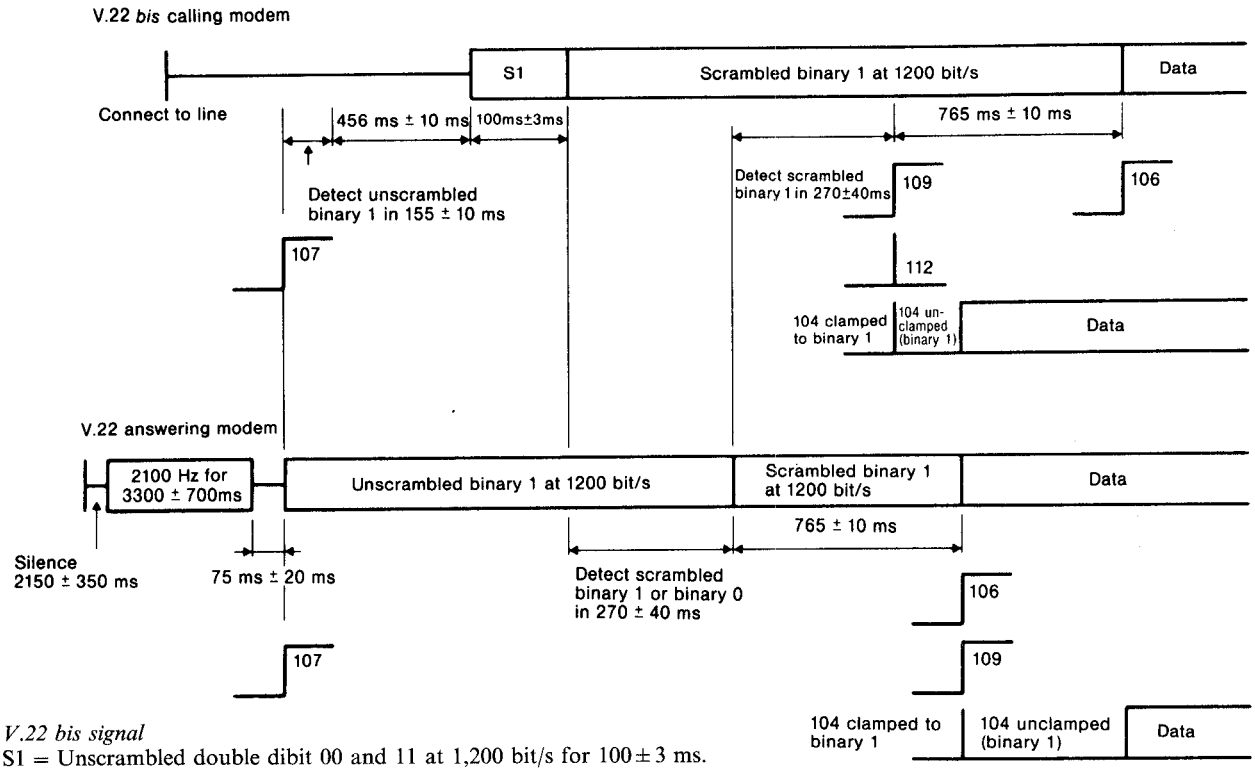
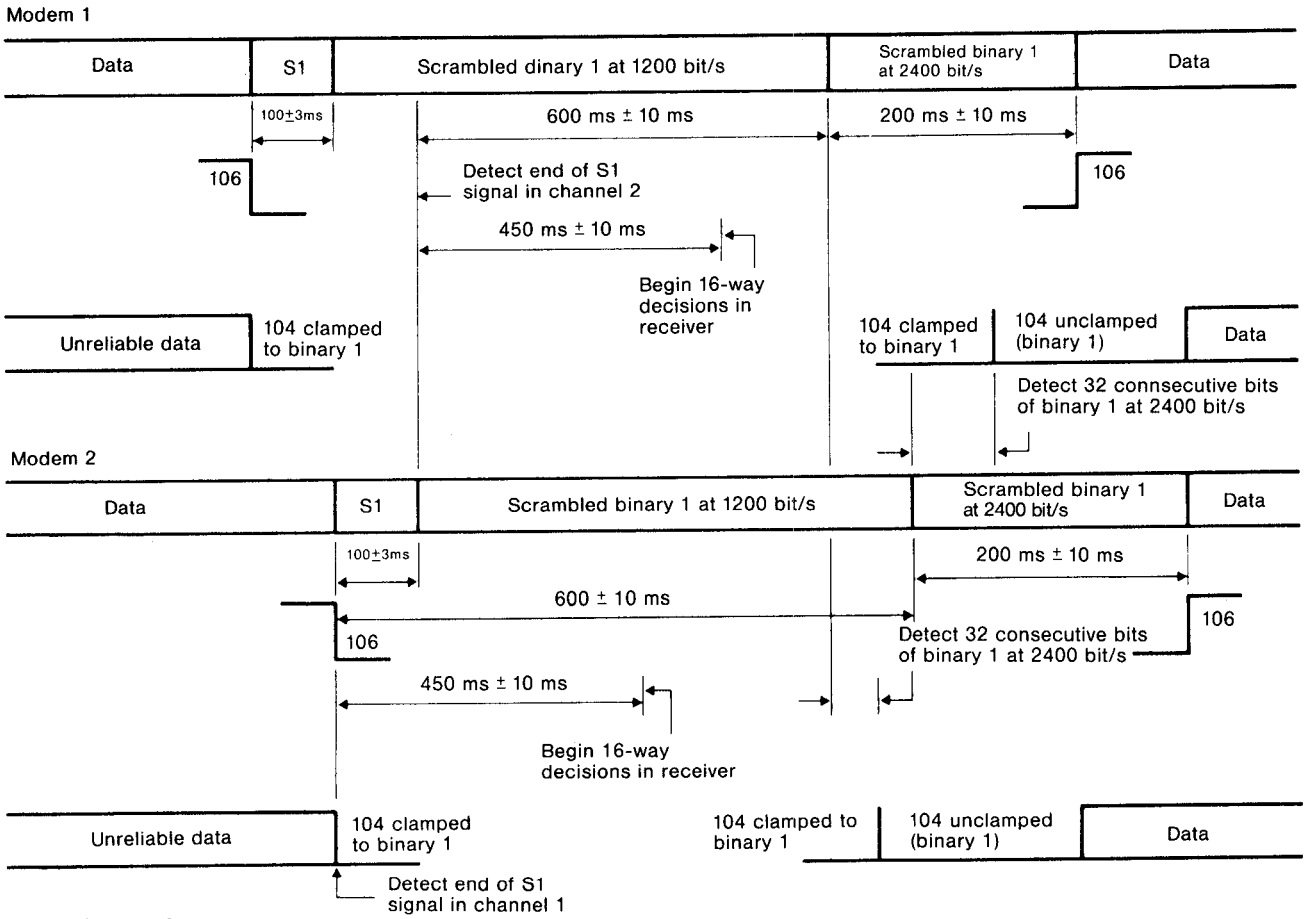


Figure 9. Handshake sequence at 1,200 bit/s with V.22 calling modem (with V.25 auto-answering).



V.22 bis signal
S1 = Unscrambled double dibit 00 and 11 at 1,200 bit/s for 100 ± 3 ms.

Figure 10. Handshake sequence at 1,200 bit/s with V.22 answering modem (with V.25 auto-answering).



V.22 bis signal
S1 = Unscrambled double dibit 00 and 11 at 1,200 bit/s for 100 ± 3 ms.

Figure 11. A retrain at 2,400 bit/s.

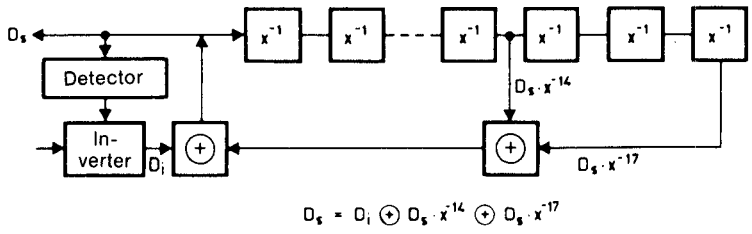


Figure 12. Scrambler.

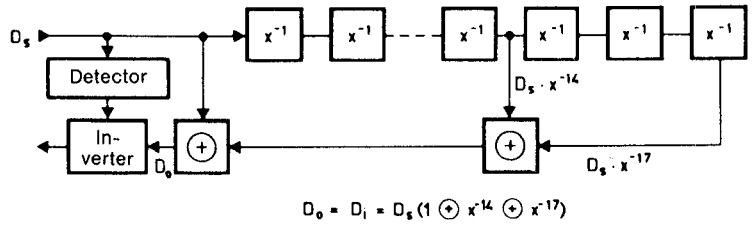


Figure 13. Descrambler.

Note: Marks (binary 1) and spaces (binary 0) at the interface correspond to ones and zeros respectively in these logic diagrams.

6. TEST LOOPS

6.1. Test loops for alternative A: 2,400 bit/s hdx DCE

To assist testing of the DTE, test loop 3 as defined in Recommendation T/CD 01-01 shall be provided in the DCE. The loop is automatically activated (circuit 141), locally controlled.

6.2. Test loops for alternative B: 2,400 bit/s dx DCE

To assist testing of the DTE, test loop 3 as defined in Recommendation T/CD 01-01 shall be provided in the DCE. The loop is automatically activated (circuit 141), locally controlled.

For network maintenance purposes a loop 2 as defined in Recommendation T/CD 01-01 shall be implemented in the DCE.

The loop is automatically activated (circuit 140), remotely controlled.

7. POWER CONSUMPTION

See Part I, Section A, item 5.

8. CONSTRUCTION

See Part I, Section A, item 6.

9. ENVIRONMENTAL REQUIREMENTS

See Part I, Section A, item 7.

2.3.3. *State 7 – Dial-out number*

When the DTE transmits a request-to-dial (RD) character 4/3 ("C") via circuit 103, the DCE shall enter this state by responding with an acknowledge character (ACK) 4/9 ("I") via circuit 104.

The DCE shall then seize the line and wait for dial tone.

An option shall be provided so that if dial tone has not been positively identified by the end of either 4.5 ± 0.5 seconds or 9.5 ± 0.5 seconds, then at the end of the appropriate period the DCE shall immediately dial the stored number. Following completion of dialling, the DCE shall enter state 8.

If the request-to-dial (RD) character 4/3 ("C") is transmitted to the DCE while the program-in-number memory is empty, the DCE shall abort the call set-up procedure, send a negative acknowledge (NACK) character 4/6 ("F") to the DTE and revert to state 5.

2.3.4. *State 8 – Transmit call tone*

2.25 ± 0.25 seconds after entering this state, the DCE shall transmit to line a $1{,}200 \pm 1$ Hz tone.

The calling tone shall be pulsed ON and OFF with an ON period of 0.6 ± 0.1 seconds and an OFF period of 3.75 ± 0.25 seconds. When ring-tone is detected in accordance with item 2.3.5., the OFF period of the calling tone shall be reduced to 1.75 ± 0.25 seconds.

When the calling tone is OFF, the DCE shall change to state 9, and when ON shall revert to state 8.

If an abort call (ABC) character 4/1 ("A") is received from the DTE while in this state, the DCE shall respond by disconnecting from line, transmitting an acknowledge (ACK) character 4/9 ("I") 3 seconds after disconnecting from line and reverting to state 5.

2.3.5. *State 9 – Await reply*

During pauses (3.75 ± 0.25 seconds) in transmitting the calling tone, the DCE shall enter this state and monitor the line for receipt of any signal. If ring tone is detected, the DCE shall send a ring-tone detected (RTD) character 5/2 ("R") to the DTE immediately before re-entering state 8.

If an engaged tone is detected, the DCE shall respond by disconnecting from line, sending an engaged-tone (ENG) character 4/5 ("E") to the DTE 3 seconds after disconnecting from line before reverting to state 5. Equipment busy or number unobtainable shall be similarly signalled to the DTE by means of an equipment-busy (EQB) character 4/2 ("B") or number-unobtainable (NU) character 5/5 ("U") 3 seconds after disconnecting from line prior to the DCE reverting to state 5. In an abort-call (ABC) character 4/1 ("A") is received from the DTE while in this state, the DCE shall respond by disconnecting from line, transmitting an acknowledge (ACK) character 4/9 ("I") 3 seconds after disconnecting from line and reverting to state 5.

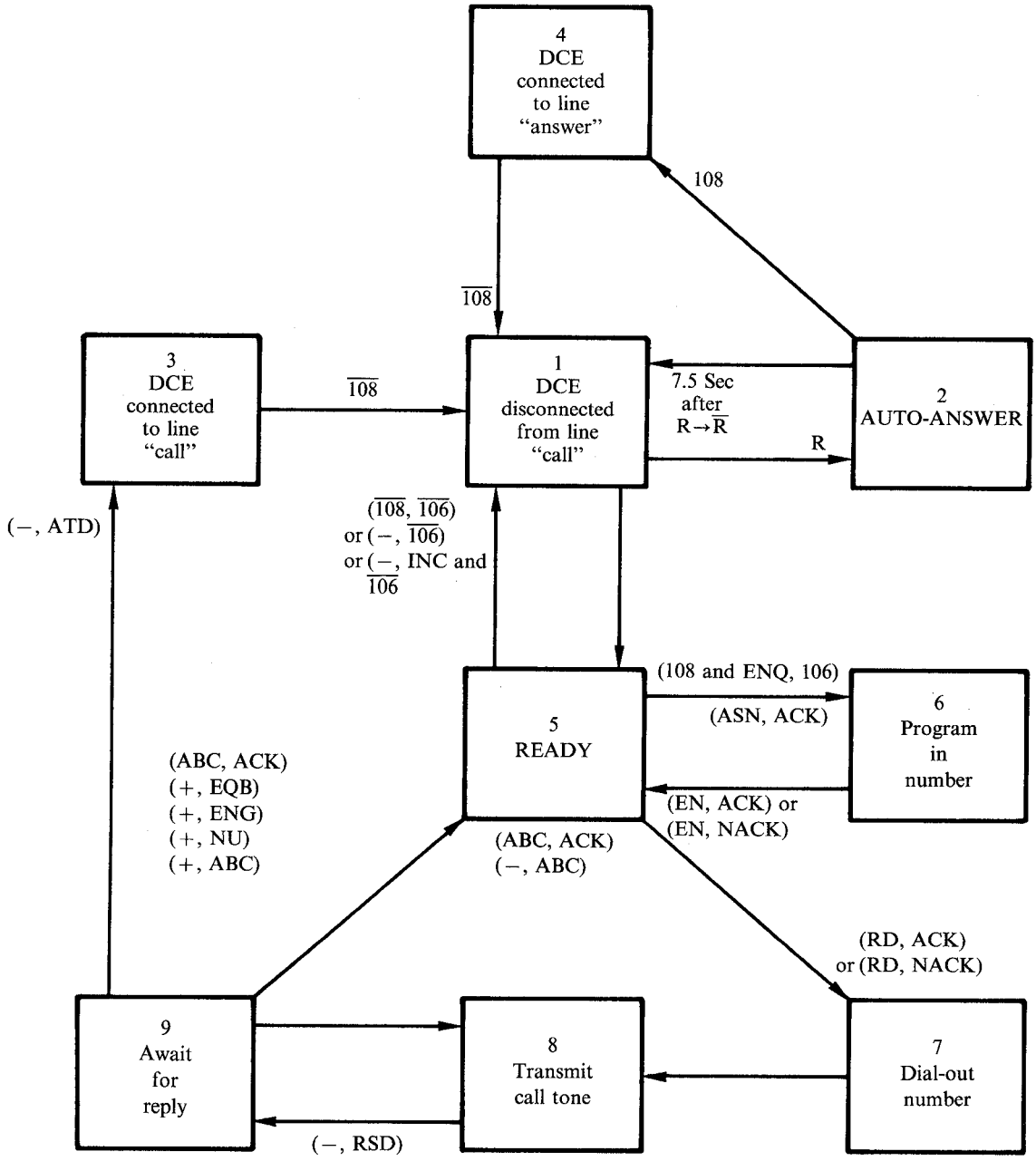
If the V.25 answer tone is detected, the DCE shall send an answer-tone-detected (ATD) character 4/8 ("H") to the DTE and enter state 3.

If a ring tone has not been received after a period of 50 seconds following the DCE entering state 9 from state 8, or if V.25 answer tone has not been received after a period of 14 seconds following receipt of ring tone, the DCE shall abort the call by disconnecting from line, sending an abort-call (ABC) character 4/1 ("A") to the DTE 3 seconds after disconnecting from line and reverting to state 5.

An option shall be provided so that if number-unobtainable or equipment-busy tone is received following the first attempt to establish a call, the DCE shall attempt to redial the number three more times by reverting to state 5 and repeating the procedure outlined in items 2.3.3., 2.3.4. and 2.3.5. above.

Symbol	Description	DCE-DTE	DTE-DCE	IA5 charac.	Binary repres.	EBCDIC repres.	Binary repres.
ABC	Abort call		X	A	0100 0001	A	1100 0001
ACK	Acknowledge	X		I	0100 1001	I	1100 1001
ASN	About-to-send number		X	D	0100 0100	D	1100 0100
ATD	Answer tone detected	X		H	0100 1000	H	1100 1000
EN	End of number		X	#	0010 0011	t	1010 0011
ENG	Engaged tone detected	X		E	0100 0101	E	1100 0101
ENQ	Enquiry		X	G	0100 0111	G	1100 0111
EQB	Equipment busy	X		B	0100 0010	B	1100 0010
INC	Incoming call	X		T	0101 0100	M	1101 0100
NACK	Negative acknowledge	X		F	0100 0110	F	1100 0110
NU	Number unobtainable	X		U	0101 0101	N	1101 0101
PAU	Pause		X	"	0010 0010	s	1010 0010
RTD	Ring tone detected	X		R	0101 0010	K	1101 0010
RD	Request to dial		X	C	0100 0011	C	1100 0011
SYN	Synchronization	X	X	SYN	0001 0110	o	1001 0110
1			X	1	0011 0001	1	1111 0001
2			X	2	0011 0010	2	1111 0010
3			X	3	0011 0011	3	1111 0011
4			X	4	0011 0100	4	1111 0100
5			X	5	0011 0101	5	1111 0101
6			X	6	0011 0110	6	1111 0110
7			X	7	0011 0111	7	1111 0111
8			X	8	0011 1000	8	1111 1000
9			X	9	0011 1001	9	1111 1001
0			X	0	0011 0000	0	1111 0000

Table 8.



In the representation (A, B)

A Denotes character from the DTE to the DCE.
B Denotes character from the DCE to the DTE.
R Ringing.

SYN	SYN	COMMAND

Figure 14(a).

SYN	SYN	NUMBER	EN

Figure 14(b).

Section C

1. GENERAL

This section specifies optional requirements which may be included in a plug-in DCE.

2. OPTIONAL MODES OF OPERATION

The DCE may be configured for the following additional modes of operation:

Mode i) 2,400 bit/s start-stop, 8, 9, 10 or 11 bits per character,

Mode ii) 1,200 bit/s start-stop, 8, 9, 10 or 11 bits per character.

2.1. Transmitter

The DCE shall accept a data stream of start-stop characters from the DTE at a nominal rate of 2,400 or 1,200 bit/s. The start-stop data shall be converted to a form suitable for transmitting synchronously at 2,400 or 1,200 bit/s ±0.01%, scrambled and then passed to the modulator for encoding. The DCE shall derive its line signal clock from internal clock source or, alternatively, from received signal element timing.

It shall be possible to condition the converter to accept the following character formats, viz:

(a) a one-unit start element, followed by 7 data units, and a stop element of one unit in length (9 bit characters),

(b) a one-unit start element, followed by 8 data units, and a stop element of one unit in length (10 bit characters),

(c) a one-unit start element, followed by 9 data units, and a stop element of one unit in length (11 bit characters).

The converter may also accept characters consisting of

(d) a one-unit start element, followed by 6 data units, and a stop element of one unit in length (8 bit characters).

Note that character formats (c) and (d) do not conform to International alphabet No. 5.

The character format selected shall be the same for both transmitter and receiver. The characters shall be in accordance with Recommendation V.4 regardless whether they are conformable with International alphabet No. 5 or not. It shall be possible to transmit characters contiguously or with any additional continuous stop element of arbitrary length between characters.

Note: In each of the four formats, data units can be replaced by additional stop units.

For example, format (c) will allow 11 bit characters consisting of a one-unit start element, followed by 8 data units and a stop element of 2 units to be handled.

2.1.1. *Signalling rate range*

The intracharacter signalling rate (signalling rate of the start bit and information bits within each character) provided by the DTE on circuit 103 must be 2,400 or 1,200 bit/s ±1%, −2.5%. In mode i), the character rate (the reciprocal of the time interval between successive start bits) provided by the DTE over circuit 103 must not exceed.

303 characters per second for 8-bit characters
269.3 characters per second for 9-bit characters
242.4 characters per second for 10-bit characters
220.3 characters per second for 11-bit characters

the start-stop to synchronous converter in the DCE transmitter shall as often as necessary delete the stop bits of the incoming characters in order to attain the nominal transmission rate. No more than one stop bit shall be deleted for any 8 consecutive characters.

When the character rate provided by the DTE on circuit 103 is less than

300 characters per second for 8-bit characters
266.6 characters per second for 9-bit characters
240 characters per second for 10-bit characters
218.2 characters per second for 11-bit characters

the start-stop to sychronous converter in the DCE is transmitting more bits per second than are provided by the DTE. The converter shall therefore insert extra stop bits in between the transmitted characters.

In mode ii) the character rates are half those of mode i).

2.1.2. *Extended signalling rate range*

Certain DTE's and multiplexers are not within the +1% overspeed limit. Facilities may therefore be provided to enable the DCE to accept data from a DTE having an intracharacter signalling rate of 2,400 or 1,200 bit/s +2.3%, −2.5%, with 8, 9, 10 or 11 bits per character by deletion of up to one stop bit in any four consecutive characters. A DCE transmitter set to work with 2.3% maximum overspeed can handle data received from a DTE in accordance with item 2.1.1.

2.1.3. *Break signal*

If the converter detects M to 2 M+3 bits all of "start" polarity, where M is the number of bits per character in the selected format, the converter shall transmit 2 M+3 bits of "start" polarity. If the converter detects more than 2 M+3 bits all of "start" polarity, the converter shall transmit all these bits as "start" polarity.

Note: The DTE must transmit on circuit 103 at least 2 M bits of "stop" polarity after the "start" polarity-break signal before sending further data characters. This ensures that the receiving DCE can regain character synchronism.

2.2. **Receiver**

The intracharacter signalling rate provided to the DTE over circuit 104 shall be in the range 2,400 to 2,455 bit/s for the mode i), in the range 1,200 to 1,227 bit/s for the mode ii). The nominal length of the start and data elements of all characters shall be the same. The length of the stop element shall not be reduced by more than 12% for the basic signalling rate range (or 25% for the optional extended signalling-rate range) to allow for overspeed in the transmitting terminal.

The use of the basic signalling-rate range is preferred since it results in lower distortion. The choice of range shall be made at time of installation, and shall be the same for both transmitter and receiver. It is not intended to be under customer control.

2.2.1. *Break signal*

The 2 M+3 or more bits of "start" polarity received from the transmitting DCE shall be put out on circuit 104. The DCE shall then regain character synchronism from the following "stop"-to-"start" transition.

3. OPTIONAL INTERCHANGE CIRCUIT

The following interchange circuit between the DCE and DTE may be provided:

Circuit 112 – Data signalling rate selector (DCE source).

4. TEST POINTS

See Part I, Section C, item 3.

5. CONSTRUCTION

See Part I, Section C, item 4.

Annex 1

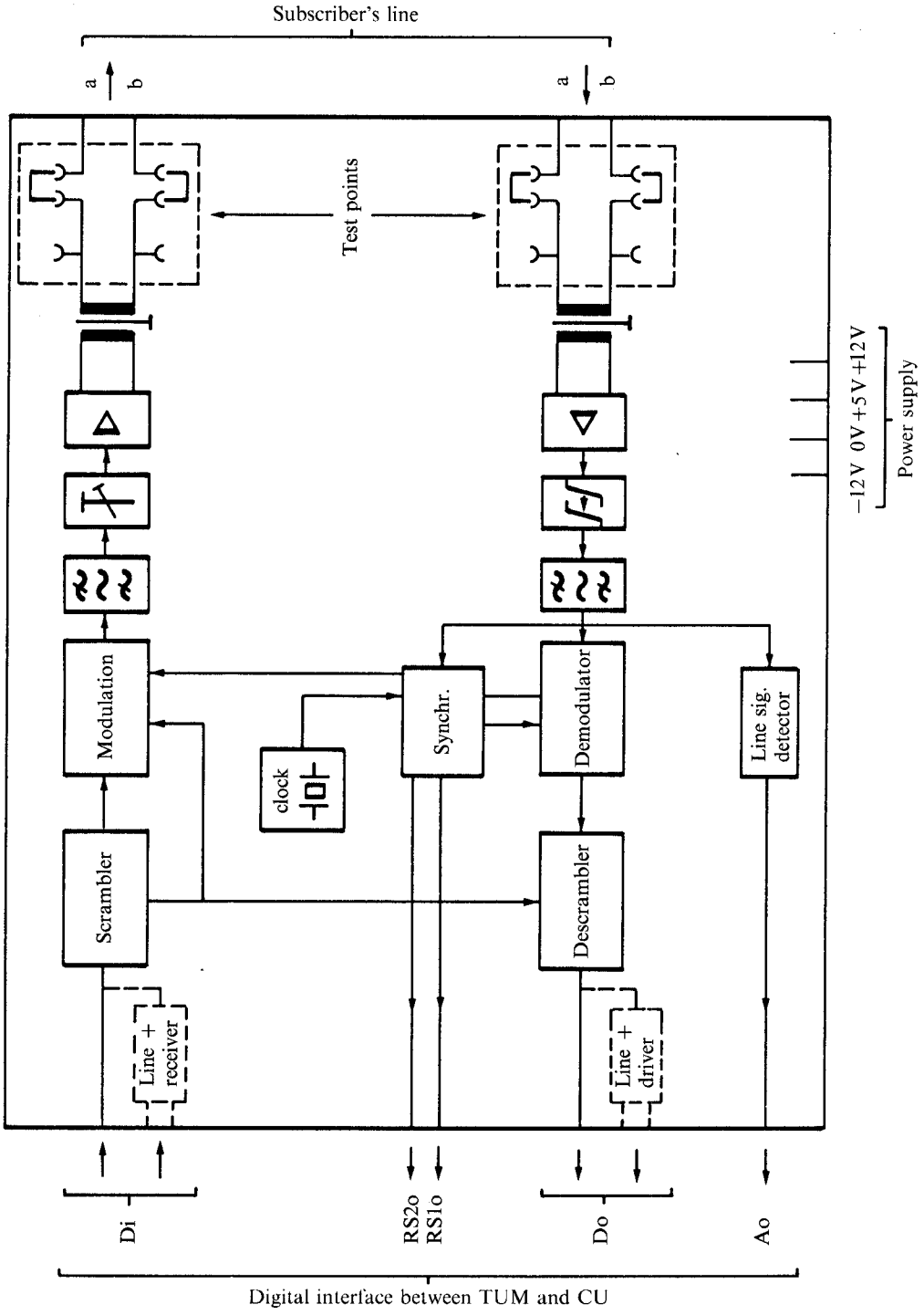
Modulation schemes

Alternative		Part	Section	Page	Description	Type I 3,000/3,200 bit/s dx 4-wire	Type I 3,000/3,200 bit/s dx 2-wire	Type 2,400 dx 4-wire
TUM	Alternative A1:	II	A	63	V.27*bis/ter*	—	—	• (*Note 1*)
	Alternative A2:	I	A	5	V.26 type A and/or B	• (*Note 3*)	—	•
	Alternative B1:	III	A	73	V.26*ter*	—	—	—
	Alternative B2:	III	A	87	V.22*bis*	—	—	—
TUB	Alternative C1:	I	B	26	WAL 2	•	—	•
	Alternative C2:	I	B	29	AM I	•	—	—
	Alternative C3:	I	B	30	AM I	•	—	•
	Alternative C4:	I	B	32	Differential biphase-space	•	—	—
	Alternative C5:	I	B	34	Differential diphase	•	—	—
	Alternative C6:	II	B	65	Differential diphase	—	—	•
	Alternative D1:	I	B	37	AM I (echo cancellation)	—	•	—
	Alternative D2:	I	B	38	Differential biphase-space (echo cancellation)	—	• (*Note 5*)	—
	Alternative D3:	II	B	66	Differential diphase	—	—	—

Note 1: V.27*bis* fall back mode.
Note 2: V.27*ter* fall back mode.
Note 3: For the time being the V.26 type A is not used in type I DCE's.
Note 4: CCITT Recommendation for GSTN working is V.26*bis*.
Note 5: The signalling rate on the line is 12 kbit/s.
• Indicates that its use under consideration by one or more Administrations.

Annex 2

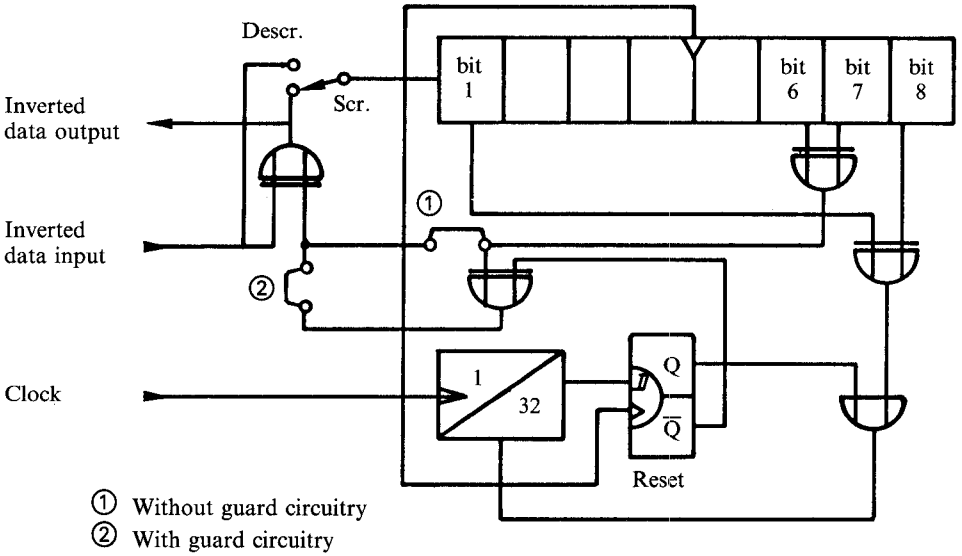
Example of a block diagram of the TUM



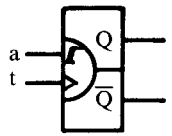
**Note:* If the TU is used e.g. in the exchange a line receiver and a line driver are necessary.

Annex 3

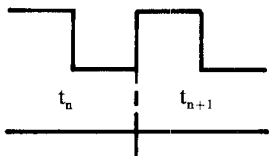
Example of scrambler and descrambler circuitry



Symbols



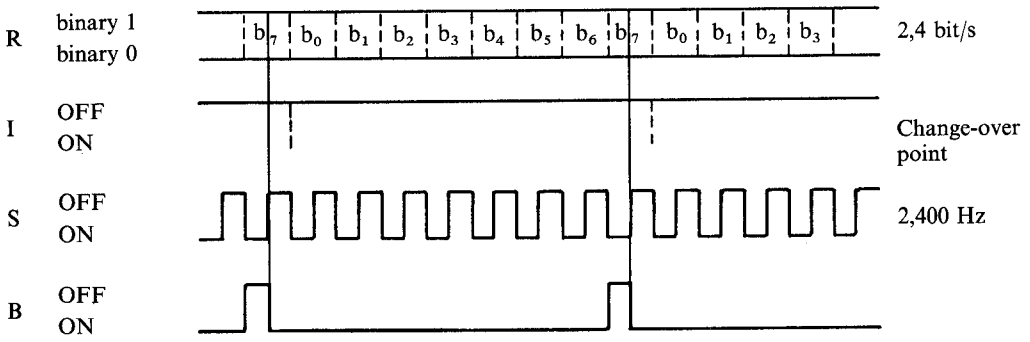
a	b	s1	s2
1	0	1	1
1	1	1	0
0	0	0	0
0	1	1	1



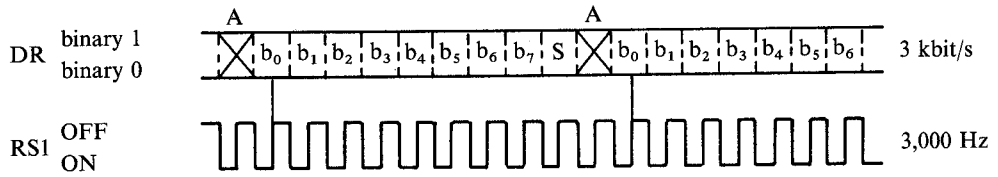
Annex 4

Relationship between data and timing

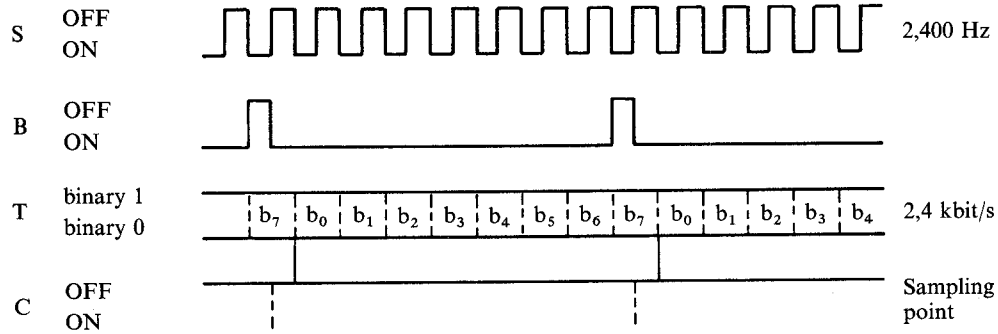
Interface CU – terminal (X.21, e.g. state 1)



Interface TU – CU (e.g. for envelope 8+2)

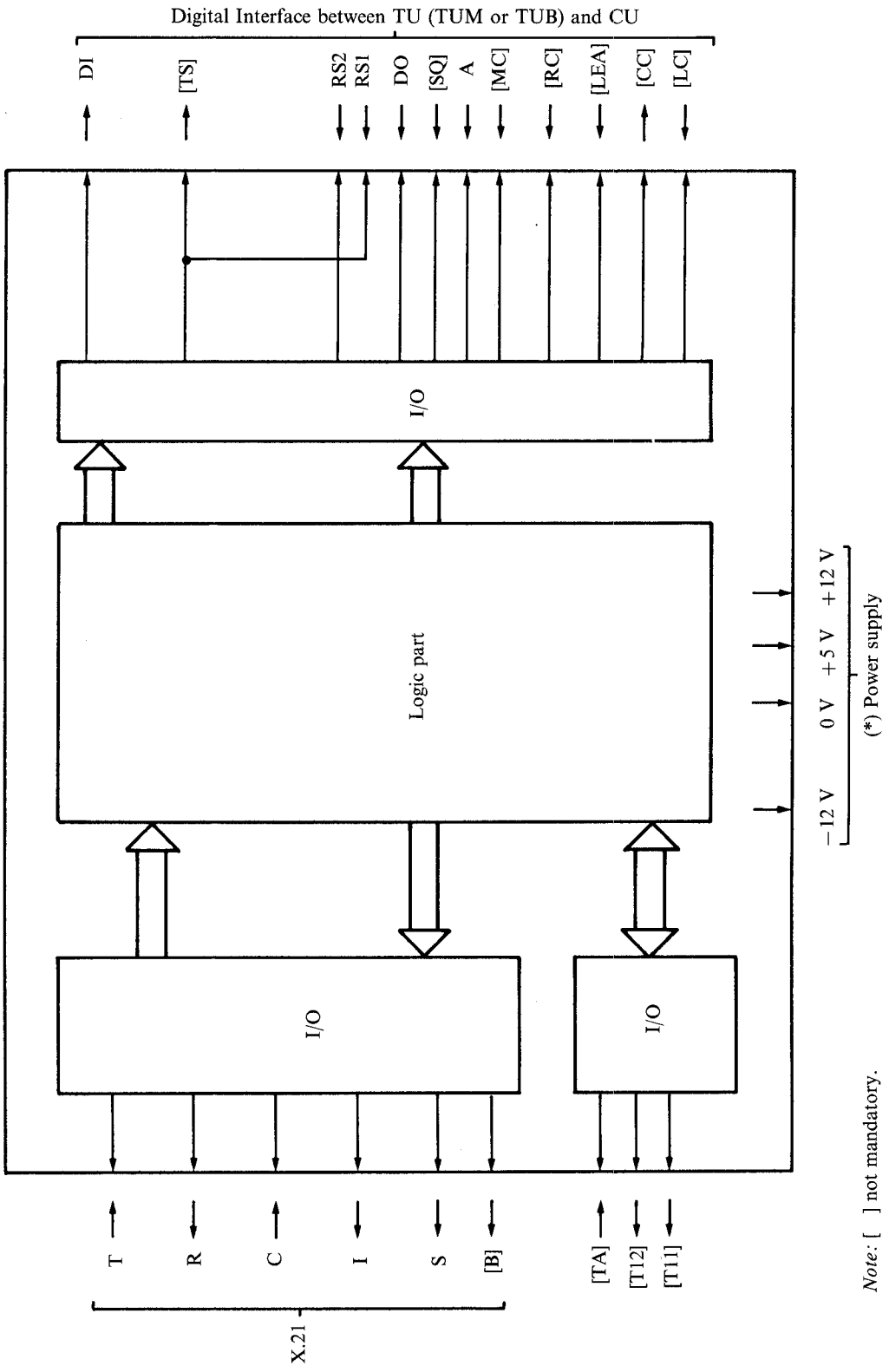


Interface terminal – CU (X.21, e.g. state 1)



Annex 5

Example of a block diagram of the CU

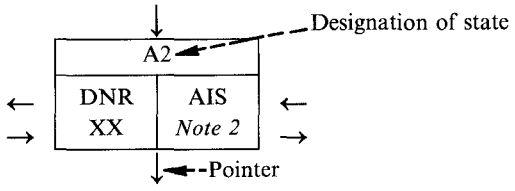


Annex 6, sheet 1

State diagram for alarms and consecutive actions

For the description the following symbols are used:

Example:



The change-over from one state to another can only be made in the direction of the pointer if the conditions associated with the relevant pointer are fulfilled.

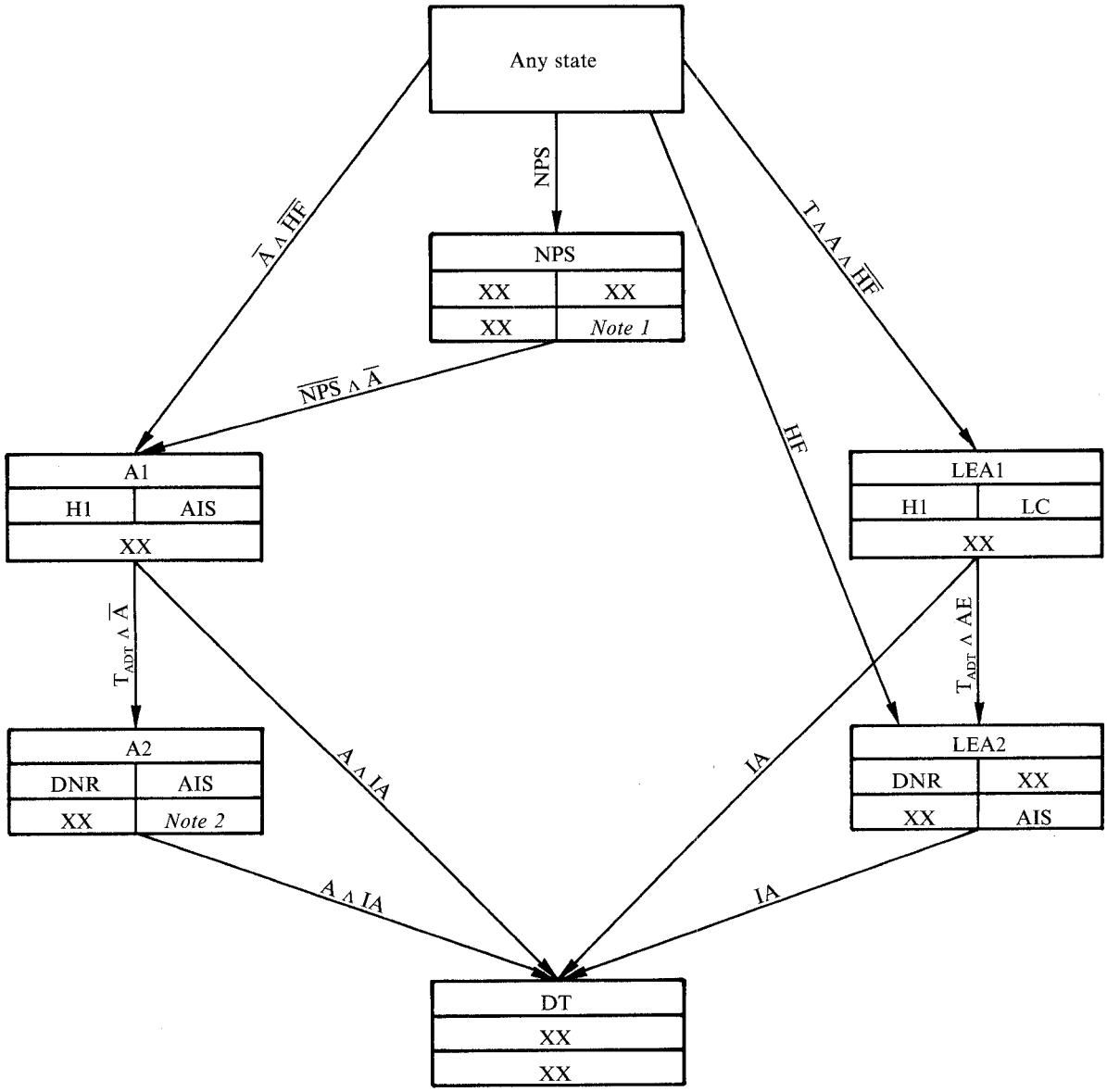
(a) Used abbreviations:

A	Received line signal detector ON ($\overline{A}$ ... OFF).
ADT	Action delay time.
AE	Alignment error.
AIS	All 1 signal.
DNR	DCE not ready.
DT	Data transfer phase (DCE transparent mode).
HF	Hardware failure.
H1	Hold signal 1.
IA	In alignment.
NPS	No power supply.
LC	LEA condition.
LEA	Loss of envelope alignment.
01	Option 1 (... without special signal).
02	Option 2 (... with special signal).
03	Option 3 (... AIS towards the network).
04	Option 4 (... without outgoing carrier).
T	Time until LEA is recognized.
TADT	Time of 2-3 s (ADT) is over.

(b) Used signals:

Signal	Interf. CU to DTE			
	T	C	R	I
H1	—	—	1	ON
DNR	—	—	0	OFF

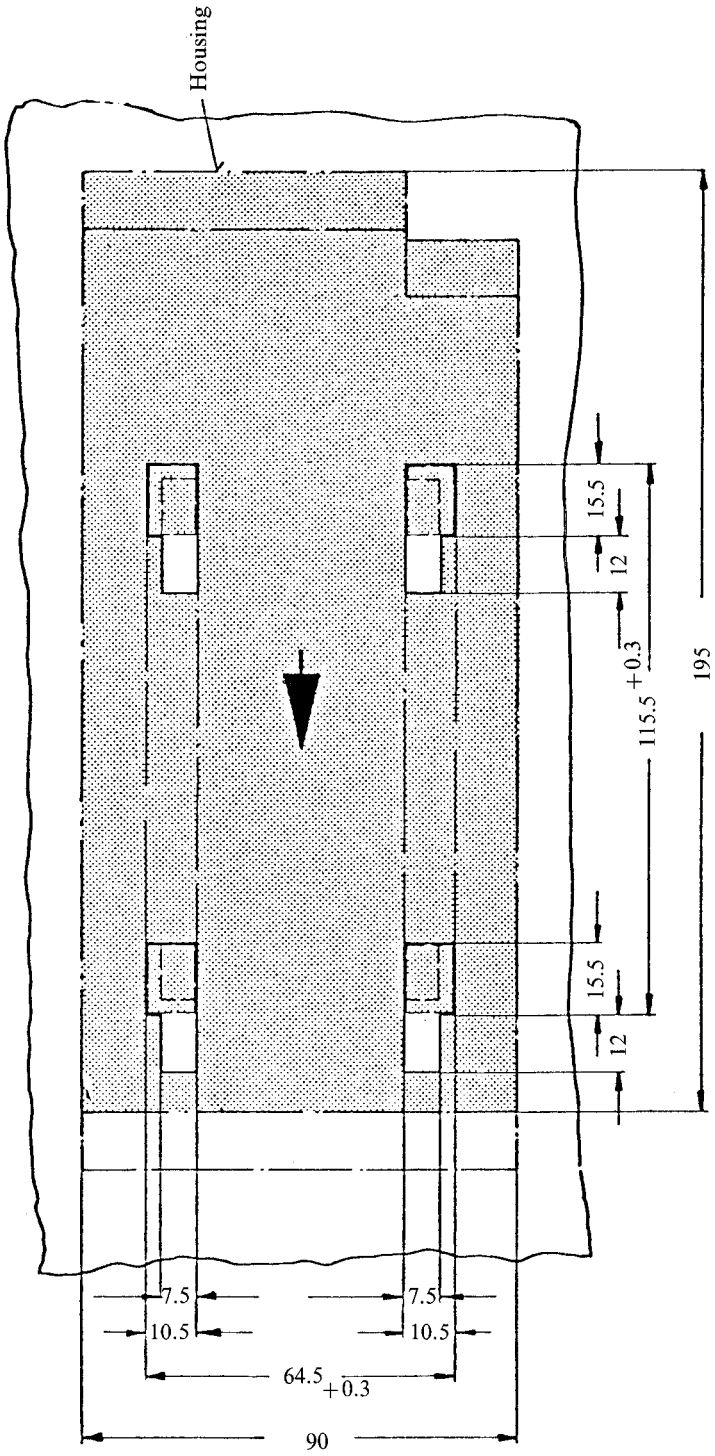
Annex 6, sheet 2



Note 1: see Part I, Section A, item 3.4.1. option 1 or 2.
Note 2: see Part I, Section A, item 3.4.2. option 3 or 4.

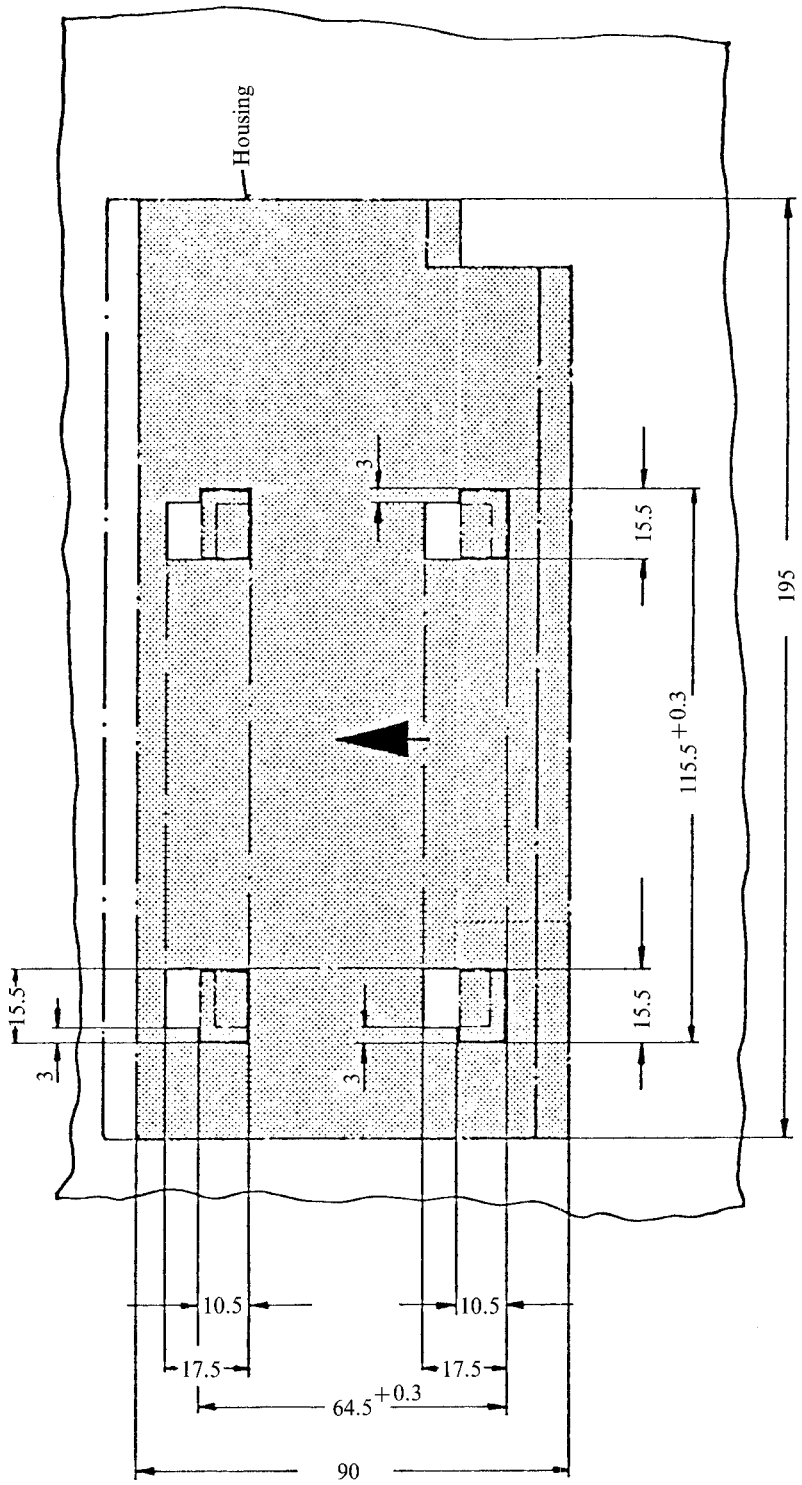
Annex 7, sheet 1

Example of fixing



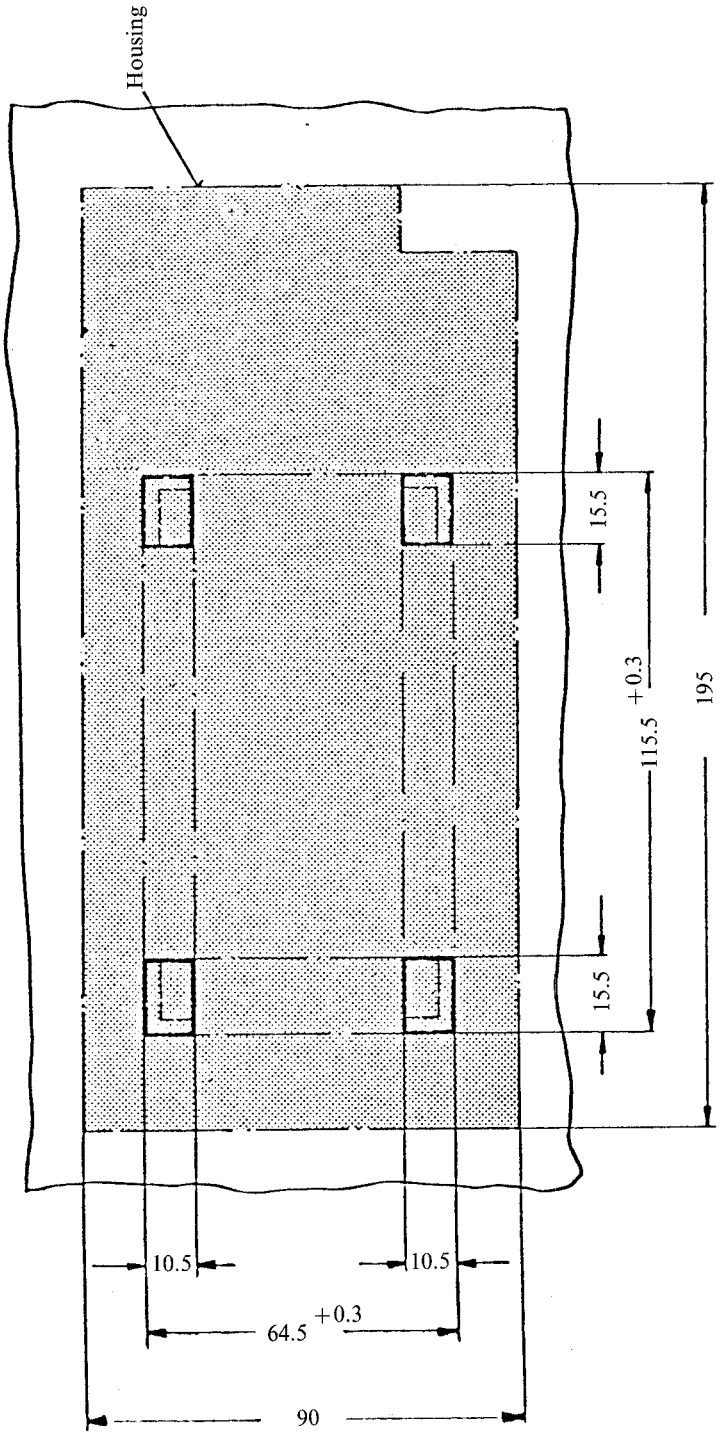
Annex 7, sheet 2

Example of fixing



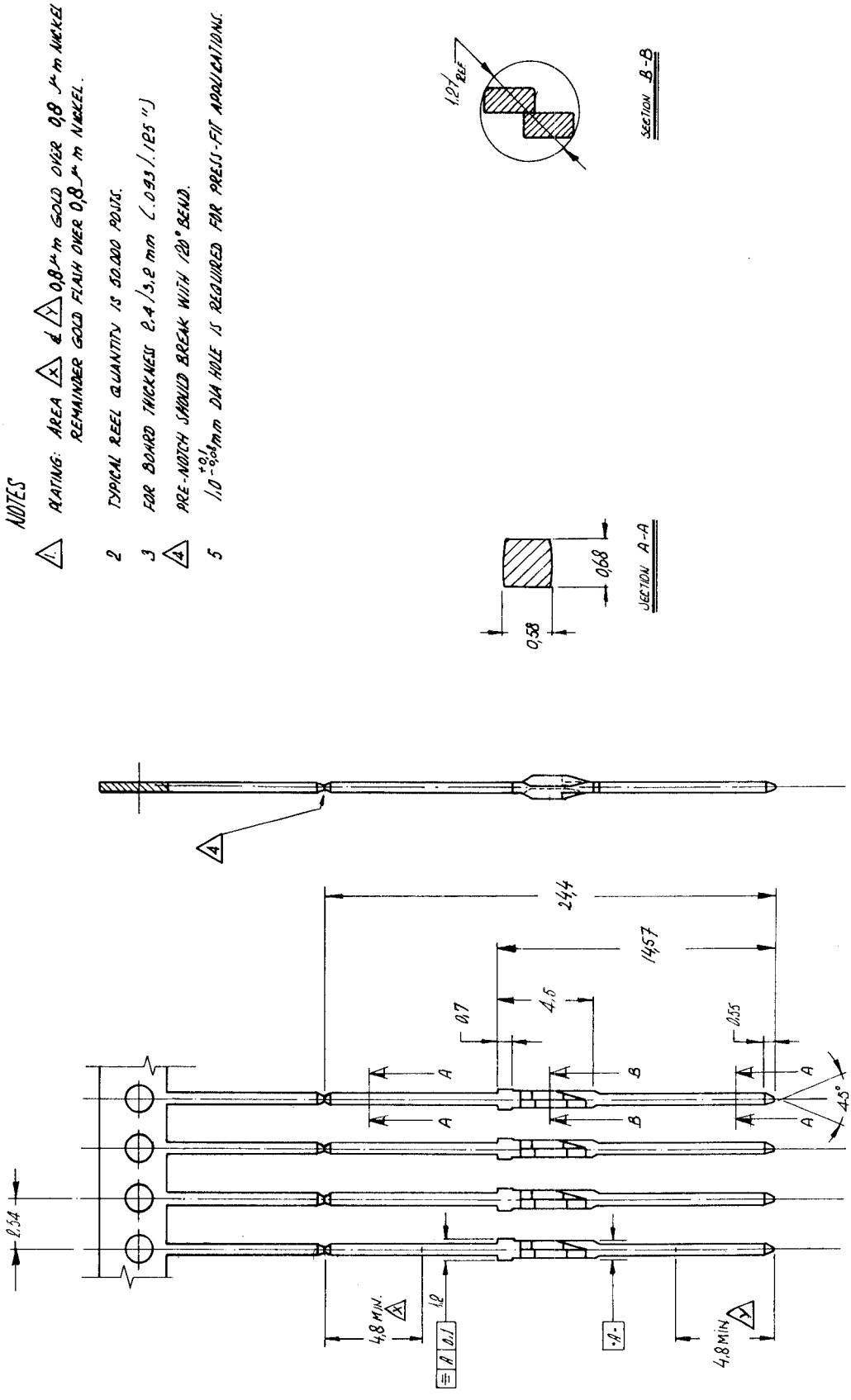
Annex 7, sheet 3

Example of fixing

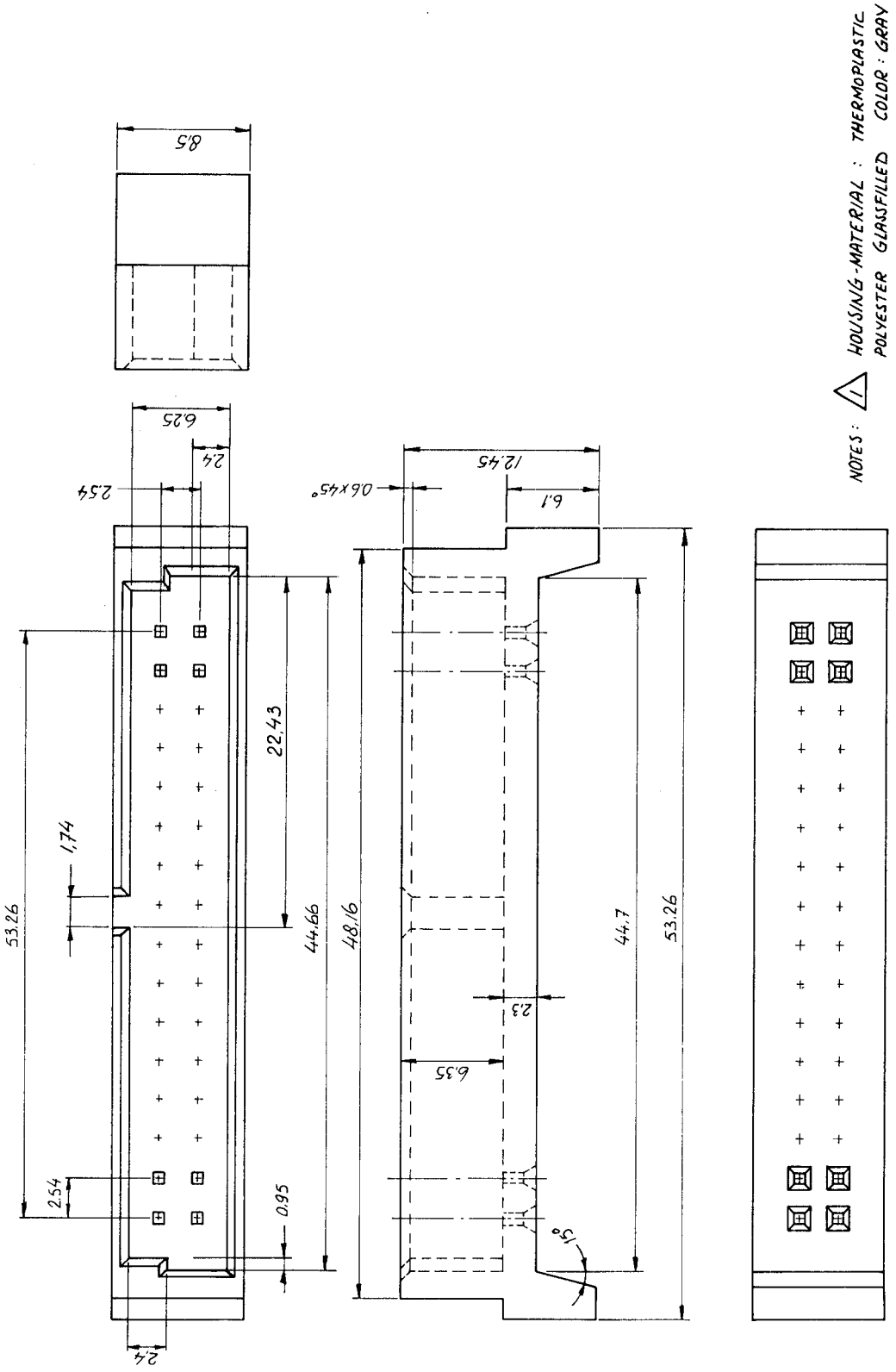


Annex 8, sheet 1

Further details of the connector



Annex 8, sheet 2

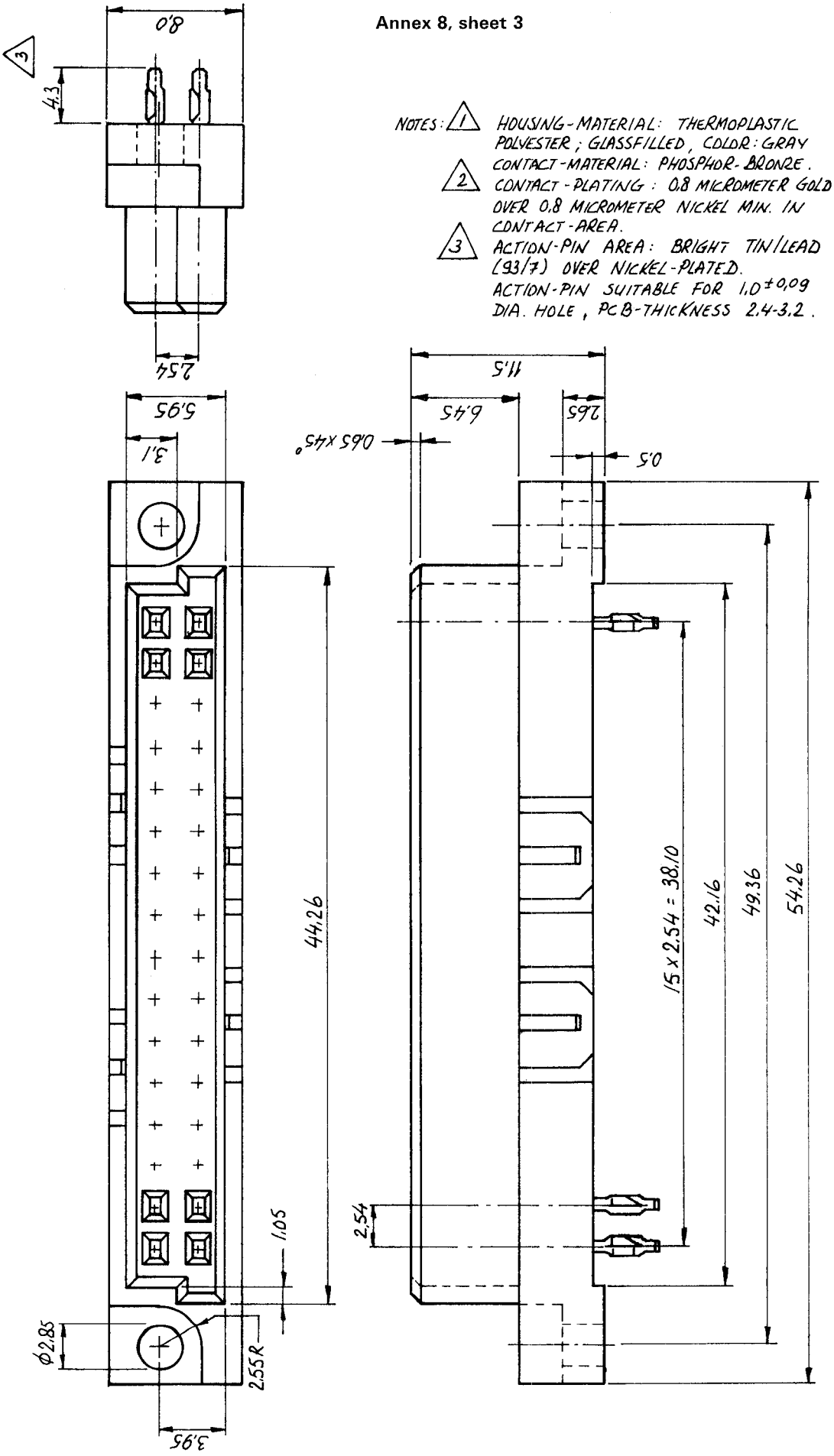


Annex 8, sheet 3

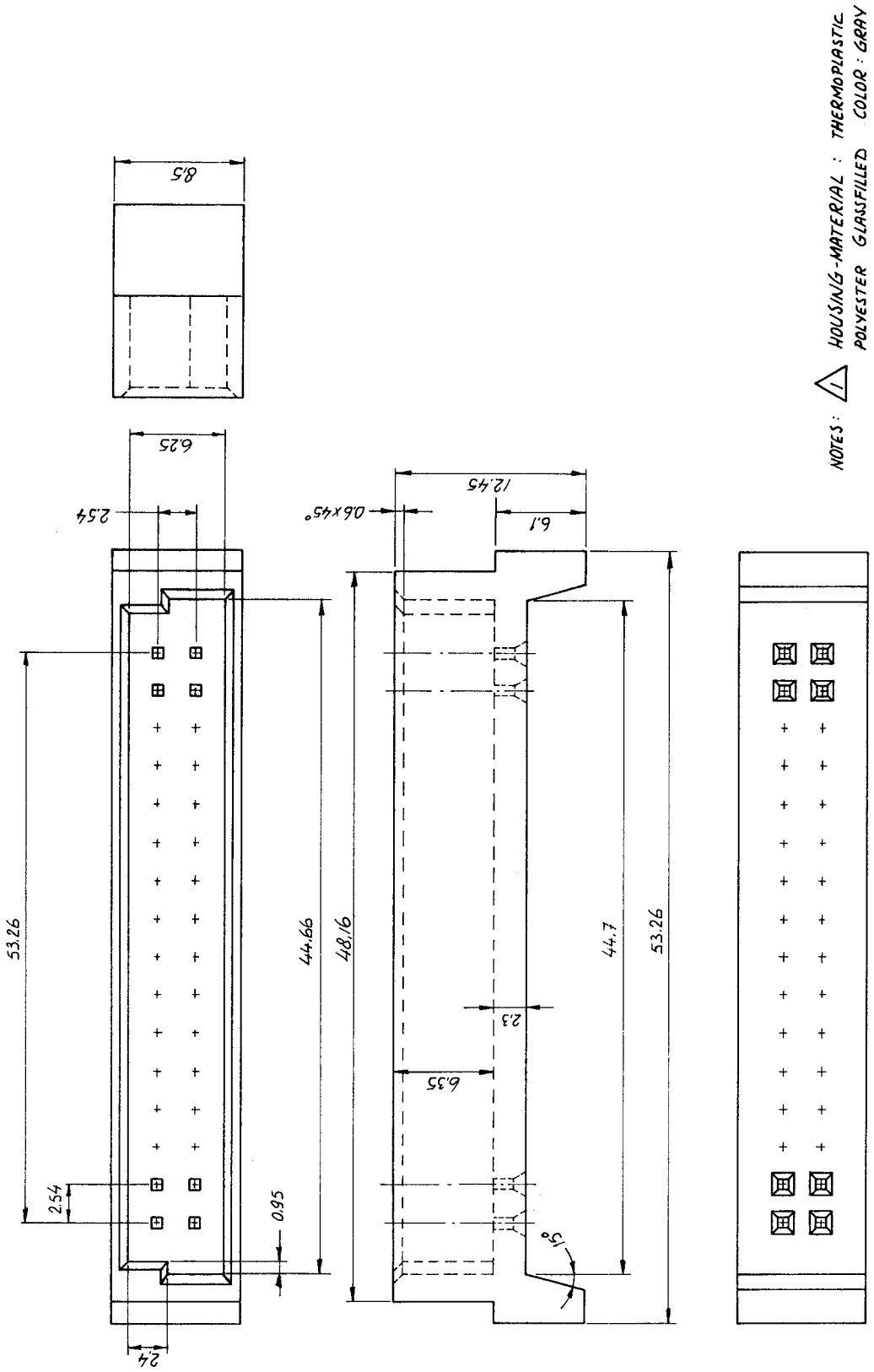
NOTES: 1 HOUSING-MATERIAL: THERMOPLASTIC POLYESTER; GLASSFILLED, COLOR: GRAY

2 CONTACT-MATERIAL: PHOSPHOR-BRONZE. CONTACT-PLATING: 0.8 MICROMETER GOLD OVER 0.8 MICROMETER NICKEL MIN. IN CONTACT-AREA.

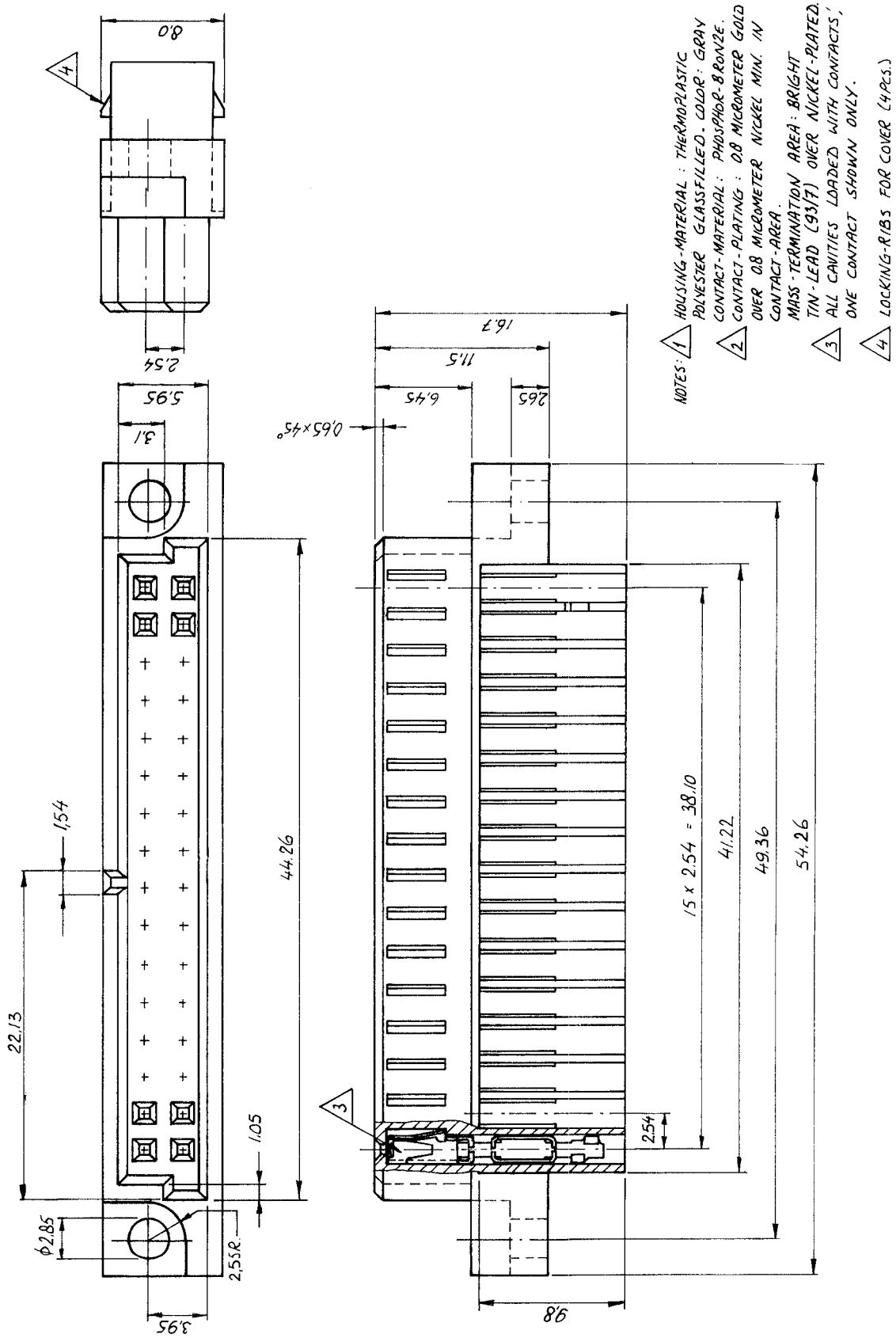
3 ACTION-PIN AREA: BRIGHT TIN/LEAD (93/7) OVER NICKEL-PLATED. ACTION-PIN SUITABLE FOR $1.0^{+0.09}$ DIA. HOLE, PCB-THICKNESS 2.4-3.2.

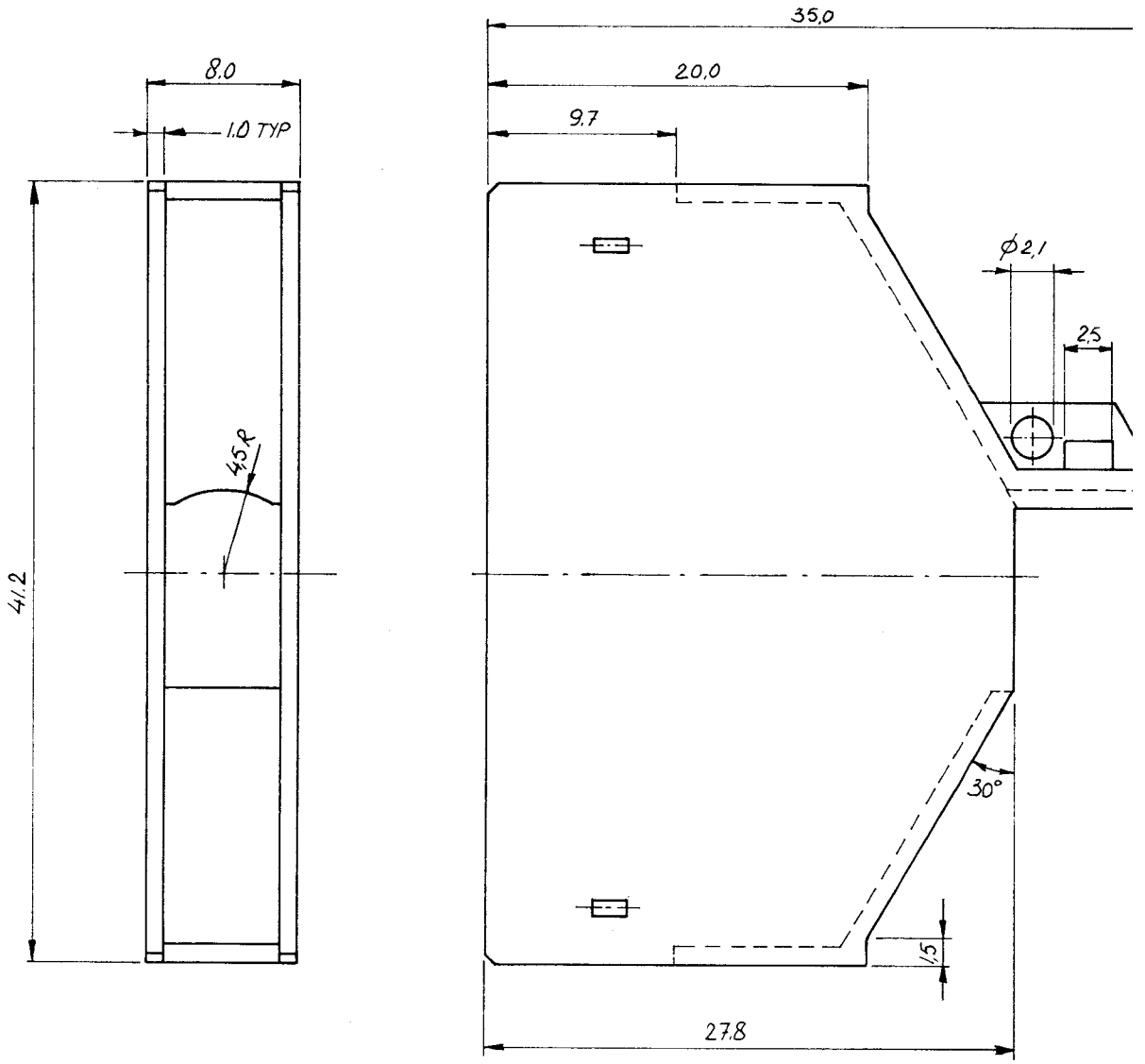


Annex 8, sheet 4



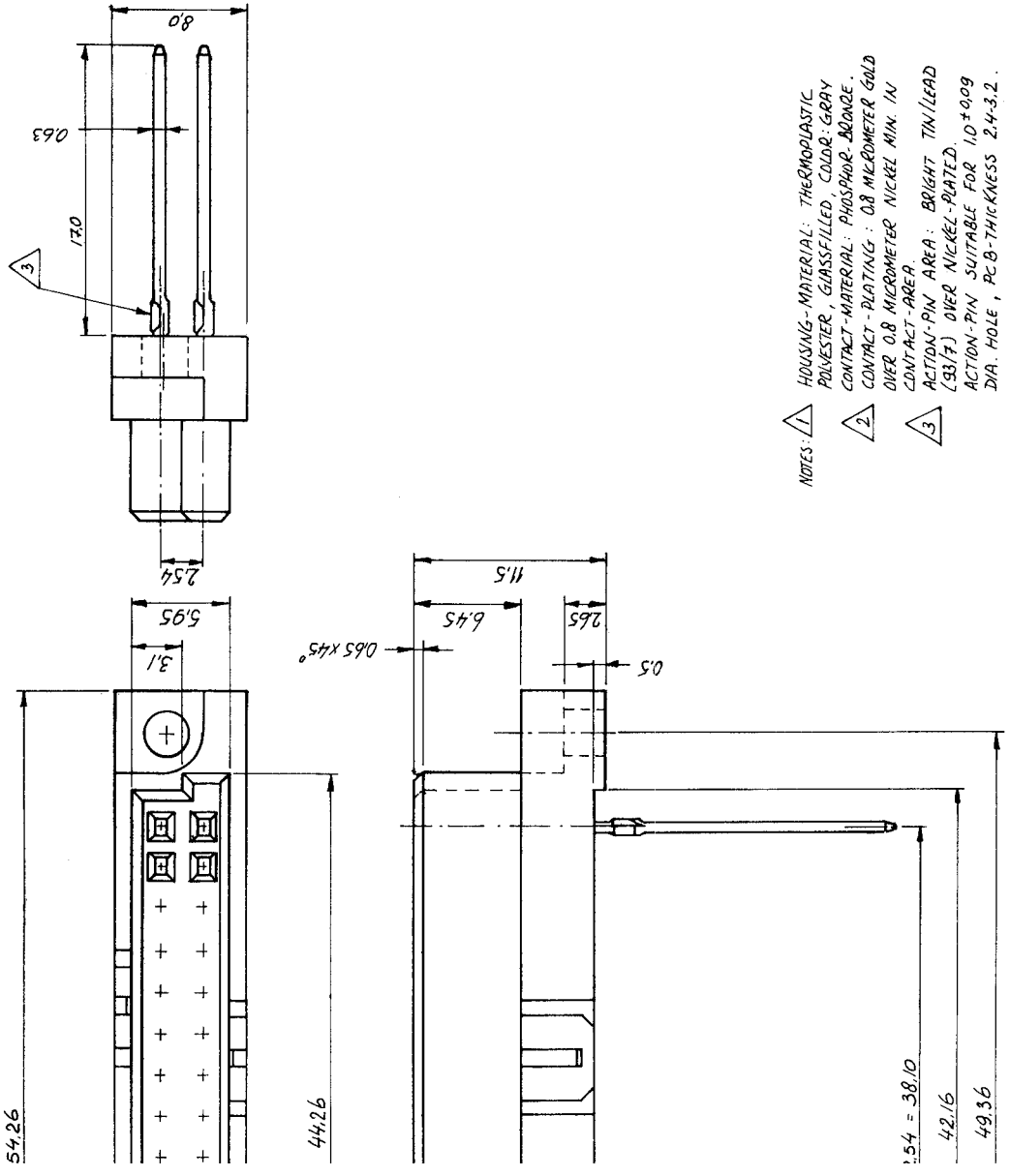
Annex 8, sheet 5



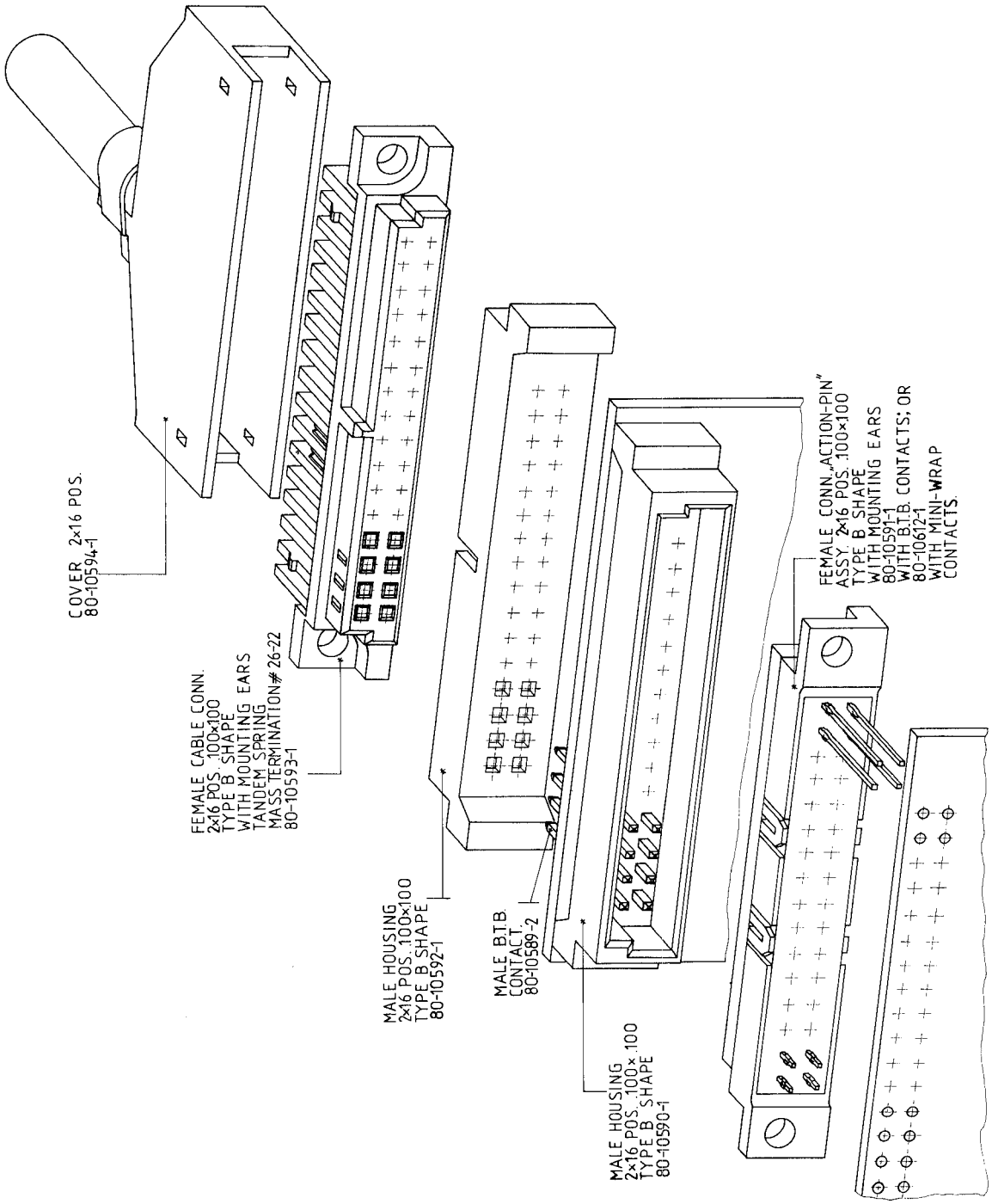


NOTES: COVER FOR CABLE CONN PARTNR. 80-10593-1

Annex 8, sheet 7



Annex 8, sheet 8



Annex 9

Pin allocation for type I, II and III plug-in DCE's

Pin No.	DCE type I	DCE type II	DCE type III	Pin No.	DCE type I	DCE type II	DCE type III
a1	−12 V	−12 V	−12 V	b1	+12 V	+12 V	+12 V
a2	+5 V	+5 V	+5 V	b2	+5 V	+5 V	+5 V
a3	G/OV	102(G)/OV	102/OV	b3	+5 V	+5 V	+5 V
a4	OV	OV	OV	b4	OV	OV	OV
a5	R	104(R)	104	b5	S	115(S)	115
a6	I	109(I)	109	b6	T	103(T)	103
a7	Ip3	141	141	b7	C	105(C)	105
8a	Ip2	140	140	b8	—	—	206*
9a	—	108/2	108	b9	—	—	204*
a10	B	114	114	b10	—	—	207*
a11	TI1	—	211*	b11	—	—	205*
a12	TI2	142	142	b12	—	—	208*
a13	—	—	202*	b13	—	—	219*
a14	—	107	107	b14	—	—	209*
a15	—	106	106	b15	—	—	111 or 112
a16	—	—	203* or 112	b16	TA	—	125

* Reserved for possible future use.

Note: Depending on the application pin No. "a10" is 114 or 113.

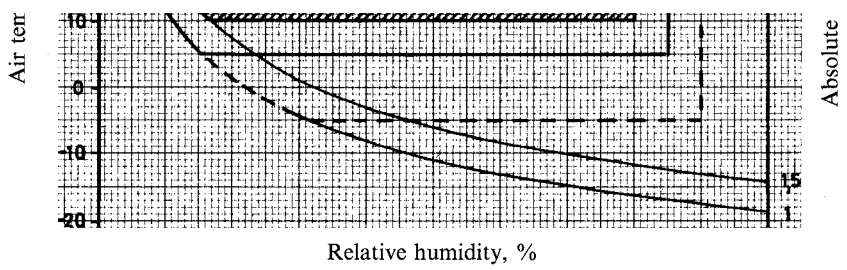


Figure a.

Climatogram for transport
(within the entire geographical area of Europe)

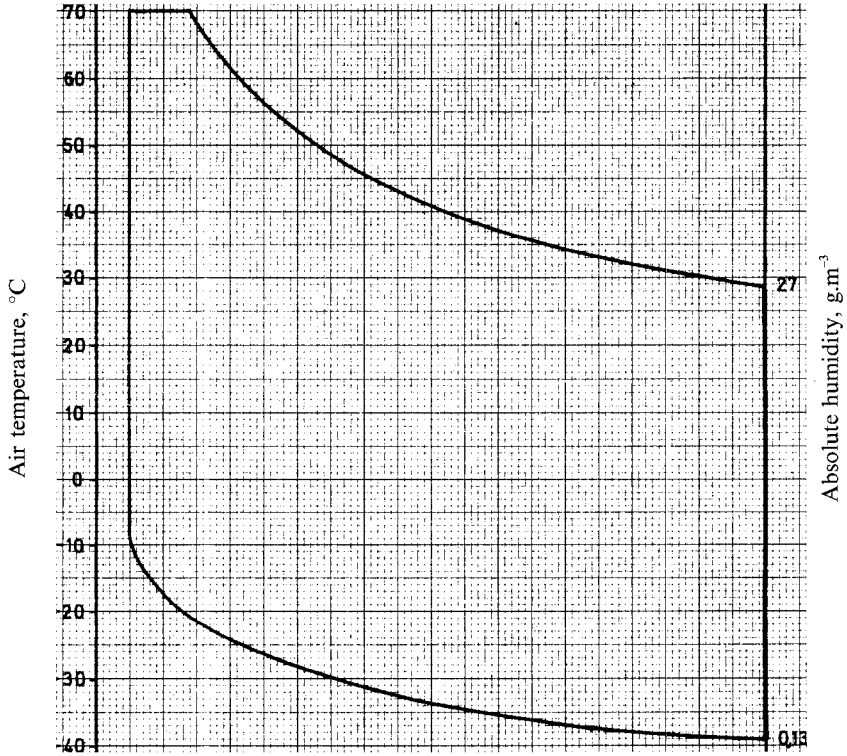


Figure b.

Annex 10, sheet 2

Climatogram for warehousing

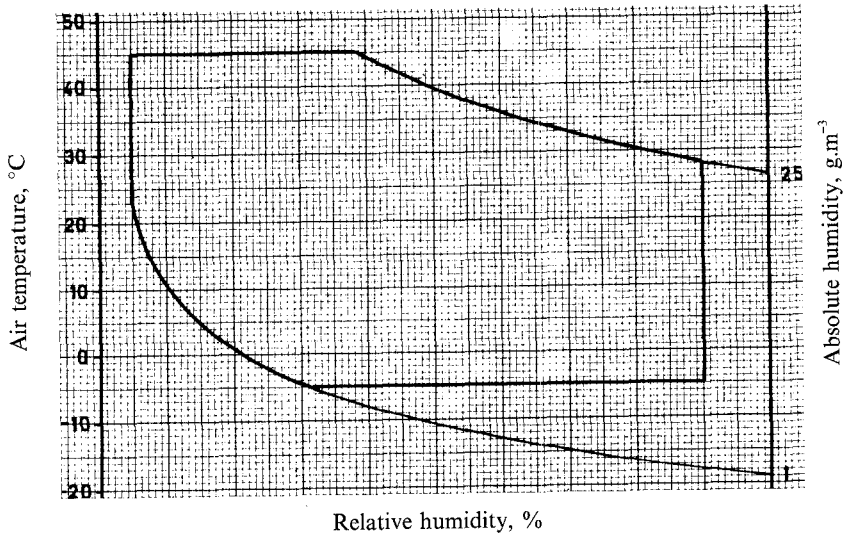
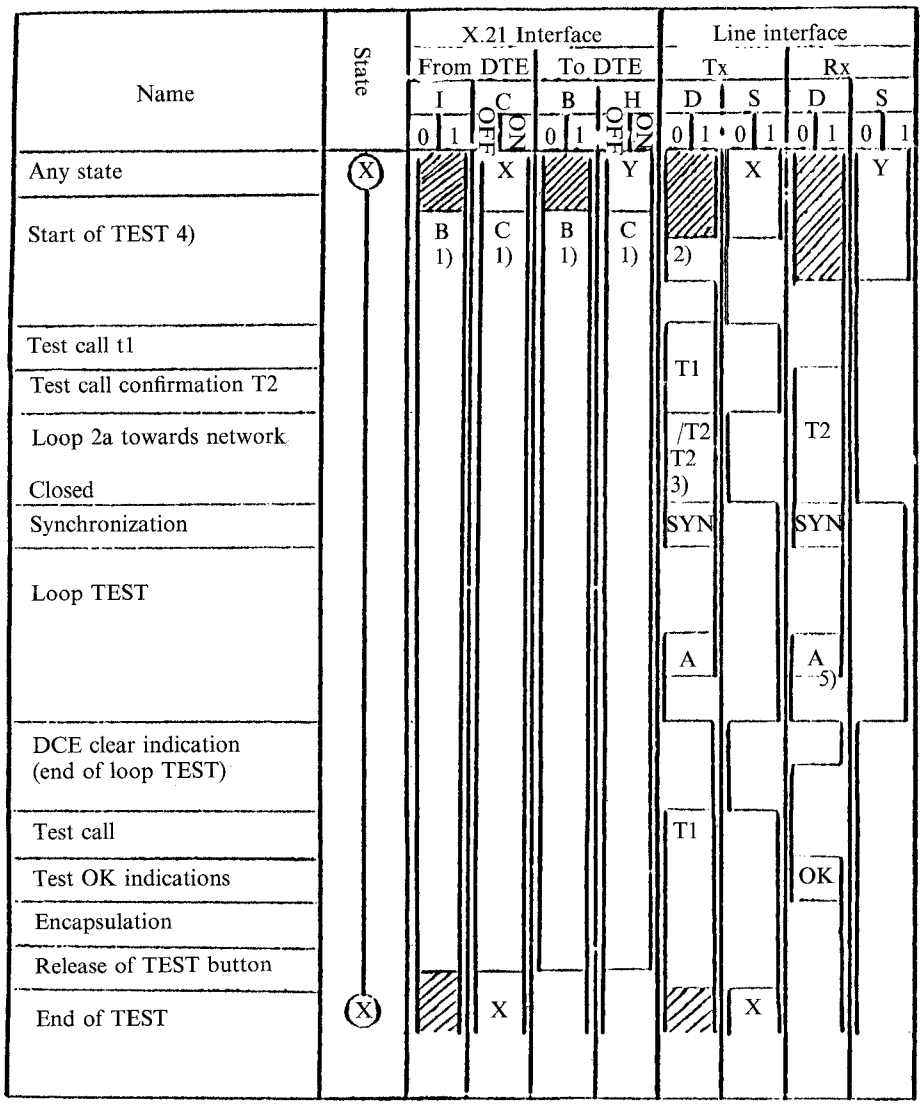


Figure c.

Annex 11

Test call from the DCE

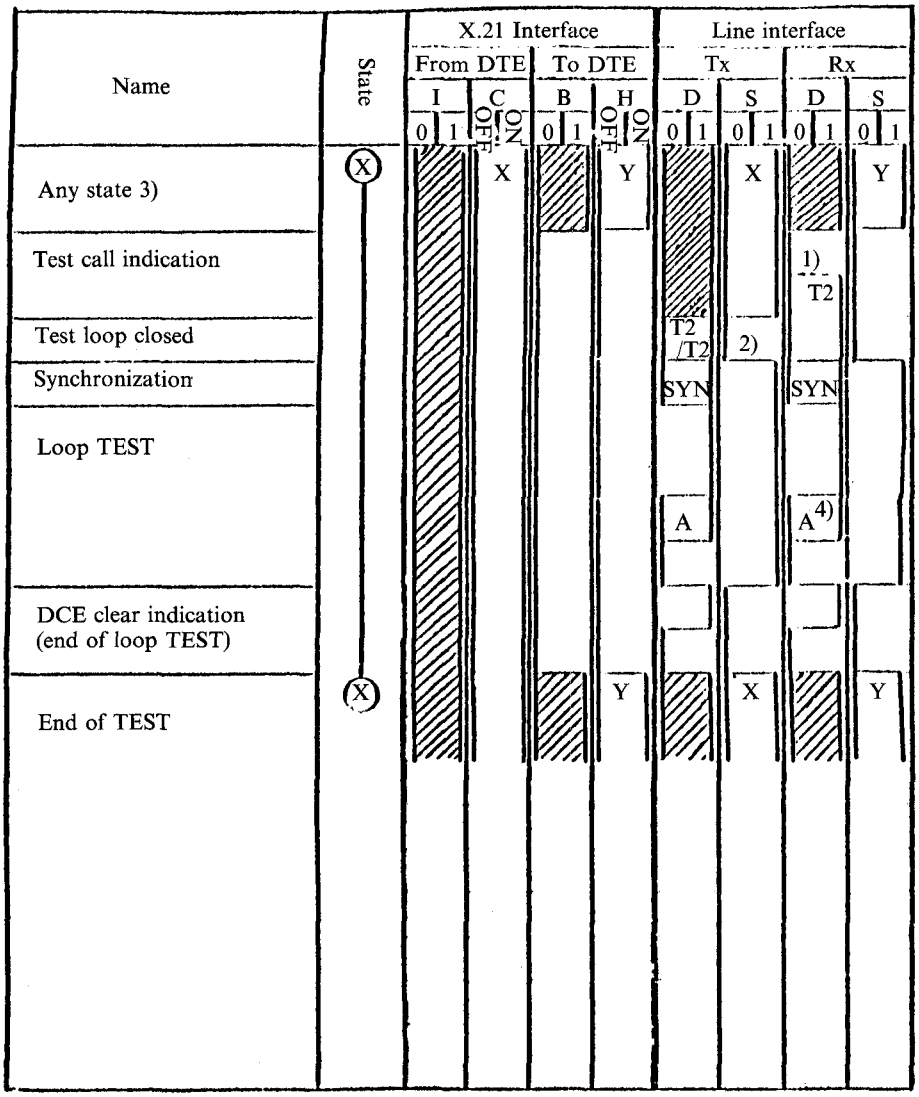


Notes:

1) B and C are signals generated by the DTE. These signals are returned to the DTE, as the loop is closed in the interface DTE-DCE.
2) Test from the DCE is initiated by the DCE sending minimum 3 envelopes CLEAR followed by minimum 3 envelopes READY until READY is received from the network.
3) In DCE's using circuits for SYN-synchronization the looped information is displaced one bit interval. The 1-bit displacement continues until SYN-synchronization has occurred in the DCE. The synchronization circuits are activated when the DCE detects T2 from the network. When the network then sends SYN-characters, synchronization is obtained in the DCE. DCE's not including SYN-circuits returns data without any phase displacement.
4) Depressing of the TEST key on the DCE will close the loop 3d towards the DTE.
5) A = two envelopes SYN′. SYN′ is SYN displaced one bit relative to the network.
6) T1 = 10 11 00 00
   T2 = 10 01 01 00
   T2′ = 01 00 10 10
   A = 00 11 01 00←data bit MSB (most significant bit)
   ↑
   data bit LSB (least significant bit).

Annex 12

Test call from the network

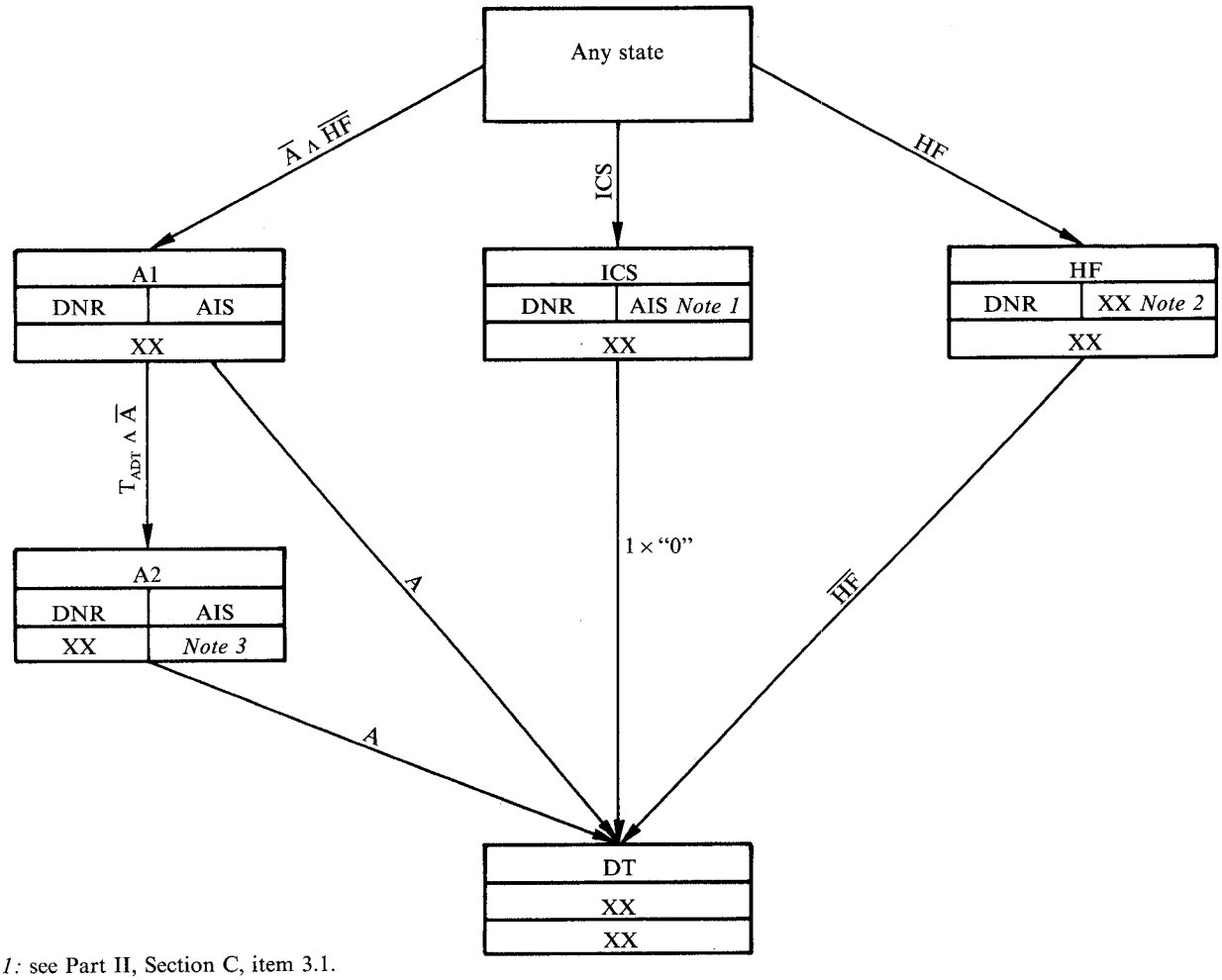


Notes:

1) As TEST CALL INDICATION the DCE will only accept two envelopes CLEAR followed by one envelope T2. The network will send four envelopes CLEAR before the envelope T2.
2) In DCE's using circuits for SYN-synchronization the looped information is displaced by one bit interval. The 1-bit displacement continues until SYN-synchronization has occurred in the DCE. The synchronization circuits are activated when the DCE detects T2 from the network. When the network then sends SYN-characters, synchronization is obtained in the DCE. DCE's not including SYN-circuits return data without any phase displacement.
3) Test with loop 2b will not be initiated when the DCE is engaged in a call.
4) A = two envelopes SYN′. SYN′ is SYN displaced one bit relative to the network.
5) T2 = 10 01 01 00
   T2′ = 01 00 10 10
   A = 00 11 01 00
   ↑ ↑
   | data bit MSB (most significant bit)
   data bit LSB (least significant bit).

Annex 13

State diagram



Note 1: see Part II, Section C, item 3.1.
Note 2: see Part II, Section C, item 3.2.
Note 3: see Part II, Section C, item 3.3.

Used abbreviations:

A	Received line signal detector ON ($\overline{A}$ ... OFF).
ADT	Action delay time.
AIS	All 1 signal.
DNR	DCE not ready (1 = OFF, R = not speficied).
DT	Data transfer phase.
HF	Hardware failure.
ICS	Idle channel state.
T_{ADT}	Time of 2-3 s (ADT) is over.