Recommendation T/CD 02-01 E (Ostende 1979, revised at Cannes 1983)
Concerning the specification of engineering requirements for a synchronous digital multiplexer operating at 64 kbit/s using an 8-bit (6+2) envelope structure

Recommendation proposed by Working Group T/WG 10 "Data Communications" (CD)

Text of the revised Recommendation adopted by the "Telecommunications" Commission:

"The Conference of European Post and Telecommunications Administrations,

Considering

— that CCITT Recommendation X.50 describes the standard for a TDM system for synchronous data transmission at 64 kbit/s using an 8-bit (6+12) envelope structure;
— that GT/CD has studied the harmonization of multiplex equipment for data communication under the auspices of Question CD 1.

Recommends

— that the attached specification of engineering requirements for a synchronous digital multiplexer operating at 64 kbit/s using an 8-bit (6+12) envelope structure, annexed to this Recommendation should be taken into account by all CEPT Administrations when implementation of such a piece of equipment is being planned by Administrations."

Administrations are free to stipulate additional requirements, and also which of the optional requirements, if any, are to be provided.

Note 1: This specification is the subject of continuing study and possible amendments.
Note 2: The Annex is an integral part of the Recommendation.

Contents

Note: Bars at the left hand margin indicate that the wording of this Specification is similar to CCITT Recommendation X.50 for the relevant item.

SCOPE

This specification gives the characteristics of a synchronous digital multiplex equipment which combines on an octet by octet basis, n synchronous homogeneous or heterogeneous tributary channels at the net bit rates from 0.6 to 9.6 kbit/s defined in CCITT Recommendation X.1 into a digital stream, at the gross bit rate of 64 kbit/s, according to CCITT Recommendation X.50.

Section A. ***Common requirements***

1. GENERAL CHARACTERISTICS

The functional structure and the interfaces of the multiplex equipment are shown in Figure 1 (T/CD 02-01).

1.1. Bit rate

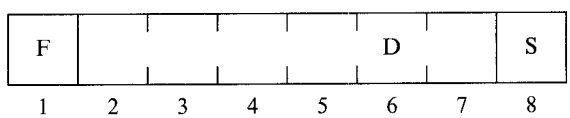
The nominal bit rate is 64 kbit/s. The tolerance on this rate is ± 50 parts per million (ppm).

1.2. Timing signal

It should be possible to synchronise the internal clock in two ways:
i) synchronization from the incoming 64 kbit/s signal;
ii) synchronization from an external clock (optional).
Moreover an independent operation mode should be possible.

2. FRAME STRUCTURE

The signal elements of each individual channel should be assembled in 8-bit envelopes.
In an 8-bit envelope, bit 1 is reserved for framing purposes, bits 2-7 are the information bits of the channel, and bit 8 is a status bit, as follows:



The addition of the framing and the status bits results in 33% increase in bit rate, so that beares channel rates are:
12.8 kbit/s for the 9.6 kbit/s data signalling rate;
6.4 kbit/s for the 4.8 kbit/s data signalling rate;
3.2 kbit/s for the 2.4 kbit/s data signalling rate;
800 bit/s for the 600 bit/s data signalling rate;
The status bit is associated with each envelope and, in conjunction with the information bit, conveys call control information.
For the multiplexing of channels, an 8-bit envelope interleaved structure should be used with a distributed framing pattern employing the framing bits of consecutive 8-bit envelopes.
The multiplexing structure will comprise 80 envelopes as described in 2.1. below; as an alternative the multiplexing structure described in 2.2. can be used.

2.1. 80 8-bit envelope structure

In the case of homogeneous multiplexing the envelopes will appear on the 64 kbit/s bearer as follows:
— 12.8 kbit/s channels will repeat every 5th 8-bit envelope;
— 6.4 kbit/s channels will repeat every 10th 8-bit envelope;
— 3.2 kbit/s channels will repeat every 20th 8-bit envelope;
— 0.8 kbit/s channels will repeat every 80th 8-bit envelope;
Where a heterogeneous multiplexing is used, within each 12.8 kbit/s channel only a homogeneous misture of sub-rate channels will be allowed.
A 72-bit long framing pattern is recommended. This pattern is part of the 80-bit pattern which is generated according to the primitive polynomial:

$$1 + X^4 + X^7$$

of the 2^7 Galois field with the forcing configuration

1 0 0 1 1 0 1

and which is reproduced in Table 1 (T/CD 02-01) showing 8 bits ("A" to "H") reserved for housekeeping.
The first F bit, indicated as "A" in Table 1 (T/CD 02-01) is used to convey to the distant end alarm indications detected at the local end (see paragraph 4.).

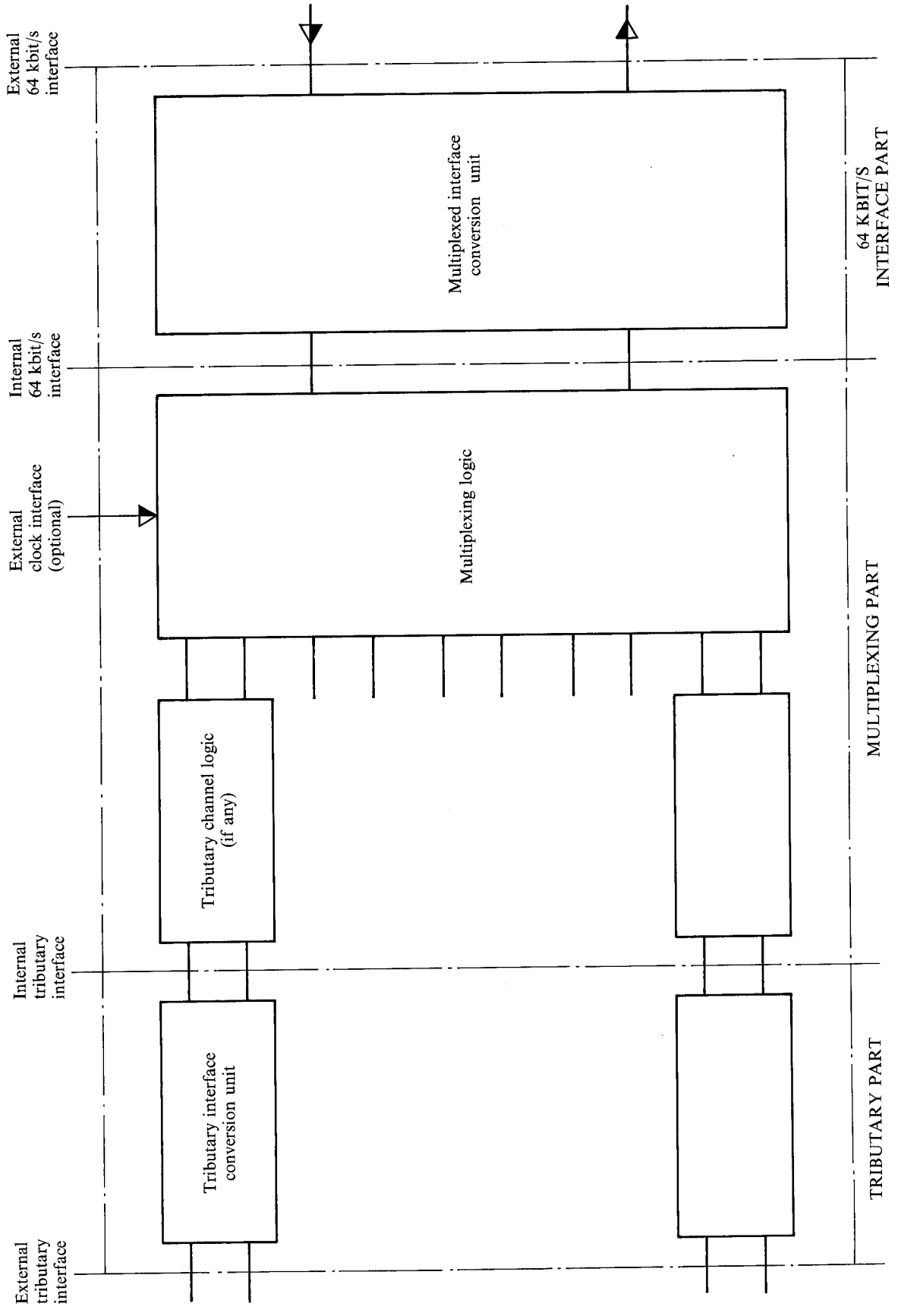


Figure 1 (T/CD 02-01). Functional structure and interfaces of 64 kbit/s data multiplexors.

The "A" bit shall be assigned such that:
"A" equals 1 means no alarm
"A" equals 0 means alarm.

The other F bits indicated as "B", "C", "D", "E", "F", "G", and "H" in Table 1 (T/CD 02-01) could be reserved to convey further international house-keeping information. Pending the resolution of the house-keeping requirements, these bits are provisionally fixed to:
"B" equals 1, "C" equals 1, "D" equals 0, "E" equals 0, "F" equals 1, "G" equals 1, "H" equals 0.

The use of these bits is under study.

1st bit																			
A	1	0	0	0	1	1	1	1	1	B	1	0	0	0	0	1	1	1	0
C	1	1	1	0	0	1	0	1	1	D	0	1	0	0	1	0	0	0	0
E	0	1	0	0	0	1	0	0	1	F	0	0	0	1	0	1	1	1	0
G	0	1	1	0	1	1	0	0	0	H	0	1	1	0	0	1	1	0	1
													└						┘
													Forcing configuration						

Table 1 (T/DC 02-01).

2.2. 20 8-bit envelope structure

In the case of homogeneous multiplexing, the envelopes will appear on the 64 kbit/s bearer as follows:
— 12.8 kbit/s channels will repeat every 5th envelope;
— 6.4 kbit/s channels will repeat every 10th envelope;
— 3.2 kbit/s channels will repeat every 20th envelope;

Where a heterogeneous multiplexing is used, within each 12.8 kbit/s channel, only a homogeneous mixture of sub-rate channels will be allowed.

A 19-bit long framing pattern is recommended. The pattern is part of the 20-bit pattern which is generated according to the primitive polynomial:

$$1 + X^2 + X^5$$

of the 2^5 Galois field with the forcing configuration

0 1 1 1 0

and is reproduced in Table 2 (T/CD 02-01).

The first F bit indicated as "A" in Table 2 (T/CD 02-01) is used to convey to the distant end alarm indications detected at the local end (see paragraph 4.).

The "A" bit shall be assigned such that:
"A" equals 1 means no alarm
"A" equals 0 means alarm

1st bit																			
A	1	1	0	1	0	0	1	0	0	0	0	1	0	1	0	1	1	1	0
															└				┘
															Forcing configuration				

Table 2 (T/DC 02-01).

2.3. Allocation of channels on international multiplex links at 64 kbit/s

On international links carrying data channels multiplexed at 64 kbit/s, the allocation of tributary channels at rates of 0.6, 2.4, 4.8, 9.6 kbit/s within the multiplex frame should be chosen, by bilateral agreement, among the configurations listed in Table 3 (T/CD 02-01).

Note: The phase number i (i = 1, ..., 5) corresponds to the set of envelopes i + 5j (j = 0, ..., 15 for 80 envelopes frames; j = 0, ..., 3 for the 20 envelopes frame) of each frame. Each phase contains either one 9.6 kbit/s or two 4.8 kbit/s or four 2.4 kbit/s or sixteen 0.6 kbit/s channels.

Configuration number	Phase number				
	1	2	3	4	5
01	9.6	9.6	9.6	9.6	9.6
02	9.6	9.6	9.6	9.6	4.6
03	9.6	9.6	9.6	9.6	2.4
04	9.6	9.6	9.6	9.6	0.6
05	9.6	9.6	9.6	4.8	4.8
06	9.6	9.6	9.6	4.8	2.4
07	9.6	9.6	9.6	4.8	0.6
08	9.6	9.6	9.6	2.4	2.4
09	9.6	9.6	9.6	2.4	0.6
10	9.6	9.6	9.6	0.6	0.6
11	9.6	9.6	4.8	4.8	4.8
12	9.6	9.6	4.8	4.8	2.4
13	9.6	9.6	4.8	4.8	0.6
14	9.6	9.6	4.8	2.4	2.4
15	9.6	9.6	4.8	2.4	0.6
16	9.6	9.6	4.8	0.6	0.6
17	9.6	9.6	2.4	2.4	2.4
18	9.6	9.6	2.4	2.4	0.6
19	9.6	9.6	2.4	0.6	0.6
20	9.6	9.6	0.6	0.6	0.6
21	9.6	4.8	4.8	4.8	4.8
22	9.6	4.8	4.8	4.8	2.4
23	9.6	4.8	4.8	4.8	0.6
24	9.6	4.8	4.8	2.4	2.4
25	9.6	4.8	4.8	2.4	0.6
26	9.6	4.8	4.8	0.6	0.6
27	9.6	4.8	2.4	2.4	2.4
28	9.6	4.8	2.4	2.4	0.6
29	9.6	4.8	2.4	0.6	0.6
30	9.6	4.8	0.6	0.6	0.6
31	9.6	2.4	2.4	2.4	2.4
32	9.6	2.4	2.4	2.4	0.6
33	9.6	2.4	2.4	0.6	0.6
34	9.6	2.4	0.6	0.6	0.6
35	9.6	0.6	0.6	0.6	0.6
36	4.8	4.8	4.8	4.8	4.8
37	4.8	4.8	4.8	4.8	2.4
38	4.8	4.8	4.8	4.8	0.6
39	4.8	4.8	4.8	2.4	2.4
40	4.8	4.8	4.8	2.4	0.6
41	4.8	4.8	4.8	0.6	0.6
42	4.8	4.8	2.4	2.4	2.4
43	4.8	4.8	2.4	2.4	0.6
44	4.8	4.8	2.4	0.6	0.6
45	4.8	4.8	0.6	0.6	0.6
46	4.8	2.4	2.4	2.4	2.4
47	4.8	2.4	2.4	2.4	0.6
48	4.8	2.4	2.4	0.6	0.6
49	4.8	2.4	0.6	0.6	0.6
50	4.8	0.6	0.6	0.6	0.6
51	2.4	2.4	2.4	2.4	2.4
52	2.4	2.4	2.4	2.4	0.6
53	2.4	2.4	2.4	0.6	0.6
54	2.4	2.4	0.6	0.6	0.6
55	2.4	0.6	0.6	0.6	0.6
56	0.6	0.6	0.6	0.6	0.6

Table 3 (T/CD 02-01). Allocation of tributary channels in the 64 kbit/s multiplex frame.

3. ALIGNMENT

3.1. Envelope alignment at the tributary interface

This paragraph is not applicable in the case in which the envelope structure is not present on subscriber loop.

The following main features should be fulfilled in any other case.

— Framing pattern in the F bits of consecutive envelopes: . . . 0 1 0 1 . . .

— Bit S transparently pass from tributary to 64 kbit/s interface and v.v. (except in some maintenance operation).

— Mean time for the recovery of envelope alignment after a slip and under the assumption of absence errors: < 50 envelopes (provisional value).

3.2. Frame alignment at 64 kbit/s interface

The 72-bit and 19-bit pattern as defined in paragraph 2.1. for an 80 envelopes frame and in paragraph 2.2., for a 20 envelopes frame, provide the means for fast and secure frame alignment.

3.2.1. *General requirements*

i) The frame synchronization method should be insensitive as far as possible to bit errors, error bursts and short bursts of AIS generated by transmission equipment.

ii) When a slip occurs in the transmission equipment a fast frame alignment recovery must be possible.

3.2.2. *Framing method performance*

i) The frame alignment recovery time, after a slip and in absence of bit errors should be less than 120 envelopes with 95% probability;

ii) The time from the start of a disturbance as defined in 3.2.1.i) to any action affecting the data channels including the transmission of alarm to the distant end defined in paragraph 2., shall be greater than X (X in the range $1 \div 20$ ms);

iii) A random error rate of 1 in 10^4 shall not cause any frame alignment recovery action.

4. FAULT CONDITIONS AND CONSEQUENT ACTIONS

4.1. Fault conditions

The multiplex equipment should detect the following fault conditions:

— Failure of power supply;
— Failure of timing:
— Loss of incoming signal at the tributary interface;
— Loss of envelope alignment at the tributary interface;
— Loss of incoming signal or frame alignment at the 64 kbit/s interface;
— Alarm from far end.

The need for an error rate monitoring is for further study.

4.2. Consequent actions

Further to the detection of a fault condition, appropriate actions should be taken as specified in Table 4 (T/CD 02-01).

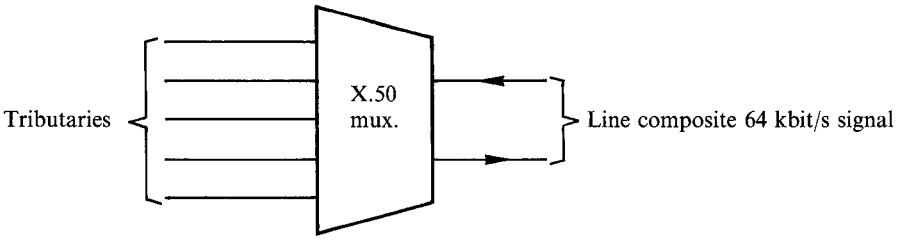
When the Alarm indication signal (AIS) (see *Note 1*) is detected at the 64 kbit/s interface, the local prompt alarm indication should optionally be inhibited and the AIS should be sent on all tributaries.

Note 1: The equivalent binary content of the Alarm indication signal (AIS) is a continuous stream of 1 s.

Note 2: The Alarm to far end is transmitted by changing bit A of 64 kbit/s framing pattern from the state 1 to the state 0 (see paragraph 2.).

Note 3: When the prompt alarm is not inhibited, the AIS or subsequent loss of frame alignment is regarded as Service alarm indicating that the data service is interrupted.

Note 4: It is for further study whether the Service alarm detected by means of AIS should be conveyed in a separate housekeeping bit, e.g. bit B, to the far end.



		Alarm		Action	
Equipment part	Fault conditions	Deferred	Prompt	Towards tributary	Towards composite signal
Central part	Power and timing failure (Other fault conditions may be relevant, e.g. buffer overflow)	—	Yes		
Receiving side from tributaries	Loss of incoming signal	—	Yes		Network out of service after a specified period *(Note 1)* on the relevant tributary channel
	Loss of envelope alignment	—	Yes		Network out of service after a specified period *(Note 1)* on the relevant tributary channel
Receiving side from composite signal	Loss of incoming signal or frame alignment	—	Yes	AIS on all tributaries	Alarm to far end
	Alarm from far end	—	Yes		

Note: A yes in the Table signifies that an action should be taken as a consequence of the relevant fault condition.

Table 4 (T/CD 02-01). Fault conditions and consequent actions for X.50 multiplexor.

Note 1: Signal during specified period to be D = 1, S = OFF.

5. TEST LOOPS

A loop (or some loops) should be implemented for maintenance purposes.

With reference to Figure 2 (T/CD 02-01) at least one of the following implementations is possible:

— loop i (external channel loop), manually and/or automatically activated, locally and/or remotely controlled;

— loop k (digital logic channel loop), automatically activated, locally and/or remotely controlled;

— loop l (digital logic channel loop, toward user), manually activated;

— loop o (digital logic aggregate loop), manually activated;

— loop x (external aggregate loop), manually activated; in some cases (when there is a built-in modem) it corresponds to loop 4.

During the condition of loops i or k activated, the AIS signal must be automatically sent toward the user.

As far as the control of loops i and k is concerned, it should be performed by mean of the multiplex signal, without interfering the transmission of the channels not interested by the loop. The signals for the activating and disactivating procedures should be inserted into the time slot relative to the interested channel through a maintenance interface (to be specified in the future) of the local or remote multiplexer.

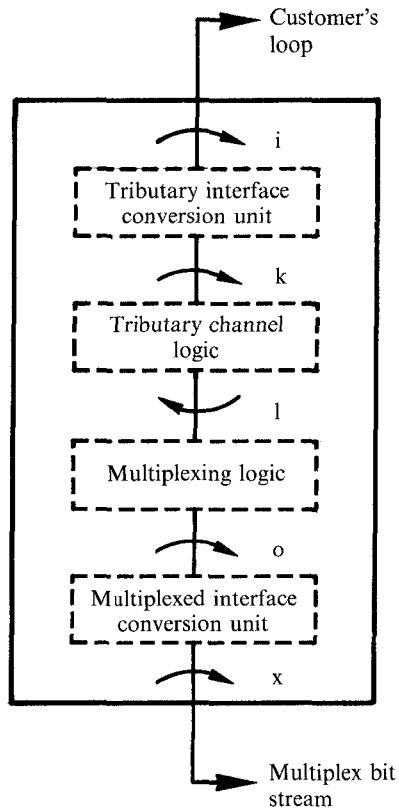


Figure 2 (T/CD 02-01). Possible test loops on X.50 multiplexor.

6. PERFORMANCES

The maximum transmission delay of the last bit of the envelope introduced between the external interfaces of the multiplexer (see Figure 1 / T/CD 02-01) is 12 bit intervals at tributary gross rate in the direction toward the multiplexed side whereas in the opposite direction it is 8 bit intervals at tributary rate plus the delay introduced by buffer if it exists (see paragraph 1. in Section C).

7. POWER SUPPLY

The requirements for the power supply are stated in specification T/TR 02-02.

8. MECHANICAL REQUIREMENTS

The mechanical requirements are stated in specification T/TR 02-01.

9. ENVIRONMENTAL REQUIREMENTS

The environmental requirements are stated in specification T/TR 02-03.

Section B. *Network dependent requirements*

1. INTERFACES

The specified interfaces are shown in Figure 1 (T/CD 02-01).

1.1. Tributary interfaces

1.1.1. *Functional requirements*

This paragraph is not applicable in the case in which the envelope structure is not present on subscriber loop.

The following main features should be fulfilled in any other case:
— both in transmit and receive directions the tributary signals have a 6 + 2 envelope structure;
— the F-bit towards the subscriber is generated in the multiplexer; the F-bit from the subscribers has to be recognized in the multiplexer.

1.1.2. *Tributary interfaces definitions*

(a) External tributary interface (see Figure 1 (T/CD 02-01)).

Two main variants of the interface exist.

i) when the Tributary interface conversion unit is an integral part of the multiplexer, the interface will be a physical two wire or four wire interface, carrying baseband or voiceband signals. The signals will be specified in the Tributary interface conversion unit specification;

ii) when external transmission equipment is used, such as individual voiceband modems for different data user rates, the interface will be a digital modem interface of the V.24 type, and the Tributary interface conversion unit consists of a modem adaptor.

Both variants can exist in the same multiplexer depending on the transmission requirements of the individual channels.

(b) Internal tributary interface (see Figure 1 (T/CD 02-01)).

The internal tributary interface is defined by the functional interface circuit as given in Table 5 (T/CD 02-01).

The electrical characteristics of the interface could be defined by the logical circuits and are left for further study.

The functional interface circuits may or may not be accessible as a physical interface.

Interface circuit designation	Interface circuit name	Direction	
		from mux.	to mux.
G	Signal ground or common return		
TT	Tributary channel transmitted data	X	
TR	Tributary channel received data		X
TST	Tributary channel transmitter signal element timing	X	
TSR	Tributary channel receiver signal element timing (optional)*		X
TLC	Loop control (optional)	X	
TA	Recieved line signal level detector		X

* This circuit must be provided when the receive tributary channel buffers are situated in the multiplexing part of the multiplexer.

Table 5 (T/CD 02-01). Interface circuits between the Tributary interface conversion unit and the Tributary channel logic (Internal tributary interface).

1.2. 64 kbit/s interface definitions

(a) Internal 64 kbit/s interface (see Figure 1 (T/CD 02-01)).

The internal 64 kbit/s interface is defined by the functional interface circuits as given in Table 6 (T/CD 02-01).

The functional interface circuits may or may not be accessible as a physical interface.

Interface circuit designation	Interface circuit name	Direction from mux.	Direction to mux.
G	Signal ground or common return		
MT	Multiplex channel transmitted data	X	
MR	Multiplex channel received data		X
MST1	Multiplex channel transmitter signal element timing (mux. source)*	X	
MST2	Multiplex channel transmitter signal element timing (64 kbit/s bearer source)*		X
MSR	Multiplex channel receiver signal element timing		X
MLC	Multiplex channel loop control (optional)	X	
MLI	Multiplex channel loop indicator (optional)		X
MA	Multiplex channel received line signal level detectors		X

* At least one of the two must be provided.

Table 6 (T/CD 02-01). Interface circuits between the Multiplexing logic and the Multiplexed interface conversion unit (Internal 64 kbit/s interface).

(b) External 64 kbit/s interface (see Figure 1 (T/CD 02-01)).

Three main variants of the interface exist:

i) a digital interface for direct connection to codirectional or contradirectional interfaces, as defined for access to PCM equipment in CCITT Recommendation G.703;

ii) a digital modem interface according to CCITT Recommendations X.27 (V.11) and V.36;

iii) an analogue line interface as defined by the Multiplexed interface conversion unit.

The Multiplexed interface conversion unit of the multiplexor corresponding to variants i) and ii) above would be PCM or modem adaptors.

In variant iii) the Multiplexed interface conversion unit would be either a 64 kbit/s baseband transmission equipment or a group band modem, both designed to be integrated parts of the data multiplexor.

2. CONTROL OF LOOPS i AND k

The signals for the activating and disactivating procedures are constituted by suitable configuration of bits D (loop characters) of the envelope, with bit S in the OFF status.

The following rules should be complied with:

— in order to perform the loop activation, loop characters are to be sent at least for n consecutive envelopes (proposed value n = 32) and are to be recognized for m consecutive envelopes (proposed value m = 8);

— the loop is held activated as long as two loop characters alternate with two different characters (utilizable as test characters) are sent and recognized;

— the loop is disactivated when the loop characters are not recognized for p consecutive envelopes (proposed value p = 8).

The loop characters have the following configurations:

0 0 1 1 1 1

The test characters can be constituted by a pseudorandom sequence that enables the computation of bit error rate or other parameters.

3. TELEMAINTENANCE OVER A DATA NETWORK USING X.50 FRAME STRUCTURE

The bit S of the envelope is used in two different ways:

— In normal mode, the S bit will be used to report to a maintenance center the status of the subscriber connection specially the following conditions:

  — Normal — S = ON

  — Line failure:
    Subscriber DCE failure
    Subscriber DCE unavailable
    — S = OFF

— During a test procedure, the S bit is multiplexed and permits maintenance information transfer between local and remote DTE/DCE interface. These information are control and supervision signals.

The frame structure of the S bits (Figure 3 (T/CD 02-01)) is as follows:

— The frame is 8 bits long.

— The first bit is the frame synchronisation bit. The transmitted information being nearly static, the frame synchronization pattern is an alternate 1-0 signal.

— The other bits represent the state of DTE/DCE interface circuits:
  — T: when a test equipment is inserted to the DTE/DCE interface, the T bit is set to 1 and when a DTE receives a frame with T bit set to 1, it transmits back a frame with T bit set to 0;
  — 105/109: request to send or carrier detect (V.24);
  — 122, 142: the circuits are not CCITT V.24 and represent the state of the data transmission;
  — 140′: (not V.24) remote loop 2 control;
  — 141′: (not V.24) remote loop 3 control;
  — The last bit is not used and is set to 1.

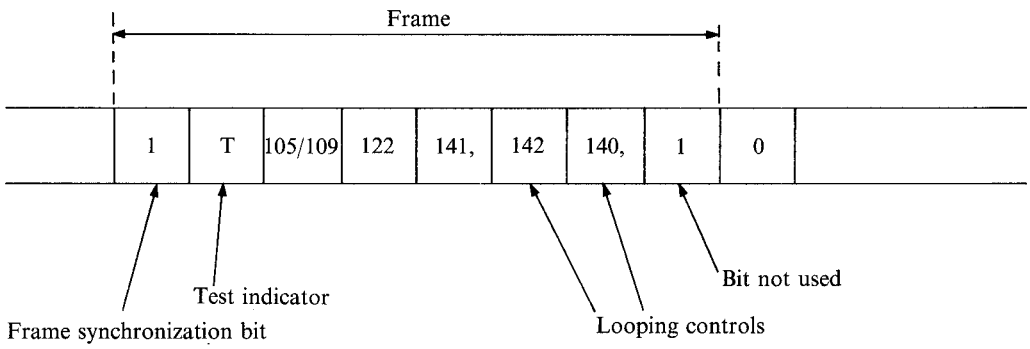


Figure 3 (T/CD 02-01).

Section C. *Optional requirements*

1. INPUT BUFFER REQUIREMENTS

1.1. Tributary side

A buffer should accept, after a slip, a phase variation of the incoming signal of at least ± 1 bit interval, without slips and with a maximum delay of 4 bit intervals.

1.2. 64 kbit/s side

A buffer should accept, after a slip, an incoming signal phase variation of at least X bit intervals, without slips and with a maximum delay of Y bit intervals.

X and Y are under study.

2. EXTERNAL CLOCK INTERFACE (See Figure 1 (T/CD 02-01))

2.1. Specification at the output port (see Table 7 (T/CD 02-01))

Frequency	2,048 kHz ± 50 ppm	
Pulse shape	The signal must conform with the mask (Figure 4 (T/CD 02-01)) The value V corresponds to the maximum peak value The value VI corresponds to the minimum peak value	
Type of pair	Coaxial pair (see *Note* in paragraph 2.2.)	Symmetrical pair (see *Note* in paragraph 2.2.)
Test load impedance	75 Ω resistive	120 Ω resistive
Max. peak voltage	1.5 Vop	1.9 Vop
Minimum peak voltage	750 mVop	1.0 Vop
Maximum jitter at an output port	Under study	

Table 7 (T/CD 02-01).

2.2. Specification at the input ports

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 2,048 kHz should be in the range 0 to 6 dB (minimum value). This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by jitter. The jitter values are under study. The return loss at 2,048 kHz should be $\geqslant 15$ dB.

Note: The outer conductor of the coaxial pair of the screen of the symmetrical pair shall be connected to earth at the output port, and provision shall be made for connecting the outer conductor of the coaxial pair of the screen of the symmetrical pair to earth if required, at the input port.

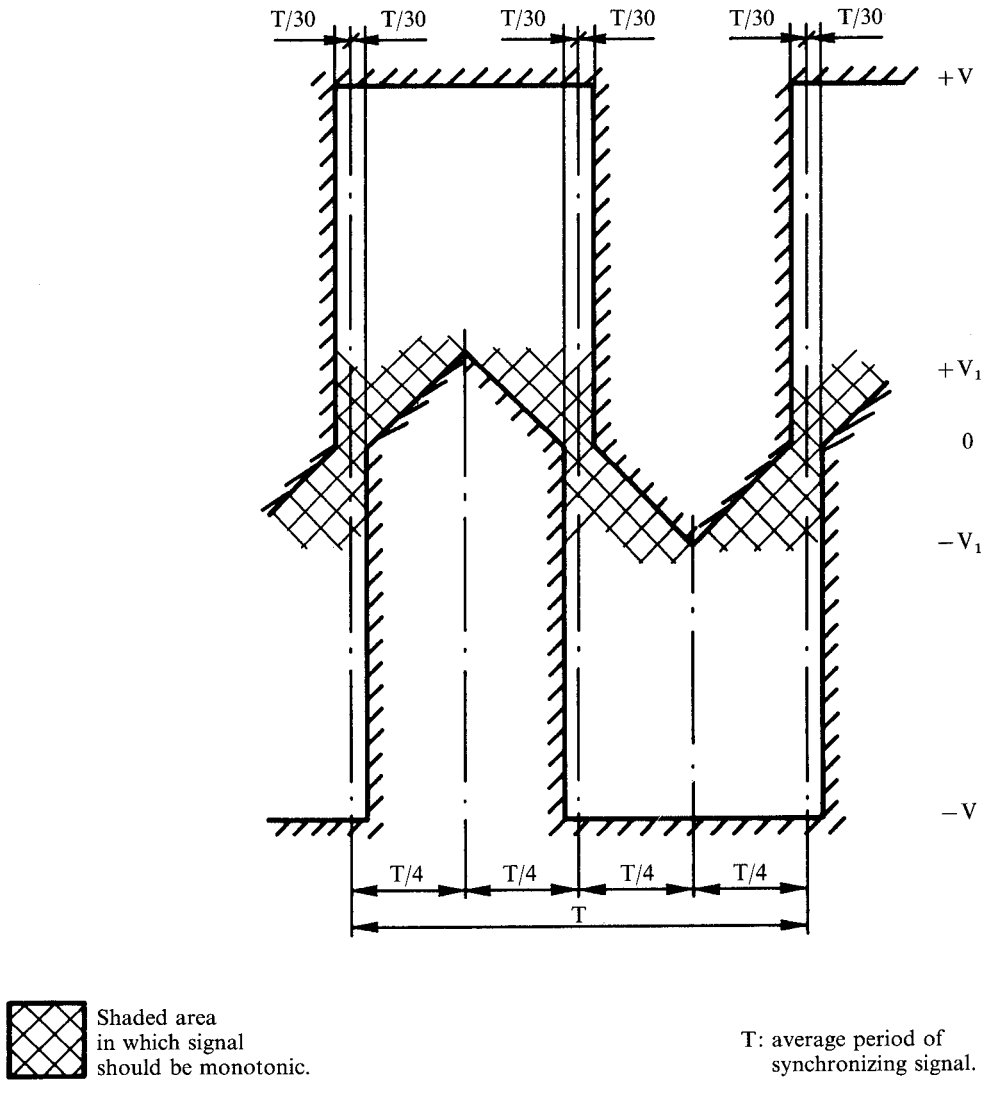


Figure 4 (T/CD 02-01). Wave shape at the output port.