Recommendation T/CD 02-04 (Odense 1986, revised in Edinburgh 1988)

ENGINEERING REQUIREMENTS FOR A SYNCHRONOUS DIGITAL MULTIPLEXER FOR USE WITH NON ENVELOPE STRUCTURED DATA

Recommendation proposed by Working T/WG 10 "Data communications" (CD)

Text of the Recommendation adopted by the "Telecommunications" Commission:

"The Conference of European Post and Telecommunications Administrations,

considering

— that working group CD has studied under the auspices of Question CD 1 the harmonization of Data Circuit Terminating Equipment,

recommends

— that the attached specification of engineering requirements for a synchronous digital multiplexer for use with non envelope structured data as contained in Annex 1 to this Recommendation should be taken into account by all CEPT Administrations when the implementation of a relevant piece of equipment is being planned by Administrations."

Administrations are free to stipulate additional requirements, and also which of the optional requirements, if any, are to be provided.

Note 1. It should be noted that this Recommendation may be revised from time to time.

Note 2. It is left to each Administration to decide which of the three Recommendations i.e. T/CD 02-01, T/CD 02-02 and T/CD 02-04 is to be used in their individual national network.
For international interworking the question of which multiplexer is to be used is a matter of bilateral or multilateral agreement.

Annex 1

SECTION I. PARAMETERS REQUIRED FOR INTERWORKING

I-1. GROSS BIT RATE

The aggregate bit stream shall have a gross bit rate of 64 kbit/s.

I-2. TRIBUTARY CHANNEL BITRATES

The following tributary channel bitrates are supported:
— 2.4 kbit/s
— 4.8 kbit/s
— 9.6 kbit/s
— 19.2 kbit/s
Other bitrates are not excluded.

I-3. MULTIPLEX SCHEME

The multiplex scheme is shown in Figure I-1 (T/CD 02-04). The frame length is 640 bit. The frame duration is 10 ms. Tributary channel data is grouped in octets and appears in slots A_n through F_n. Slots S_n contain synchronisation octets. Slots T_n contain service octets.

160 bits = 20 octets

S1	A1	B1	C1	D1	E1	F1	B2	A2	D2	C2	F2	E2	A3	B3	C3	D3	E3	F3	T1
S2	B4	A4	D4	C4	F4	E4	A1	B1	C1	D1	E1	F1	B2	A2	D2	C2	F2	E2	T2
S3	A3	B3	C3	D3	E3	F3	B4	A4	D4	C4	F4	E4	A1	B1	C1	D1	E1	F1	T3
S4	B2	A2	D2	C2	F2	E2	A3	B3	C3	D3	E3	F3	B4	A4	D4	C4	F4	E4	T4

Figure I-1 (T/CD 02-04). Multiplex scheme.

I-3.1. Data Octets

One frame contains 72 data octets. Thus the multiplex stream can support
24 channels of 2.4 kbit/s, or
12 channels of 4.8 kbit/s, or
6 channels of 9.6 kbit/s, or
3 channels of 19.2 kbit/s, or
combinations thereof.

The allocation of individual octets to a tributary channel is detailed below.

I-3.1.1. *2.4 kbit/s*

2.4 kbit/s tributary channels employ 1 out of 24 data octets. A 2.4 kbit/s channel will thus be allocated to all slots with the same identifier, i.e. identification letter and identification digit (e.g. A1).

I-3.1.2. *4.8 kbit/s*

4.8 kbit/s tributary channels employ 1 out of 12 data octets. A 4.8 kbit/s channel will thus be allocated to all slots with the same identification letter in the range A-F and two different identification digits 1 and 3 or 2 and 4 (e.g. B1 and B3).

I-3.1.3. *9.6 kbit/s*

9.6 kbit/s tributary channels employ 1 out of 6 data octets. A 9.6 kbit/s channel will thus be allocated to all slots with the same identification letter in the range A-F and four different identification digits 1, 2, 3 and 4 (e.g. D1, D2, D3 and D4).

I-3.1.4. *19.2 kbit/s*

19.2 kbit/s tributary channels employ 1 out of 3 data octets. A 19.2 kbit/s channel will thus be allocated to slots with two different identification letters from the range A-F: A and D or B and E or C and F, and four different identification digits 1, 2, 3 and 4 (e.g. C1, F1, C2, F2, C3, F3, C4 and F4).

I-3.1.5. *Other bitrates*

For other bitrates no allocation of octets to a tributary channel is specified. From the scheme in Figure I-1 (T/CD 02-04) it can be derived that any bitrate n times 2.4 kbit/s where n is 1 through 24 can be supported.

I-3.2. **Synchronisation Octets**

One frame contains 4 synchronisation octets. These contain fixed bit patterns as follows:
S1 = 27 = 00100111
S2 = 1B = 00011011
S3 = 05 = 00000101
S4 = 35 = 00110101

Note. Coding of the synchronisation octets is such that they do not overlap; i.e. when in random data one of the synchronisation octets is simulated, no other simulation will occur for 125 μs being the nominal duration of one octet.

I-3.3. **Service octets**

Use of these octets is to be defined. Possible applications are:

— use for exchange of information between the multiplexers concerning tributary channel allocation, routing, maintenance etc.;

— transfer of status information (V.24 105-109 signalling or X.24 C-I signalling) per tributary channel;

— justification.

I-4. **FRAME SYNCHRONISATION**

Frame synchronisation is obtained by the receiving multiplexer during normal operation. No interaction between multiplexers at both ends of the link is required for this purpose.

SECTION II. EQUIPMENT SPECIFICATION

II-1. SYSTEM LAYOUT

The basic multiplexer consists of two different units, tributary channel units (TCUs) and multiplexing units (MUs). See Figure II-1 (T/CD 02-04). Several units of each type constitute a physical multiplexer configuration. The minimum configuration is one MU and one TCU. Specific configurations may be tailored by Administrations depending on the application and can be changed when so required.

Note. Other units may be specified in future.

All units are connected via a bus in accordance with the CEPT BUS SPECIFICATION T/CD 02-05. Structure 2 of this specification is recommended. The basic function of each unit is to receive data from the external interface (tributary channel or aggregate channel), arrange these data into octets, apply these octets together with adequate address information to the bus and vice versa. There shall be no limitation to the possibility to transmit data via the bus to any other unit.

The internal address option of the structure 2 bus is used to identify physical channels in TCUs or logical channels in MUs.

Address information is derived from instructions received from the maintenance system as described in chapter II-5.

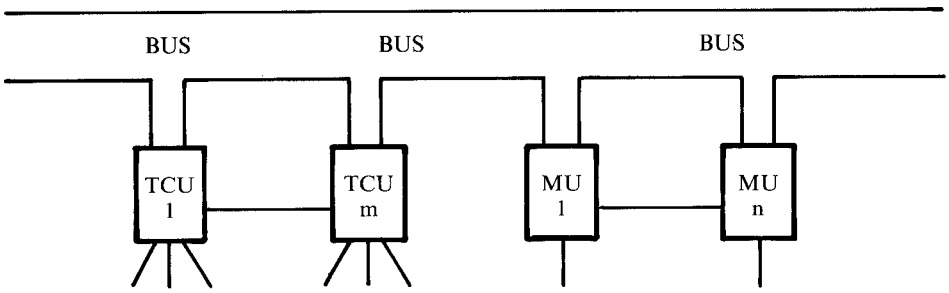


Figure II-1 (T/CD 02-04). System layout.

II-2. TRIBUTARY CHANNEL UNIT

The tributary channel unit (TCU) may support one or more tributary channels. If the unit supports more than one tributary channel, the channel data rates may be:

— identical
— independent within the set 2.4-19.2 kbit/s
— independent within a subset

The TCU will collect data from the tributary channel interfaces, arrange these data into octets and apply these octets together with address information (destination address, consisting of unit address and internal address) to the bus with minimal delay.

Data octets received from the bus will be buffered prior to being transferred to the tributary channel interface in order to allow for the correction of system jitter. A maximum delay of 8 octets is recommended for rates until 9.6 kbit/s. Buffer size for 19.2 kbit/s is for further study. For 2.4 kbit/s a smaller buffer may be advisable.

Channels (= bus internal addresses) are numbered with even numbers starting with 2. Internal address 0 is reserved for maintenance purposes (ref. chapter II-5.).

Maintenance functions of the TCU are described in chapter II-5.

II-3. MULTIPLEXING UNIT

II-3.1. General

The multiplexing unit (MU) will support one 64 kbit/s channel.

The MU will collect data octets from the incoming 64 kbit/s line. Synchronisation octets will be used for framing purposes as described in chapter II-3.2.

Service octets will be used for maintenance purposes as described in chapter II-5.

Data octets will be applied to the bus with minimal delay together with address information (destination address, consisting of unit address and internal address).

Data octets received from the bus will be buffered prior to being transferred to the 64 kbit/s channel interface in order to allow for the correction of system jitter. Buffering may be employed on a per channel basis or via a common buffer for all channels. Recommended delay is between 5 and 15 ms.

Logical channels (= bus internal addresses) are numbered with even numbers starting with 2. Internal address 0 is reserved for maintenance purposes (ref. chapter II-5.).

Allocations of time slots to logical channels is described in chapter II-5.

Maintenance functions of the MU are described in chapter II-5.

Timing functions of the MU are described in chapter II-6.

II-3.2. Frame alignment

II-3.2.1. *General requirements*

— The frame synchronisation method should be insensitive as far as possible to bit errors, error bursts, and short bursts of AIS generated by transmission equipment.

— When a slip occurs in the transmission equipment, a fast frame alignment recovery must be possible.

II-3.2.2. *Framing method performance*

— The frame alignment recovery time after a slip, in the absence of bit errors and with random data in all channels, should be less than 160 octets (2 frames) with 95% probability.

— A random error ratio of 1 in 10^{-4} shall not cause any frame alignment recovery action.

— When the unit loses synchronisation, e.g. due to the synchronisation pattern no longer being present in the incoming bit stream, the unit will enter the loss of synchronisation state after 50 ms (minimum) to 100 ms (maximum).

II-3.3. Consequent action in case of loss of synchronisation

When the MU is in the loss of synchronisation state it should transmit to the bus at least 24 octets containing all logical ones in all logical channels that are active. After that, the MU will continue to send these octets or cease sending octets in logical channels completely.

Indication of this state to the maintenance system is described in chapter II-5.

II-4. INTERFACES

Three different interfaces may be identified in the multiplexer, i.e. the tributary channel interface, the 64 kbit/s channel interface and the bus interface.

II-4.1. Tributary channel interface

Three different types of interface are envisaged.

II-4.1.1. If the tributary channel modem is integrated in the TCU, the interface will comply with the respective modem recommendation.

II-4.1.2. If the tributary channel modem is not integrated in the TCU, the interface towards the modem is a "normal" DTE-DCE interface.

The following circuits are considered to be essential:

102 (a, b, c)	Signal Ground(s)	
103	Transmit Data	to DCE
104	Receive Data	from DCE
109	Received Line Signal Detector	from DCE
113	Transmitter Signal Element Timing (DTE source)	to DCE
115	Receiver Signal Element Timing (DCE source)	from DCE
141	Local Loopback	to DCE

Electrical characteristics may be V.28 or other, depending on the nature of the modem.

II-4.1.3. If the DTE is interfaced directly to the multiplexer, a V.24/V.28 interface is required in which the multiplexer simulates a DCE. Details of this interface are under study.

II-4.2. The 64 kbit/s channel interface

The interface towards the 64 kbit/s channel will be in accordance with CCITT Recommendation G.703 paragraph 1. Additionally interfaces according to CCITT Recommendations V.35 and/or V.36 may be required.

II-4.3. The bus interface

The bus interface is in accordance with the CEPT BUS SPECIFICATION T/CD 02-05, structure 2 with some limitations:

— The Central Controller will issue BUS REQUEST STROBES while polling all units present or potentially present in the system. When the polled unit responds via the BUS SEIZED line, the Central Controller will issue an ADDRESS STROBE, followed by an INTERNAL ADDRESS STROBE, followed by a DATA STROBE, followed by a bus release action.

— Only write actions are envisaged. Thus the Central Controller will keep the WRITE line permanently in the active state.

— The duration of a complete poll is equal to or greater than 1 μs.

The following additional circuits are used:

Name	Abbreviation	Direction
UNIT ADDRESS	UA7-UA0	to unit
256 kHz CLOCK	256 kHz	to unit
19.2 kHz CLOCK	19.2 kHz	to unit
CLOCK SYNCHRONISATION	CS	from unit (MU only)

The UNIT ADDRESS lines contain the 6 bit address of the unit (see chapter II-9.).

The 256 kHz CLOCK line contains a 256 kHz clock signal (see chapter II-6.).

The 19.2 kHz CLOCK line contains a 19.2 kHz clock signal (see chapter II-6.).

The CLOCK SYNCHRONISATION line contains a signal derived from the incoming 64 kbit/s signal. Transitions in this signal occur at time intervals which are multiples of 1/256 ms.

II-5. MAINTENANCE

II-5.1. General

The maintenance of the multiplexer is performed under control of a maintenance system. This system is not described in this specification, which is limited to maintenance functions to be performed by multiplexers and multiplexer components.

II-5.2. Information transfer

The maintenance system issues instructions to units anywhere in the network. Units answer these instructions with responses. The maintenance system can enter the multiplexer network at one or various locations via a dedicated channel in a TCU, which operates at a fixed data rate of 2,400 bit/s. Messages containing instructions or responses flow via buses (internal address 0) and 64 kbit/s multiplexer channels (service octets) from maintenance system entrance to units and vice versa. Details on the protocol between the maintenance system and the TCU at its entrance point and between MUs (link layer protocol), the routing of messages through the network (network layer protocol) and the coding of instructions and responses are described in Appendix I.

II-5.3. Configuration Control

Each unit is provided by the maintenance system with information concerning the configuration. In the case of MUs, for each logical channel the following information is provided:
— whether or not the channel is active,
— number of first time slot,
— data rate,
— destination address (unit address + internal address).

In the case of TCUs, for each physical channel the following information is provided:
— whether or not the channel is active,
— data rate,
— destination address (unit address + internal address).

II-5.4. Alarms

Units may detect alarm situations in the unit itself or in associated equipment. This information is transferred to the maintenance system in responses.

In the case of MUs, alarms comprise:
— loss of synchronisation,
— loss of incoming signal.

In the case of TCUs alarms comprise:
— loss of incoming carrier (for each channel separately).

II-5.5. Testing

Units can be instructed to establish test loops in the lines they control. Loop control may be via circuits 140-142 when available. Alternatively, when these circuits are not available, the unit will take over the responsibility of the loop originating DCE and generate and monitor patterns according to CCITT Recommendation V.54.

Loop tests may be either simple point to point (tributary channel, 64 kbit/s channel with two modems) or tandem with addressing capability (more complex 64 kbit/s channels). Which loop is applicable is derived from the instruction the unit receives.

Instructions may either command the mere establishment of loops or command a complete loop test to be performed by the unit itself including emission and evaluation of a test pattern and presentation of the results in a subsequent response.

The TCU will not apply loops in more than one channel simultaneously.

Channels that have been tested will be reprogrammed after the test.

II-6. TIMING

Timing of a multiplexer configuration is derived from one of the incoming 64 kbit/s channels. Each MU will derive timing from its incoming 64 kbit/s signal. The 64 kHz timing signals derived by the two units situated most closely to the central controller will be passed to the central controller. The central controller will evaluate whether these two signals are present and use the signal from the first unit, if available to synchronize a system clock. If this signal is not avaiblable, the central controller will use the timing signal of the second unit. If both signals fail, the system clock will be running free.

The system clock is passed to all units in the configuration in the form of two synchronized timing signals, one operating at 256 kHz, the other at 19.2 kHz. All units will control their output channels with one of these timing signals.

II-7. PERFORMANCE

Jitter performance at the 64 kbit/s interface is as described in CCITT Recommendation G.823.

Jitter performance of the tributary channel interface is for further study.

Error performance of the system should be such that no bit errors occur in a free standing mutliplexer for at least one hour.

II-8. POWER CONSUMPTION

All unit will operate from a single +5 V power supply. Maximum supply current for each unit is 1.2 A provided the interfaces are not connected. In case electrical characteristics according to V.28 are required, additional power supplies for + and −12 V are used. Maximum supply currents for these supplies: 300 mA.

II-9. CONSTRUCTION

Units are type II cards (CEPT Recommendation T/CD 01-14 on Equipment Practice). Their spacing is 6 HP. Pin allocation of the DIN 41612 connector is as specified in T/CD 02-02 with additional pins reserved for timing and position identification purposes. (Ref. Table II-1 (T/CD 02-04)). A second DIN 41612 connector (64 or 96 way) is mounted in the other half of the card and contains all the interface circuits to the transmission facilities.

A maximum of eight units can be mounted in a shelf. At the right hand side of the shelf, a power supply unit is mounted (spacing: 21 HP). At the left hand side a unit is mounted that can be used either as central controller or as bus repeater. The spacing of this unit is 15 HP.

The bus address of a unit is position dependent. The least significant three address bits are determined by the position in the shelf. The other bits are determined by the position of the shelf in the rack. Units determine their address by the code they find on the UNIT ADDRESS pins in the connector (the two most significant bits are zero).

	A	B	C
1	0 V	0 V	0 V
2	DA0		
3	DA1		
4	DA2		
5	DA3		
6	DA4		
7	DA5		
8	DA6		
9			
10	DA7		
11	BR		
12	BRS		
13	AS		
14	DS		
15	IAS		
16	BS		
17			
18	DAS		
19	WR		
20	256 kHz		CS
21	19.2 kHz		
22	UA0		UA1
23	UA2		UA3
24	UA4		UA5
25			
26			
27	−12 V	−12 V	−12 V
28	+12 V	+12 V	+12 V
29	+5 V	+5 V	+5 V
30	+5 V	+5 V	+5 V
31	0 V	0 V	0 V
32	0 V	0 V	0 V

Table II-1 (T/CD 02-04). Pin Allocation.

Appendix I

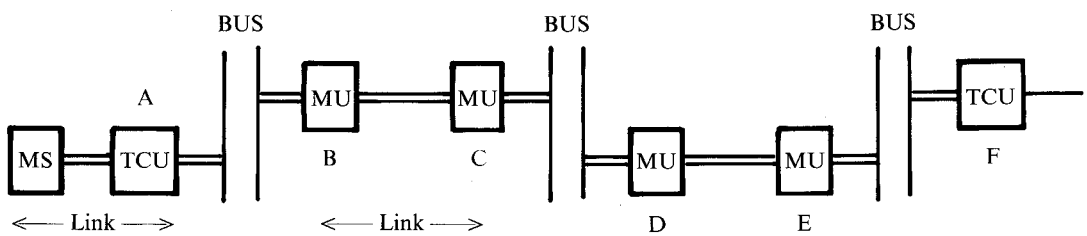
MAINTENANCE PROTOCOLS

Note. See the abbreviations list at the end of this Appendix.

A.I-1. GENERAL

Every unit (TCU, MU) can be reached by the maintenance system (MS). The route to the unit is described in the block that is sent to the unit by the MS. Blocks that are sent back by the unit to the MS, do not contain any routing information. Every unit knows the route to the OC.

Blocks are provided with a BCS. Protection is per link. In this respect a link is a 64 kbit/s path or the path between maintenance system and its TCU (see figure).



Units are polled. Reception of a block from the MS is also seen as an invitation to indicate the status of the unit itself.

A.I-2. LINK LAYER (2)

A.I-2.1. Reference

The link layer protocol described here is an implementation of ISO R1745.

A.I-2.2. Block structure

A block has the following structure:
DLE STX <information> DLE ETX BCS

A.I-2.3. Conventions

— BCS
In accordance with ISO 2111; "code independent transmission procedures".

— Transparence
In accordance with ISO 2111; "code independent transmission procedures".

— Acknowledgement
Blocks received correctly are acknowledged alternatingly with DLE 0 and DLE 1. Blocks received incorrectly are responded with NAK.

— Retransmission
After reception of NAK a block is repeated. Maximum number of repetitions: 2.

— Time-out
If acknowledgement is not received in time, the receiver is requested by an ENQ from the transmitter to repeat the last transmitted acknowledgement. When in that case NAK is received or a DLE with a wrong number then the block is repeated (maximum 2 times). Maximum number of ENQ's for one block: also 2.

— Bus
With transmission over the bus a BCS in accordance with ISO 2111 is added and no acknowledgement is transmitted.

— Duplex
The protocol operates duplex at this layer; i.e. information transfer in both directions is independent.

— Parity
All control characters are transmitted with odd parity.

— Initiation
The link MS-TCU is initiated as follows: At an OFF-ON transition of circuit 109, the TCU will start searching for octet synchronisation from the received SYN characters. Afterwards the MS will send an ENQ character. The TCU will respond with DLE 0.

A.I-3. NETWORK LAYER (3)

A.I-3.1. Structure

The information field of the block of layer 2 is coded as follows:
<address field> <instruction field>

— Address field
Consists of 3 or more octets. The first octet contains the number of addresses in the field. The second octet contains an address pointer. The following octets contain the successive addresses of the units to be passed. E.g. for the structure shown in the figure: 6 0 A B C D E F to reach unit F. The MS sends this block first to A. A increases the address pointer (1) and sends the block to B. B increases again the address pointer (2) and sends the block via the bus to unit C, etc. Blocks with an address field, of which the first two octets are equal, are intended for the MS. Every unit derives the direction in which the MS is to be found from the addressfield of the message passed.

— Instruction field
See description of instruction layer.

A.I-4. INSTRUCTION LAYER

The instruction field is coded as follows:
<instruction code> <parameter field>

The instruction code is constructed as follows:
— bit 7: 0 = instruction (from the MS)
1 = response (to the MS)
— bit 6-3: type number of the unit: TCU (0), MU (1), ...
— bit 2-0: number of the instruction/the response

For the time being the following instructions and responses are foreseen:

(a) TCU; instruction 1.
Instruction code: 00 (hex)
Parameter field:
25 octets; the first octet is not used. After that 8 groups of 3: respectively destination address (unit) for each channel, channel number within that unit and the status. The status is coded as follows:
— bit 7-6: 00 = 2,400 bit/s
01 = 4,800 bit/s
10 = 9,600 bit/s
11 = 19,200 bit/s
— bit 5-4: 00 = no action
01 = establish loop 3
10 = test tributary channel with loop 2
11 = test tributary channel with loop 3
— bit 3-1: not used
— bit 0: channel active
If a channel is no in use the combination FF FF 00 is recommended.

(b) TCU; instruction 2 (short poll for instruction code 00).
Instruction code: 01 (hex)
Parameter field:
1 octet; not used (=00).

(c) TCU; response 1.
Instruction code: 80 (hex)
Parameter field:
26 octets; the first octet is not used. After that 8 groups of 3: respectively destination address (unit) for each channel, channel number within that unit and the status.

The status is coded as follows:
— bit 7-6: 00 = 2,400 bit/s
01 = 4,800 bit/s
10 = 9,600 bit/s
11 = 19,200 bit/s
— bit 5-4: 00 = no test active
01 = loop 3 established
10 = tributary channel test with loop 2 busy/ready
11 = tributary channel test with loop 3 busy/ready
— bit 3: DTE interface
— bit 2: test ready or loop established (see bit 5-4)
— bit 1: circuit 109 OFF
— bit 0: channel active

The last octet contains the number of wrong octets in 256 transmitted octets in a channel that has been tested (bit 2 = 1).

(d) TCU; response 2 (answer short poll 01 (hex))

Instruction code: 81 (hex)

Parameter field:
11 octets: the first octet is not used (= 00), the 8 status octets for the channels 0 to 7. The octets 10 and 11 contain the BCS, according to ISO 2111, over the parameter field of 25 octets of instruction 00. The status is coded in the same way as in intruction 00.

(e) TCU; response reject

Instruction code: 87 (hex)

Parameter field:
3 octets; the first octet is not used. The second octet contains the software version number of the unit. The third octet is reserved for an errorcode.

(f) MU; instruction 1.

Instruction code: 08 (hex)

Parameter field:
3 n + 1 octets; in which n is the number of channels that is realised (max. 24). The first octet is not used. After that n groups of 3 octets follow. The first and second octet of every group contain the destination address of the channel. The third octet of every group contains the slot number (0-23) of the first timeslot in the frame of this channel (bit 4-0) and the channel data rate (bit 7-6).

Timeslot numbers are coded as follows:

	A	B	C	D	E	F
1	0	1	2	3	4	5
2	6	7	8	9	10	11
3	12	13	14	15	16	17
4	18	19	20	21	22	23

Coding of channel speed:
00 = 2,400 bit/s
01 = 4,800 bit/s
10 = 9,600 bit/s
11 = 19,200 bit/s

(g) MU; instruction 2 (loop test instruction).

Instruction code: 09 (hex)

Parameter field:
2 octets; the first octet is not used. The second octet contains the V.54 address of the loop in the 64 kbit/s path over which a test is to be carried out ("FF" = an unnumbered loop; "00" is the loop in the MU itself). After the loop test the unit is to be restarted via an instruction 1 or 3.

(h) MU; instruction 3 (64 kbit/s transparent).

Instruction code: 0A (hex)

Parameter field:
3 octets; the first octet is not used. The second and third octet contain the destination address of all octets of the 64 kbit/s channel.

(i) MU; instruction 4 (short poll for instruction code 08 (hex)).
Instruction code: 0B (hex)
Parameter field:
1 octet; not used (= 00).

(j) MU; response 1.
Instruction code: 88 (hex)
Parameter field:
3 n + 2 octets; the first 3 n + 1 identical to the parameter field of instruction 1. The last octet is coded as follows:
— bit 7-2: not used
— bit 1: no incoming signal
— bit 0: sync loss

(k) MU; response 2.
Instruction code: 89 (hex)
Parameter field:
4 octets; the first two octets are identical to the parameter field of instruction 2. The third octet contains the number of octets received in error during the test. The fourth octet contains the number of octets transmitted during the test. If the establishment of the loop is not successful, the third octet will contain "FF" and the fourth "00".

(l) MU; response 3.
Instruction code: 8A (hex)
Parameter field:
4 octets; the first three octets are identical to the parameter field of instruction 3. The last octet is coded as follows:
— bit 7-2: not used
— bit 1: no incoming signal
— bit 0: not used

(m) MU; response 4 (answer short poll 0B (hex)).
Instruction code: 8B (hex)
Parameter field:
4 octets: the first is not used (= 00), the second contains the status from response 80 (hex), the third and fourth octet contain the BCS, according to ISO 2111, over 3 n + 1 octets of the parameter field.

(n) MU; response reject.
Instruction code: 8F (hex)
Parameter field:
3 octets: the first octet is not used. The second octet contains the software version number of the unit. The third octet is reserved for an errorcode.

Abbrevation list

BCS	block control signal
BSC	binary synchronous control
CRC...	cyclic redondancy check...
DLE	data link escape
ENQ	enquiry
ETB	end transmission block
ETX	end of text
hex	hexadecimal
MS	maintenance system
MU	multiplexing unit
NAK	negative acknowledgment
OC	originating call
STX	start of text
SYN	synchronisation
TCU	tributary channel units
TE	terminal equipment