**Recommendation T/CD 02-05 (Odense 1986)**

# ENGINEERING REQUIREMENTS FOR A BUS INTERFACE TO BE USED IN DATA COMMUNICATION EQUIPMENT

Recommendation proposed by Working Group T/WG 10 "Data communications" (CD)

*Text of the revised Recommendation adopted by the "Telecommunications" Commission:*

"The Conference of European Post and Telecommunications Administrations,

*considering*

— that working group CD has studied under the auspices of Question CD 1 the harmonization of Data Circuit Terminating Equipment,

*recommends*

— that the attached specification of engineering requirements for a bus interface to be used in data communication equipment as contained in Annex 1 to this Recommendation should be taken into account by all CEPT Administrations when the implementation of a relevant piece of equipment is being planned by Administrations."

Administrations are free to stipulate additional requirements, and also which of the optional requirements, if any, are to be provided.

*Note 1.* It should be noted that this Recommendation may be revised from time to time.

## Annex 1

## 1. SCOPE

This specification is generally applicable for use within data communication systems. Its application for specific equipment will be defined in relevant equipment specifications. These equipment specifications may also indicate which specific structures or options apply for that equipment.

## 2. SYSTEM LAYOUT

Three different structures are described in this specification. Selection of one of these structures is dependent on the application.

— Structure I consists of one bus master unit connected to a number of bus slave units.

— Structure II consists of a CENTRAL CONTROLLER connected to a number of units, some or all of which have the capability of becoming bus master, under control of the CENTRAL CONTROLLER.

— Structure III consists of a number of interconnected units, some or all of which have the capability of becoming bus master. Units negotiate this via a separate bus.

*Note.* Units that do not have the capability to become bus master can be used in all three structures.

## 3. FUNCTIONAL CHARACTERISTICS

The bus consists of a number of lines as listed in Table 1 (T/CD 02-05).

| Name | Abbr. | Struct. | Type | Status |
|---|---|---|---|---|
| *Transfer control* | | | | |
| ADDRESS STROBE | AS | 1, 2, 3 | TP/TS | essential |
| DATA STROBE | DS | 1, 2, 3 | TP/TS | essential |
| WRITE | WR | 1, 2, 3 | TP/TS | essential |
| INTERNAL ADDRESS STROBE | IAS | 1, 2, 3 | TP/TS | optional |
| DATA/ADDRESS SOURCE | DAS | 1, 2, 3 | OC | optional |
| *Master control* | | | | |
| BUS REQUEST STROBE | BRS | 2, 3 | TP/TS | essential |
| BUS SEIZED | BS | 2, 3 | OC | essential |
| BUS RELEASE | BR | 2 | TP | essential |
| PRIORITY | PR7-PR0 | 3 | OC | essential |
| *Maintenance* | | | | |
| RESET | RES | 1, 2, 3 | | for further study |
| HALT | HT | 1, 2, 3 | | for further study |
| PERIPHERAL CONTROL | PER | 1, 2, 3 | | for further study |
| SYSTEM CONTROL | SYS | 1, 2, 3 | | for further study |
| *Data/address* | | | | |
| DATA/ADDRESS | DA7-DA0 | 1, 2, 3 | TS | essential |
| ADDRESS | A15-A8 | 1, 2, 3 | TS | optional |
| *Additional* | | | | |
| — | — | — | — | for further study |

Table 1 (T/CD 02-05). Bus lines.

*Note.* For explanation of the column "type" refer to section 5 of this specification.

The *ADDRESS STROBE* line validates the signals on the DATA/ADDRESS lines DA7-DA0 and potentially A15-A8 as an address. The line is controlled by the bus master or by the CENTRAL CONTROLLER (structure II).

The *DATA STROBE* line validates the signals on the DATA/ADDRESS lines as data. The line is controlled by the bus master or by the CENTRAL CONTROLLER (structure II).

The *WRITE* line determines whether a transfer action is a read or a write action. The line is controlled by the bus master or by the CENTRAL CONTROLLER (structure II).

The *INTERNAL ADDRESS STROBE* line validates the signals on the DATA/ADDRESS lines as an internal address. The line is controlled by the bus master or by the CENTRAL CONTROLLER (structure II).

The *DATA/ADDRESS SOURCE* line is used to control repeaters in extended bus systems. The line is activated by the unit that activates the DATA/ADDRESS and/or ADDRESS lines.

The *BUS REQUEST STROBE* line
— in structure II validates the signals on the DATA/ADDRESS and ADDRESS lines as a bus request poll address. The line is controlled by the CENTRAL CONTROLLER;
— in structure III validates the signals on the PRIORITY and BUS SEIZED lines. This line is controlled by the master unit.

The *BUS SEIZED* line
— in structure II indicates that a unit has seized the bus and thus become bus master;
— in structure III validates a bus request on the priority lines and initializes the transmit address procedure.

The line is controlled by the master unit.

The *BUS RELEASE* line indicates to a unit that it shall release the bus and thus cease to be the bus master. The line is controlled by the CENTRAL CONTROLLER (structure II).

The *PRIORITY* lines determine which unit may become bus master. The line is controlled by all units wishing to become bus master.

The function of the *RESET*, *HALT*, *PERIPHERAL CONTROL* and *SYSTEM CONTROL* lines is under study.

The *DATA/ADDRESS* lines are multifunctional lines. Their function is determined by signals on STROBE lines.

The *ADDRESS* lines contain the most significant octet of an address when validated by the ADDRESS STROBE line.

Additional lines may be defined for specific applications. Study is underway to determine whether some of these lines can be harmonized.

## 4. BUS PROCEDURES

### 4.1. Transfer Control

The transfer control procedure is identical for all structures. Transfer actions consist of two or three different phases, the address phase, the optional internal address phase and the data phase.

#### 4.1.1. *Address phase*

In this phase the bus master will apply a two octet address to the ADDRESS lines (most significant octet) and the DATA/ADDRESS lines (least significant octet). The master unit or the CENTRAL CONTROLLER will activate the ADDRESS STROBE line. A unit responding to the address will enter the read/write active mode.

Systems, not requiring more than 256 different addresses, will not implement the optional ADDRESS lines.

#### 4.1.2. *Internal address phase*

In this optional phase, the bus master will apply the internal address to the DATA/ADDRESS lines. The master unit or the CENTRAL CONTROLLER will activate the INTERNAL ADDRESS STROBE. The unit being in the read/write active mode will accept the internal address and regard subsequent data transfer actions as pertinent to this internal address. The internal address could, e.g. indicate a modem on a multiple modem unit or a timeslot in a multiplexer unit, etc.

#### 4.1.3. *Data phase*

The procedure during this phase depends on whether the action is a read or a write action.

4.1.3.1. Read action

During a read action the master unit or the CENTRAL CONTROLLER will activate the DATA STROBE line. The master unit will not activate the write line. The unit(s) being in the read/write active mode will apply a data octet to the DATA/ADDRESS lines.

4.1.3.2. Write action

During a write action the master unit or the CENTRAL CONTROLLER will activate the DATA STROBE line. The master unit will activate the write line and apply a data octet to the DATA/ADDRESS lines. The unit(s) being in the read/write active mode will receive the data octet.

4.1.4. *Detailed procedure*

The sequence of address, internal address and data phases is defined as follows:

A complete sequence consists of one or more address phases followed by one or more secundary phases. A secundary phase consists of zero or more internal address phases followed by one or more data phases. Units will leave the read/write active mode at the end of a complete sequence; i.e. when a data phase is followed by an address phase. Internal addresses are released at the end of a secundary phase; i.e. when a data phase is followed by an internal address phase.

Also a bus release action (structure II) or a new request (structure III) may cause units to leave the read/write active mode.

## 4.2. Master control

4.2.1. *Master control for structure II*

The following actions are specified:
— Bus grant action.
— Bus release action.

4.2.1.1. Bus grant action

The CENTRAL CONTROLLER will apply the address of a unit to the DATA/ADDRESS and ADDRESS lines and activate the BUS REQUEST STROBE line. The unit, recognizing its address will, when it wishes to become bus master, respond by activating the BUS SEIZED line. As long as this line remains activated, the unit is bus master.

Systems, not requiring more than 256 different addresses, will not implement the optional ADDRESS lines.

4.2.1.2. Bus release action

Units may cease to be bus master in one of the following ways:
— de-activation of the BUS SEIZED line by the unit;
— activation of the BUS RELEASE line by the CENTRAL CONTROLLER.

4.2.2. *Master control for structure III*

*Note 1.* Only units having an address equal to or less than 255 can become bus master in this structure.

*Note 2.* Specific precautions may be required for start-up conditions.

Bus grant negotiation takes place on a separate set of lines (BUS REQUEST STROBE, BUS SEIZED and PRIORITY) simultaneously with transfer actions on other lines. The action is divided into two phases:
1. to detect the level of priority defined by each unit on its own;
2. to choose a unit between all units with the same level of priority.

4.2.2.1. Priority determination

Each unit wishing to become bus master sends its level of priority on one of the PRIORITY lines while activating the BRS and BS lines. A unit detecting a higher priority on the lines than its own will withdraw. After some time only those units having the highest priority will remain active.

The way in which units determine their level or priority is not specified. Priority may depend on:
— the message priority;
— the message type;
— the duration since the last message was sent, etc.

4.2.2.2. Address determination

In this phase only those units participate that have the highest priority. During this phase units will send their address on the PRIORITY lines. The procedure is then identical with that in the previous phase (only the BRS line is used).

The unit address is defined by 8 bits. Each unit will translate its address in three codes:
— one for the most significant two bits;
— one for the following three bits;
— one for the least significant three bits.

The decimal value of the three groups of bits (0-7) will correspond to the decimal designation order of one of the PR0-PR7 lines. Each unit sends the first code and withdraws if necessary. The same procedure is applied for all three codes.

So, after 4 clock cycles on BRS, the new master is appointed.

Optionally, each unit is able to detect the new master, but for more reliability, the previous master will send the address of the new master on the DATA/ADDRESS and/or ADDRESS lines validated by a BUS REQUEST STROBE.

### 4.3. Options

Not all units present in a system will necessarily be capable of performing all actions described in this section. Depending on the application units may, e.g. implement or not implement the following capabilities:
— become the bus master;
— write as a bus master;
— read as a bus master;
— go into the read/write active mode;
— write action in the read/write active mode;
— read action in the read/write active mode.

## 5. ELECTRICAL CHARACTERISTICS

In this section only the receiver characteristics are described in detail. Driver characteristics will depend on
— the number of receivers to be driven;
— the transfer rate;
— the presence of bus terminations.

### 5.1. Drivers

Drivers may be of the following type
— Totem-pole (TP)
— Open collector (OC)
— Three state (TS)

Which type is applicable for which line is indicated in Table 1 (T/CD 02-05).

The following characteristics apply
— high level output current $< 50\ \mu A$ at $Vo = 2.4$ V three state off;
— low level output current $> -50\ \mu A$ at $Vo = 0.6$ V three state off;
— output capacitance Cout $< 15$ pF.

### 5.2. Receivers

Receivers shall meet the following characteristics:
— Low level input current $> -400\ \mu A$ at $Vi = 0.5$ V
— High level input current $< 50\ \mu A$ at $Vi = 2.7$ V
— Threshold voltage $0.8\ V < Vt < 2.0\ V$
— Input capacitance $Cin < 7$ pF

### 5.3. Transceivers

Transceivers shall meet requirements of drivers and receivers. The total load capacitance, however, is limited to 18 pF.

### 5.4. Repeaters

As the fan-out of drivers is limited, repeaters are required in larger bus-systems. To minimize delay, a set-up as given in Figure 1 (T/CD 02-05) is recommended.

The direction in which the DATA/ADDRESS and ADDRESS lines are repeatered is determined by the DATA/ADDRESS SOURCE line. This line itself will not be repeatered.

*Note.* Repeater set-ups for structure III require further study.

The electrical characteristics of the bus between the CENTRAL CONTROLLER (if present) and the repeaters is for further study. Study in CCITT Study Group XVII concerning a multipoint version of Recommendation V.11 ("V.12") is to be considered.

## 6. BUS TIMING

To ensure proper operation of a bus system based on this specification, the following general rules should be observed.

All the control lines are in the logical "1" condition when not activated. When a STROBE line moves to the logical "0" condition (active state), the unit which is responsible for the DATA/ADDRESS and ADDRESS lines during this phase can activate these lines. When after a certain time the control line moves back to the logical "1" conditions, the information on the DATA/ADDRESS and ADDRESS lines has to be valid.

*Note.* It should be noted that in larger systems there will be a delay (propagation delay and delay due to repeaters) between the instant in which a unit activates a line and the instant in which all other units in the system recognize this change in condition. This should be taken into account when designing systems and system components.

The reaction times and thus the minimum required duration of the active states of the control lines are for the time being not specified. Further study is required to determine whether such times are to be specified, and if so, whether a unique value for all applications is to be preferred or that several classes of equipment, each with their own requirements should be introduced.

Figures 2 (T/CD 02-05) - 8 (T/CD 02-05) show the basic timing arrangements for:

— an address phase;
— an internal address phase;
— a read action;
— a write action;
— a bus grant action (structure II);
— a bus release action; unit initiative (structure II);
— a bus release action; CENTRAL CONTROLLER initiative (structure II).

Timing arrangements for structure III are to be defined.

## 7. MECHANICAL CHARACTERISTICS

The physical dimensions of a unit are those specified for type II or III cards in the draft CEPT specification of equipment practice for Data Transmission Equipment (T/CD 01-14), the latter type being under study. The connector and its position are as specified there. An additional connector, for the time being unspecified, may be provided for "non-bus" purposes.

The pin allocation is provided in Annex A.

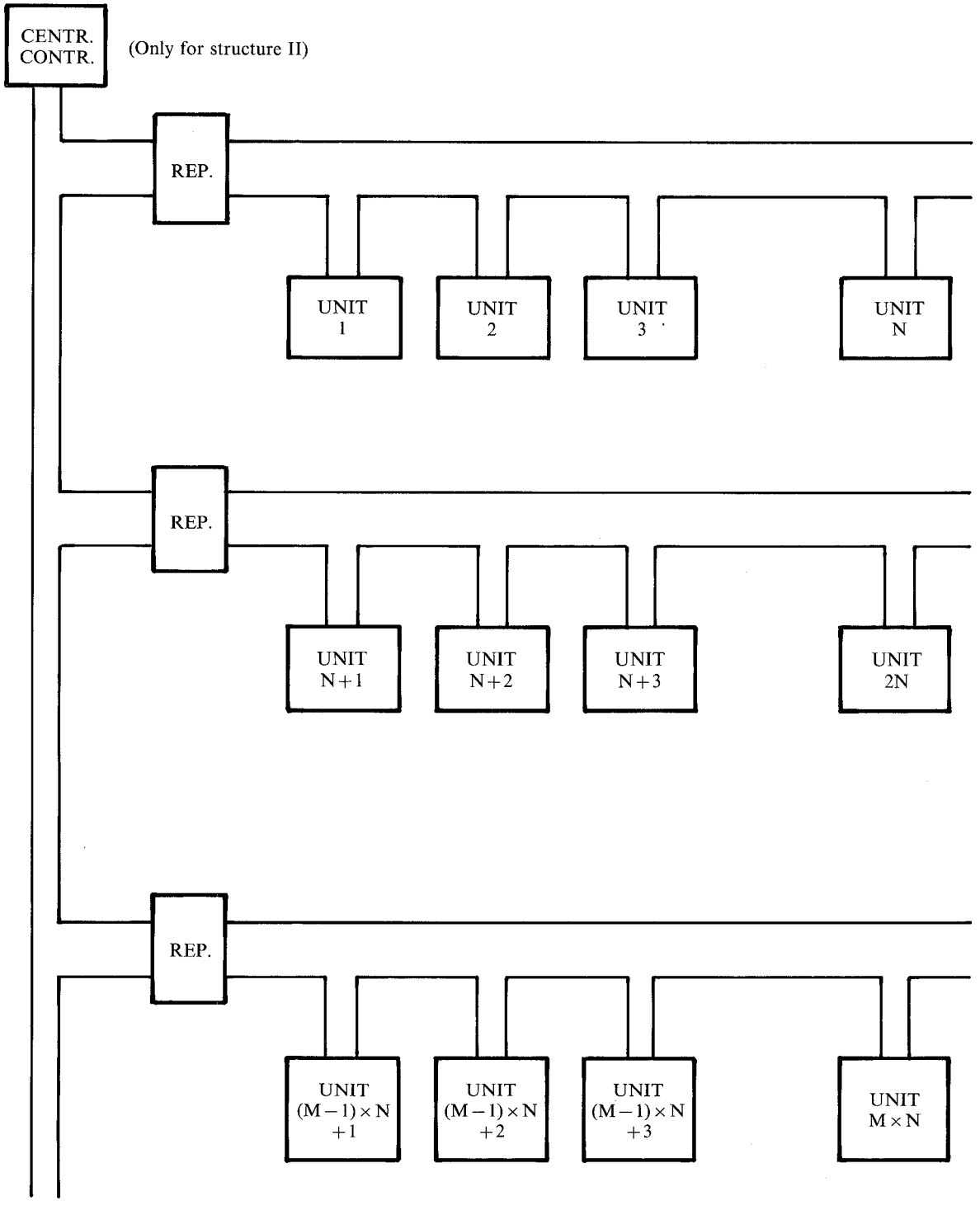
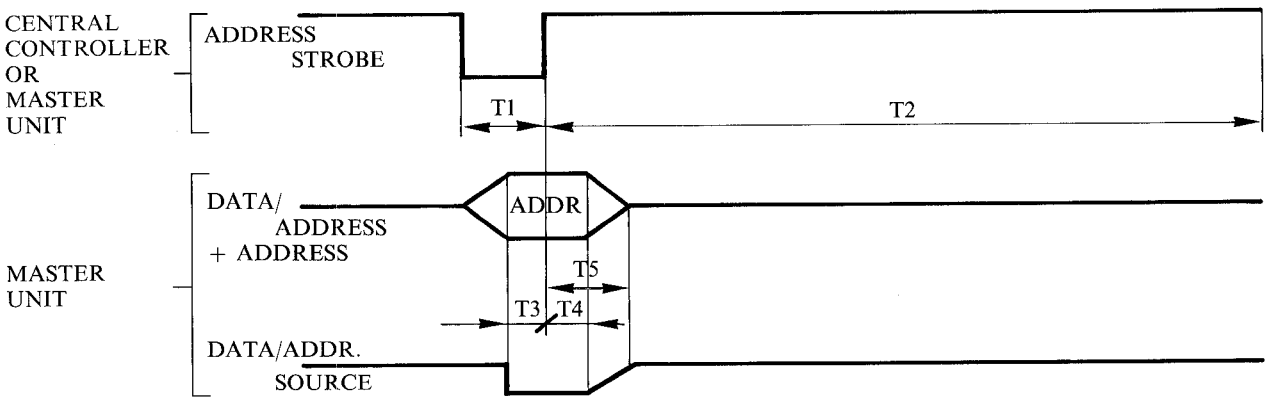



Figure 1 (T/CD 02-05). Recommended set-up for larger bus systems.



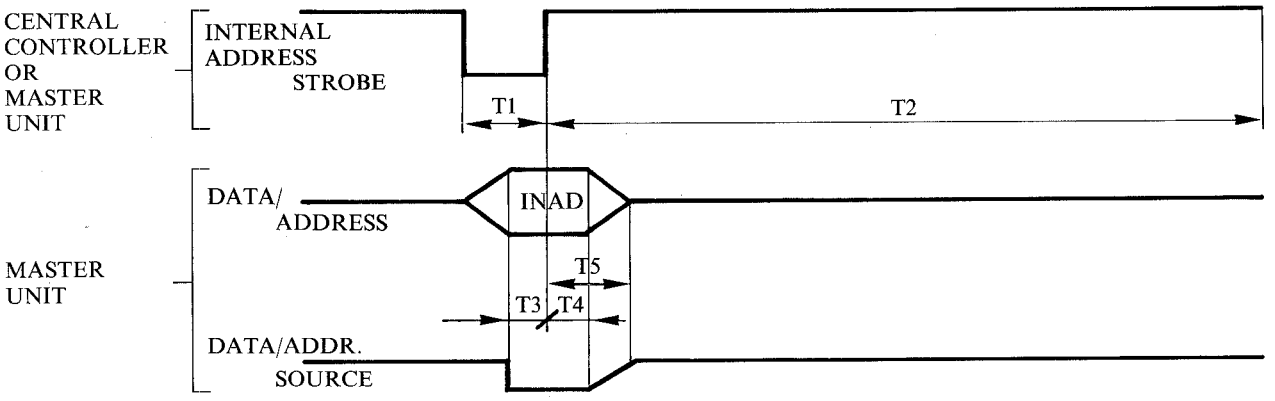

T1 = STROBE pulse duration — STROBE LOW – STROBE HIGH
T2 = address phase duration — AS HIGH – AS or DS LOW
T3 = set-up time — address valid – STROBE HIGH
T4 = hold time — STROBE HIGH – address invalid
T5 = release time — AS HIGH – DA7-DA0, A15-A8 and DAS HIGH IMPEDANCE

| | MIN | MAX |
|---|---|---|
| T1 | X | X |
| T2 | X | X |
| T3 | X | X |
| T4 | 0 | – |
| T5 | – | X |

– = Not specified.
X = To be specified for each application.

Legend:
Levels: ——— = HIGH (logical "1")
——— = HIGH IMPEDANCE
——— = LOW (logical "0")

Figure 2 (T/CD 02-05). Address phase.



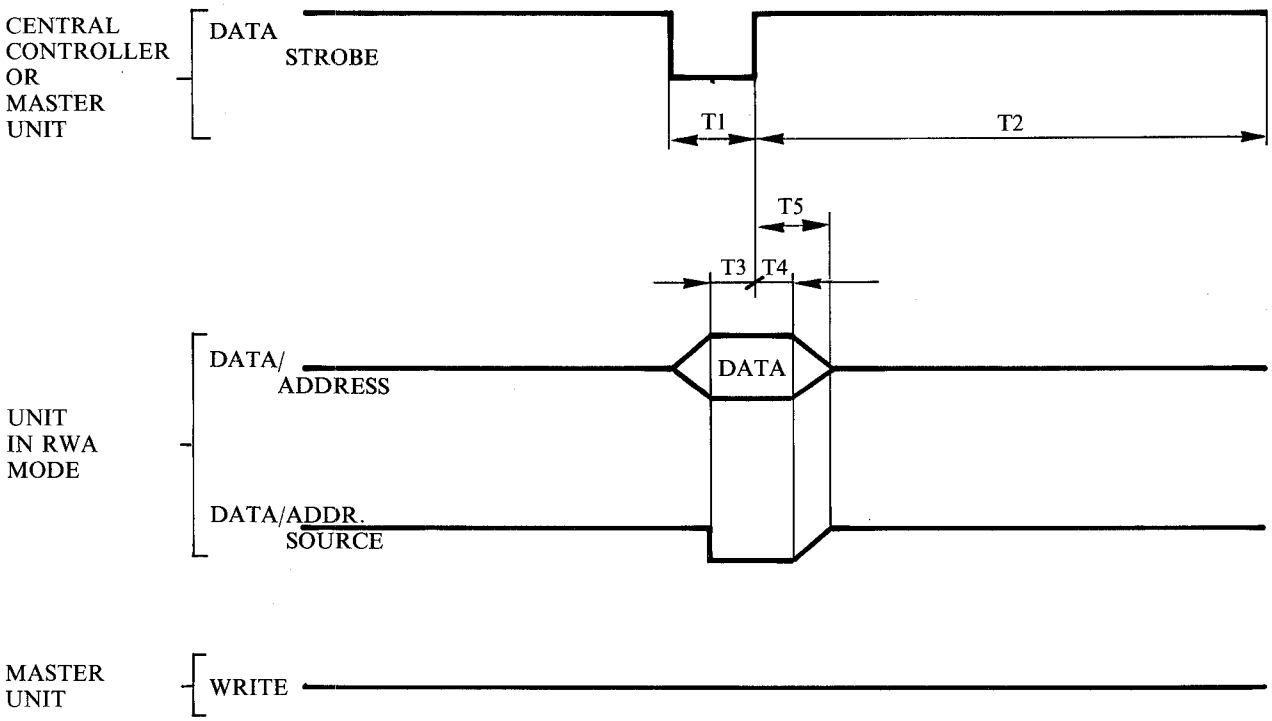

T1 = STROBE pulse duration — STROBE LOW – STROBE HIGH
T2 = int. addr. phase duration — IAS HIGH – IAS or DS LOW
T3 = set-up time — address valid – STROBE HIGH
T4 = hold time — STROBE HIGH – address invalid
T5 = release time — IAS HIGH – DA7-DA0 and DAS HIGH IMPEDANCE

| | MIN | MAX |
|---|---|---|
| T1 | X | X |
| T2 | X | X |
| T3 | X | X |
| T4 | 0 | – |
| T5 | – | X |

– = Not specified.
X = To be specified for each application.

Legend:
Levels: —— = HIGH (logical "1")
—— = HIGH IMPEDANCE
—— = LOW (logical "0")

Figure 3 (T/CD 02-05). Internal address phase.



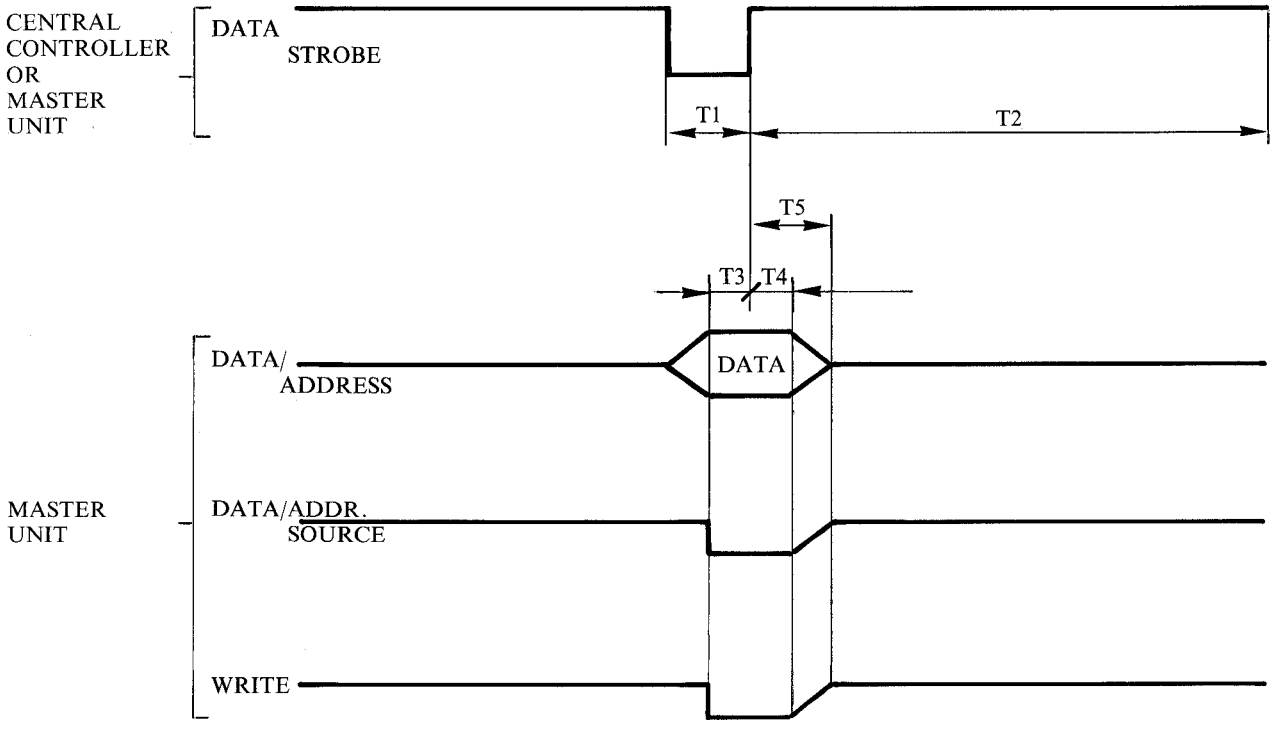

T1 = STROBE pulse duration — STROBE LOW – STROBE HIGH
T2 = read action duration — DS HIGH – AS, IAS or DS LOW
T3 = set-up time — data valid – STROBE HIGH
T4 = hold time — STROBE HIGH – data invalid
T5 = release time — DS HIGH – DA7-DA0 and DAS HIGH IMPEDANCE

| | MIN | MAX |
|---|---|---|
| T1 | X | X |
| T2 | X | X |
| T3 | X | X |
| T4 | 0 | – |
| T5 | – | X |

– = Not specified.
X = To be specified for each application.

Legend:
Levels: —— = HIGH (logical "1")
—— = HIGH IMPEDANCE
—— = LOW (logical "0")

Figure 4 (T/CD 02-05). Read action.

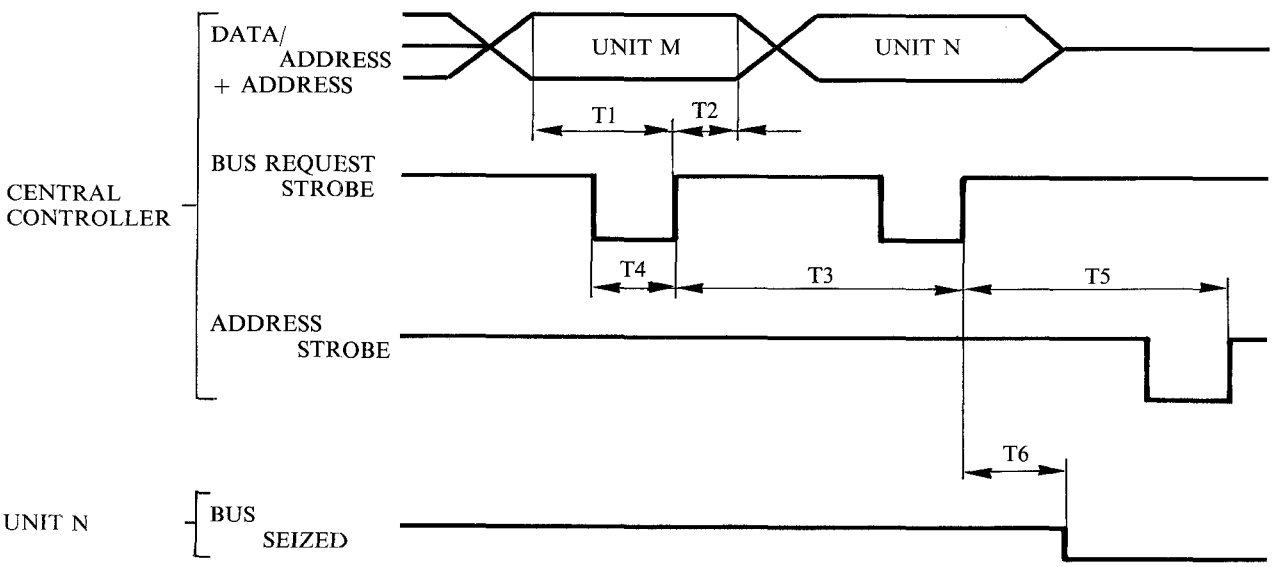



| | | |
|---|---|---|
| T1 | = STROBE pulse duration | STROBE LOW – STROBE HIGH |
| T2 | = write action duration | DS HIGH – AS, IAS or DS LOW |
| T3 | = set-up time | data valid – STROBE HIGH |
| T4 | = hold time | STROBE HIGH – data invalid |
| T5 | = release time | DS HIGH – DA7-DA0, WR and DAS HIGH IMPEDANCE |

T1-T5 identical values as given in Figure 4 (T/CD 02-05).

Legend:
Levels: ——— = HIGH (logical "1")
——— = HIGH IMPEDANCE
——— = LOW (logical "0")

Figure 5 (T/CD 02-05). Write action.




T1 = set-up time
T2 = hold time
T3 = BUS REQUEST STROBE repetition time
T4 = BUS REQUEST STROBE pulse duration
T5 = read/write cycle delay
T6 = BUS SEIZED delay

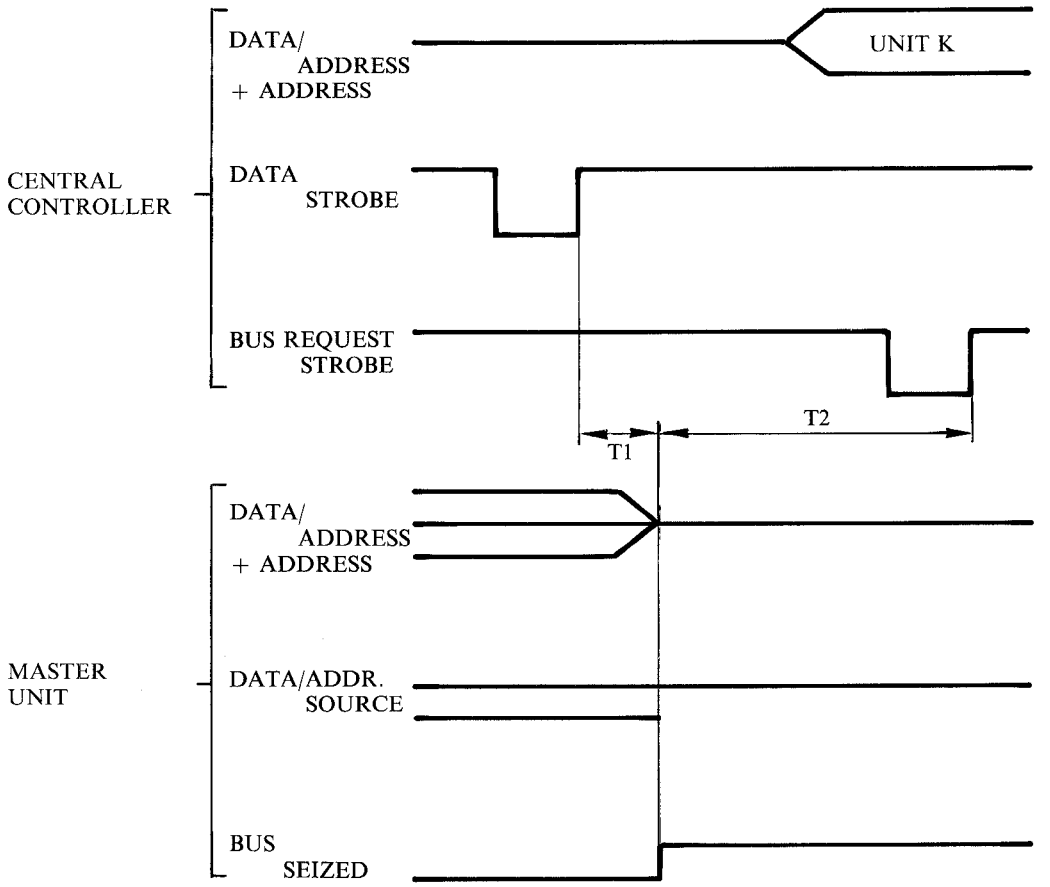
address valid – BUS REQUEST STROBE HIGH
BUS REQUEST STROBE HIGH – address invalid
BRS HIGH – BRS HIGH
BRS LOW – BRS HIGH
BRS HIGH – ADDRESS STROBE HIGH
BRS HIGH– BUS SEIZED LOW

| | MIN | MAX |
|---|---|---|
| T1 | X | – |
| T2 | 0 | – |
| T3 | X | X |
| T4 | X | T3-X |
| T5 | X | X |
| T6 | – | X |

– = Not specified.
X = To be specified for each application.

Legend:
Levels: ——— = HIGH (logical "1")
——— = HIGH IMPEDANCE
——— = LOW (logical "0")

Figure 6 (T/CD 02-05). Bus grant action.



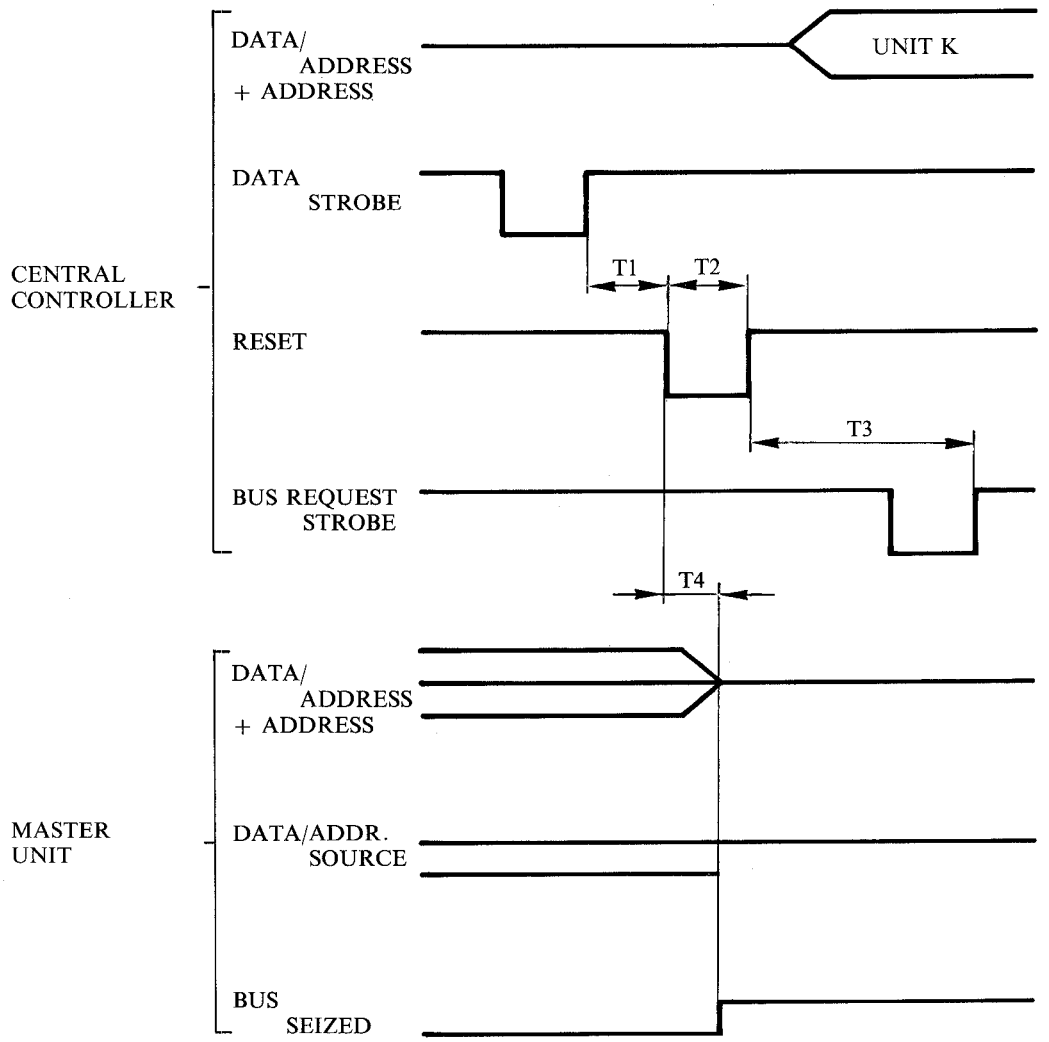

T1 = release time — DS HIGH – DA7-DA0, A15-A8, DAS and BS HIGH IMPEDANCE
T2 = recovery time — DS or AS HIGH – BRS HIGH

| | MIN | MAX |
|---|---|---|
| T1 | – | X |
| T2 | X | X |

– = Not specified.
X = To be specified for each application.

Legend:
Levels: —— = HIGH (logical "1")
—— = HIGH IMPEDANCE
—— = LOW (logical "0")

Figure 7 (T/CD 02-05). Bus release action; unit initiative.




T1 = BUS RELEASE delay — AS or DS HIGH – BR LOW
T2 = BR pulse duration — BR LOW – BR HIGH
T3 = recovery time — BR HIGH – BRS HIGH
T4 = release time — BR LOW – DA7-DA0, A15-A8, DAS and BS HIGH IMPEDANCE

| | MIN | MAX |
|---|---|---|
| T1 | X | X |
| T2 | X | X |
| T3 | X | X |
| T4 | – | X |

– = Not specified.
X = To be specified for each application.

Legend:
Levels: —— = HIGH (logical "1")
—— = HIGH IMPEDANCE
—— = LOW (logical "0")

Figure 8 (T/CD 02-05). Bus release action; Central Controller initiative.

## Annex A

## Pin Allocation

| | A | B | C |
|---|---|---|---|
| 1 | 0 V | 0 V | 0 V |
| 2 | DA0 | | A8 |
| 3 | DA1 | | A9 |
| 4 | DA2 | | A10 |
| 5 | DA3 | | A11 |
| 6 | DA4 | | A12 |
| 7 | DA5 | | A13 |
| 8 | DA6 | | A14 |
| 9 | | | |
| 10 | DA7 | | A15 |
| 11 | BR | | RES |
| 12 | BRS | | HT |
| 13 | AS | | PER |
| 14 | DS | | SYS |
| 15 | IAS | | |
| 16 | BS | PR0 | |
| 17 | | | |
| 18 | DAS | PR1 | |
| 19 | WR | PR2 | |
| 20 | | PR3 | |
| 21 | | PR4 | |
| 22 | | PR5 | |
| 23 | | PR6 | |
| 24 | | PR7 | |
| 25 | | | |
| 26 | −5 V | −5 V | −5 V |
| 27 | −12 V | −12 V | −12 V |
| 28 | +12 V | +12 V | +12 V |
| 29 | +5 V | +5 V | +5 V |
| 30 | +5 V | +5 V | +5 V |
| 31 | 0 V | 0 V | 0 V |
| 32 | 0 V | 0 V | 0 V |