

ETSI TS 101 135 V1.5.3 (2000-09)

Technical Specification

**Transmission and Multiplexing (TM);
High bit-rate Digital Subscriber Line (HDSL)
transmission systems on metallic local lines;
HDSL core specification and applications for combined
ISDN-BA and 2 048 kbit/s transmission**



Reference

RTS/TM-06019

Keywordsaccess, basic, digital, HDSL, ISDN, local loop,
rate, subscriber, transmission**ETSI**

650 Route des Lucioles
F-06921 Sophia Antipolis Cedex - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Siret N° 348 623 562 00017 - NAF 742 C
Association à but non lucratif enregistrée à la
Sous-Préfecture de Grasse (06) N° 7803/88

Important notice

Individual copies of the present document can be downloaded from:

<http://www.etsi.org>

The present document may be made available in more than one electronic version or in print. In any case of existing or perceived difference in contents between such versions, the reference version is the Portable Document Format (PDF). In case of dispute, the reference shall be the printing on ETSI printers of the PDF version kept on a specific network drive within ETSI Secretariat.

Users of the present document should be aware that the document may be subject to revision or change of status. Information on the current status of this and other ETSI documents is available at <http://www.etsi.org/tb/status/>

If you find errors in the present document, send your comment to:
editor@etsi.fr

Copyright Notification

No part may be reproduced except as authorized by written permission.
The copyright and the foregoing restriction extend to reproduction in all media.

© European Telecommunications Standards Institute 2000.
All rights reserved.

Contents

Intellectual Property Rights	11
Foreword.....	11
1 Scope	12
2 References	13
3 Abbreviations	15
4 Reference configuration and functional description.....	16
5 HDSL core specification	18
5.1 Functions	18
5.1.1 Transparent transport of core frames	19
5.1.2 Stuffing and destuffing	19
5.1.3 CRC-6 procedures and transmission error detection	19
5.1.4 Error reporting	19
5.1.5 Failure detection	19
5.1.6 Failure reporting	19
5.1.7 Bit timing	19
5.1.8 Frame alignment	19
5.1.9 HDSL transceiver autonomous start-up control.....	19
5.1.10 Loopback control and co-ordination	19
5.1.11 Mapping between core frames and HDSL frames	19
5.1.12 Control of the maintenance channel.....	20
5.1.13 Synchronization and co-ordination of HDSL transceivers	20
5.1.14 Identification of pairs.....	20
5.1.15 Correction of pair identification.....	20
5.1.16 Remote power feeding.....	20
5.1.17 Wetting current	20
5.2 Transmission medium	20
5.2.1 Description.....	20
5.2.2 Minimum Digital Local Line (DLL) requirements for HDSL applications.....	20
5.2.3 DLL physical characteristics.....	21
5.2.4 DLL electrical characteristics	21
5.2.4.1 Principal characteristics	21
5.2.4.2 Differences in physical transmission characteristics between pairs in the DLL	22
5.2.4.3 Crosstalk characteristics.....	22
5.2.4.4 Unbalance about earth.....	22
5.2.4.5 Impulse noise	22
5.2.4.6 Micro-interruptions	22
5.3 Transmission method	23
5.3.1 General.....	23
5.3.2 Transmission on three pairs	23
5.3.3 Transmission on two pairs	23
5.3.4 Transmission on one pair	23
5.3.5 Transmission on four pairs	23
5.3.6 Line code	23
5.3.7 Line baud rate	24
5.4 Frame structure.....	24
5.4.1 Core frame	24
5.4.2 2B1Q HDSL frame	24
5.4.2.1 2B1Q HDSL frame structure.....	29
5.4.2.1.1 Frame structure of the three pair system.....	29
5.4.2.1.2 Frame structure of the two pair system.....	30
5.4.2.1.3 Frame structure of the one pair system.....	32
5.4.2.2 Frame bit assignments.....	33
5.4.3 Scrambling method	36

5.5	HDSL embedded operations channel (eoc)	38
5.5.1	Functions of the HDSL eoc	38
5.5.2	HDSL eoc acknowledgement protocol	39
5.5.2.1	Message/echo response protocol state.....	40
5.5.2.2	Unable To Comply (UTC) mode of operation	40
5.5.3	The HDSL eoc data read/write mode.....	41
5.5.3.1	Data read protocol	41
5.5.3.2	HDSL eoc data read mode requirements.....	42
5.5.3.3	Data write protocol.....	43
5.5.3.4	HDSL eoc data write mode requirements	43
5.5.4	HDSL eoc message list	44
5.5.5	HDSL eoc message set requirements.....	44
5.5.6	Data registers in the NTU and in regenerators.....	47
5.5.7	Noise margin.....	48
5.5.7.1	General	48
5.5.7.2	Coding of the noise margin values	48
5.6	Start-up procedure	48
5.6.1	General.....	48
5.6.1.1	Start-up.....	48
5.6.1.2	Activation of HDSL transceiver pairs	49
5.6.1.3	Transparency	49
5.6.1.4	Noise margin	49
5.6.2	Control and status signals	49
5.6.2.1	Control signals	49
5.6.2.1.1	QUIET	49
5.6.2.1.2	ACTREQ	49
5.6.2.2	Status signals.....	49
5.6.2.2.1	LOSW.....	49
5.6.2.2.2	LOSWT	49
5.6.2.2.3	LOS	50
5.6.2.2.4	LOST	50
5.6.2.2.5	INDC	50
5.6.2.2.6	INDR	50
5.6.3	Transmitted signals	50
5.6.3.1	Silent	50
5.6.3.2	S0 signal	50
5.6.3.3	S1 signal.....	50
5.6.3.4	2B1Q data	51
5.6.4	Timers	51
5.6.4.1	T1	51
5.6.4.2	T2	51
5.6.4.3	T3	51
5.6.4.4	T4	51
5.6.4.5	T-Act	51
5.6.4.6	Timer values.....	51
5.6.5	Activation state diagrams.....	52
5.6.5.1	HDSL transceiver states at the NTU	52
5.6.5.2	HDSL transceiver states at the LTU	55
5.6.5.3	The HDSL synchronization state machine.....	57
5.6.6	Regenerator related procedures.....	57
5.6.6.1	Activation state diagrams for the REG.....	58
5.6.6.1.1	HDSL transceiver states at the REG-R.....	58
5.6.6.1.2	HDSL transceiver states at the REG-C.....	58
5.7	Operation and Maintenance (O&M).....	61
5.7.1	Functions at the LTU external O&M reference point	61
5.7.2	Functions at the NTU external O&M reference point	61
5.7.3	O&M messages and functions supported by the HDSL core.....	62
5.7.4	Power feeding related O&M functions	64
5.7.5	Regenerator behaviour.....	64
5.7.5.1	Response to LOS/LFA	64
5.7.5.2	Operation of loopback 1A.....	64
5.8	Electrical characteristics of a single 2B1Q transceiver	65

5.8.1	General.....	65
5.8.2	Transmitter/Receiver impedance and return loss.....	65
5.8.3	Transceiver reference clock.....	67
5.8.4	Transmitter output characteristics.....	67
5.8.4.1	Pulse amplitude.....	67
5.8.4.2	Pulse shape.....	67
5.8.4.3	Power Spectral Density (PSD).....	69
5.8.4.3.1	PSD for 392 kbaud systems.....	69
5.8.4.3.2	PSD for 584 kbaud systems.....	69
5.8.4.3.3	PSD for 1 160 kbaud systems.....	69
5.8.4.4	Total power.....	70
5.8.5	Unbalance about earth.....	71
5.8.5.1	Longitudinal Conversion Loss (LCL).....	71
5.8.5.2	Longitudinal output voltage.....	73
5.9	Performance of individual HDSL transceivers.....	74
5.9.1	Performance requirements.....	74
5.9.2	DLL physical models (test loops).....	74
5.9.3	Jitter and wander.....	74
5.9.3.1	General.....	74
5.9.3.2	Input jitter tolerance at the HDSL transceiver at the NTU.....	74
5.9.3.3	Output jitter limitations at the HDSL transceiver at the NTU.....	75
5.9.3.4	Input jitter tolerance at the HDSL transceiver at the LTU.....	75
5.9.3.5	Output jitter limitation of the HDSL transceiver at the LTU.....	75
6	Common circuitry specification.....	75
6.1	Delay difference buffer.....	75
6.2	The pair identification mechanism.....	76
6.2.1	Pair identification initial values.....	76
6.2.2	Pair identification at the NTU.....	76
6.2.3	Pair identification at the LTU.....	76
6.3	Laboratory performance measurements.....	77
6.3.1	General.....	77
6.3.2	Test configuration.....	77
6.3.3	Test procedure with shaped noise.....	82
6.3.3.1	General.....	82
6.3.3.2	Generation.....	83
6.3.3.3	Injection.....	83
6.3.3.4	Tolerances and calibration.....	83
6.3.3.4.1	0 dB level calibration.....	83
6.3.3.4.2	Test loop tolerances.....	83
6.3.4	Test procedure for impulse noise.....	83
6.3.4.1	Impulse noise test waveform.....	83
6.3.4.2	Impulse noise test measurement.....	84
6.3.4.3	Impulse noise test performance requirements.....	84
6.3.5	Common mode rejection test.....	85
6.3.6	Micro-interruption test.....	85
7	Application specific requirements.....	85
7.1	Application specific requirements for ISDN PRA.....	85
7.1.1	Mapping of 2 048 kbit/s to HDSL.....	85
7.1.2	Mapping of HDSL maintenance functions to the interface.....	86
7.1.3	Performance.....	86
7.1.3.1	Performance specification.....	86
7.1.3.2	Signal transfer delay.....	86
7.1.3.3	Clock specification for external interfaces.....	86
7.1.3.3.1	NTU clock tolerance.....	86
7.1.3.3.2	LTU clock tolerance.....	87
7.1.3.3.3	Jitter specification.....	87
7.1.3.3.4	Wander specification.....	88
7.1.3.4	Laboratory performance measurement.....	89
7.2	Application specific requirements for the 2 048 kbit/s digital unstructured leased line (D2048U).....	89
7.2.1	Application interfaces.....	89

7.2.1.1	Application interface at the customer side	89
7.2.1.2	Application interface at the network side	89
7.2.2	Mapping of the D2048U signal to HDSL	89
7.2.3	Mapping of HDSL maintenance functions to the interface.....	89
7.2.4	Performance.....	90
7.2.4.1	Performance specification	90
7.2.4.2	Signal transfer delay.....	90
7.2.4.3	Clock specification for external interfaces	90
7.2.4.3.1	NTU clock tolerance.....	90
7.2.4.3.2	LTU clock tolerance	90
7.2.4.3.3	Jitter specification.....	90
7.2.4.4	Laboratory performance measurements	91
7.3	Application specific requirements for the 2 048 kbit/s digital structured leased line (D2048S)	91
7.3.1	Application interfaces	91
7.3.1.1	Application interface at the customer side	91
7.3.1.2	Application interface at the network side.....	91
7.3.2	Mapping of the D2048S signal to HDSL.....	91
7.3.3	Mapping of HDSL maintenance functions to the interface.....	92
7.3.4	Performance.....	92
7.3.4.1	Performance specification	92
7.3.4.2	Signal transfer delay.....	92
7.3.4.3	Clock specification for external interfaces	92
7.3.4.3.1	NTU clock tolerance.....	92
7.3.4.3.2	LTU clock tolerance	93
7.3.4.3.3	Jitter specification.....	93
7.3.4.4	Laboratory performance measurements	93
7.4	Application specific requirements for fractional installation	94
7.4.1	Mapping of fractional services to HDSL	94
7.4.1.1	Overview of mapping procedure.....	94
7.4.1.2	Details of mapping of the application interface from the HDSL core frame	94
7.4.1.3	Details of HDSL core frame mapping into HDSL frame	94
7.4.1.4	Optional external mappings into the application frame.....	94
7.4.2	Mapping of HDSL maintenance functions to the interface.....	95
7.4.3	Performance.....	100
7.4.3.1	Performance specification	100
7.4.3.2	Clock specification for external interfaces	100
7.4.3.2.1	Clock tolerance	100
7.4.3.2.2	Jitter and wander specifications.....	100
7.4.3.3	Laboratory performance measurements	100
7.5	Application specific requirements for partial operation	100
7.5.1	Mapping of the application frame for partial operation application	100
7.5.2	Mapping of HDSL maintenance functions to the interface.....	100
7.5.3	Performance.....	101
7.5.4	Remote power feeding	101
7.5.5	Partial failure criteria	101
7.5.6	Action following partial failure	101
7.5.7	Time slot prioritization/reallocation	102
7.6	Application specific requirements for the 2 048 kbit/s mapped into TU-12 structure.....	105
7.6.1	Reference configuration.....	105
7.6.2	Application Interfaces.....	105
7.6.2.1	Application interface at the customer side	105
7.6.2.2	Application interface at the network side.....	105
7.6.3	Mapping of application frame into HDSL using TU-12 structure	105
7.6.3.1	Mapping of application frame into VC-12 structure	105
7.6.3.2	Mapping of VC-12 into TU-12	106
7.6.3.3	Mapping of TU-12 into HDSL.....	106
7.6.4	Mapping of HDSL maintenance functions to the interface.....	106
7.6.5	Performance.....	107
7.6.5.1	Performance specification	107
7.6.5.2	Signal transfer delay.....	107
7.6.5.3	Clock specification.....	107
7.6.5.3.1	Clock synchronization at the NTU	107

7.6.5.3.2	Jitter specification.....	107
7.6.5.4	Laboratory performance measurement.....	108
7.7	Application specific requirements for the simultaneous connection of 2 048 kbit/s digital signals and ISDN-BA inside the HDSL core frame.....	111
7.7.1	Reference Configuration.....	111
7.7.2	Application interfaces.....	111
7.7.2.1	Application interfaces at the customer side.....	111
7.7.2.1.1	2 048 kbit/s interfaces.....	111
7.7.2.1.2	ISDN interfaces.....	111
7.7.2.2	Application interfaces at the network side.....	111
7.7.2.2.1	2 048 kbit/s interfaces.....	111
7.7.2.2.2	ISDN interfaces.....	111
7.7.3	Mapping procedures.....	112
7.7.3.1	Conversion of the ISDN-BA signals.....	112
7.7.3.2	Mapping of the ISDN-BA to the core frame.....	112
7.7.3.3	Core frame mapping into HDSL frame.....	113
7.7.4	Mapping of HDSL maintenance functions to the interface.....	116
7.7.5	Performance.....	116
7.7.5.1	Performance specification.....	116
7.7.5.2	Signal transfer delay.....	116
7.7.5.3	Clock specification.....	116
7.7.5.3.1	NTU clock tolerance.....	116
7.7.5.3.2	LTU clock tolerance.....	116
7.7.5.3.3	ISDN clock tolerance.....	116
7.7.5.3.4	Clock synchronization for ISDN-BA.....	116
7.7.5.3.5	Jitter and wander specification.....	117
7.7.5.4	Laboratory performance measurements.....	117
7.7.6	Power feeding.....	117
7.8	Application specific requirements for the simultaneous connection of 2 048 kbit/s digital signals and analogue telephone lines inside the HDSL core frame.....	118
7.8.1	Reference Configuration.....	118
7.8.2	Application interfaces.....	118
7.8.2.1	Application interface at the customer side.....	118
7.8.2.1.1	2 048 kbit/s interfaces.....	118
7.8.2.1.2	Analogue telephone interfaces.....	118
7.8.2.2	Application interface at the network side.....	118
7.8.2.2.1	2 048 kbit/s interfaces.....	118
7.8.2.2.2	Analogue telephone interfaces.....	118
7.8.3	Mapping procedures.....	119
7.8.3.1	Conversion of the analogue telephone signals.....	119
7.8.3.2	Mapping of the combined signals to the core frame.....	119
7.8.3.3	Core frame mapping into HDSL frame.....	119
7.8.4	Mapping of HDSL maintenance functions to the interface.....	119
7.8.5	Performance.....	119
7.8.5.1	Performance specification.....	119
7.8.5.2	Signal transfer delay.....	119
7.8.5.3	Clock specification.....	121
7.8.5.3.1	NTU clock tolerance.....	121
7.8.5.3.2	LTU clock tolerance.....	121
7.8.5.3.3	Clock synchronization for analogue telephony interfaces.....	121
7.8.5.3.4	Void.....	121
7.8.5.3.5	Jitter and wander specification.....	121
7.8.5.4	Laboratory performance measurements.....	121
7.8.6	Power feeding.....	121
8	Power feeding.....	122
8.1	General.....	122
8.2	Wetting current.....	122
8.3	Remote power feeding aspects.....	122
8.3.1	Remote power feeding aspects at the LTU.....	123
8.3.2	Remote power feeding aspects at the NTU.....	123
8.3.3	Remote power feeding aspects at the regenerator.....	123

9	Environmental requirements	124
9.1	Climatic conditions.....	124
9.2	Safety.....	124
9.3	Overvoltage protection	124
9.4	Electromagnetic compatibility (EMC)	124
Annex A (informative): Detailed definition of cable characteristics and test loops.....		125
A.1	Typical characteristics of cables.....	125
A.2	Theoretical characteristics of test loops for $Y = 31$ dB at 150 kHz.....	126
Annex B (normative): High bit-rate Digital Subscriber Line (HDSL) CAP based system		128
B.1	Scope and general information.....	128
B.1.1	Scope	128
B.2	References	128
B.3	Abbreviations	128
B.4	Reference configuration and functional description.....	128
B.5	HDSL core specification	128
B.5.1	Functions	128
B.5.2	Transmission medium	129
B.5.3	Transmission method	129
B.5.3.1	General.....	129
B.5.3.2	Transmission on one pair.....	129
B.5.3.3	Transmission on two pairs	129
B.5.3.4	Transmission on three or four pairs	129
B.5.3.5	Line code	129
B.5.3.5.1	Trellis encoding/decoding	129
B.5.3.5.1.1	64 point constellation - two pair system	129
B.5.3.5.1.2	128 point constellation - one pair system	130
B.5.3.5.2	Scrambling method	132
B.5.3.6	Line symbol rate	134
B.5.4	Frame structure.....	135
B.5.4.1	Core frame	135
B.5.4.2	HDSL frame.....	135
B.5.4.2.1	HDSL frame structure	135
B.5.4.2.1.1	Frame structure for two pair system.....	135
B.5.4.2.1.2	Frame structure for one pair system	136
B.5.4.2.2	HDSL frame bit assignments	138
B.5.5	HDSL embedded operations channel (eoc).....	140
B.5.5.1	Signal Quality (SQ)	140
B.5.6	Start-up procedure	140
B.5.6.1	General.....	140
B.5.6.1.1	Start-up.....	140
B.5.6.1.2	Activation of HDSL transceiver pairs	140
B.5.6.1.3	Transparency.....	140
B.5.6.1.4	Signal quality (SQ).....	141
B.5.6.2	Control and status signals	141
B.5.6.3	Transmitted signals	141
B.5.6.3.1	Silent	141
B.5.6.3.2	S0 signal.....	141
B.5.6.3.3	S1 signal.....	141
B.5.6.3.4	S2 signal.....	141
B.5.6.3.5	S3 signal.....	142
B.5.6.4	Timers	142
B.5.6.4.1	T1	142
B.5.6.4.2	T2.....	142
B.5.6.4.3	T3.....	142
B.5.6.4.4	T4.....	142

B.5.6.4.5	T5	142
B.5.6.4.6	T6	142
B.5.6.4.7	T7	142
B.5.6.4.8	T8	143
B.5.6.4.9	T9	143
B.5.6.4.10	T10	143
B.5.6.4.11	T11	143
B.5.6.4.12	T12	143
B.5.6.4.13	T-Act	143
B.5.6.4.14	Timer values	143
B.5.6.5	HDSL transceiver activation	144
B.5.6.5.1	Alerting	146
B.5.6.5.1.1	Two pair system alerting sequence	146
B.5.6.5.1.2	One pair transceiver alerting sequence	147
B.5.6.5.2	Transmit power mode selection	147
B.5.6.5.3	Front-end training	148
B.5.6.5.4	Timing recovery, echo canceller and equalizer training	148
B.5.6.5.5	Tomlinson coefficient exchange	149
B.5.6.5.6	Control field bit assignments	151
B.5.6.5.7	Transition to data mode	151
B.5.6.6	Retrain procedure	152
B.5.6.7	Loop activation state diagrams	152
B.5.6.7.1	HDSL transceiver states at the NTU	152
B.5.6.7.1.1	Inactive State	152
B.5.6.7.1.2	Activating State	152
B.5.6.7.1.3	Active-Rx State	153
B.5.6.7.1.4	Active-Tx State	153
B.5.6.7.1.5	Active-Tx/Rx State	153
B.5.6.7.1.6	Pending Deactivation State	153
B.5.6.7.1.7	Deactivated State	154
B.5.6.7.2	HDSL transceiver states at LTU	154
B.5.6.7.2.1	Inactive State	154
B.5.6.7.2.2	Activating State	154
B.5.6.7.2.3	Active-Rx State	155
B.5.6.7.2.4	Active-Tx State	155
B.5.6.7.2.5	Active State	155
B.5.6.7.2.6	Pending Deactivation State	155
B.5.6.7.2.7	Deactivated State	155
B.5.6.7.3	The HDSL synchronization state machine	155
B.5.6.8	Regenerator related procedures	155
B.5.6.9	The pair identification mechanism for two pair system	156
B.5.7	Operation and Maintenance (O&M)	156
B.5.7.1	Regenerator behaviour	156
B.5.7.1.1	Response to LOS/LFA	156
B.5.7.1.2	Operation of loopback 1A	156
B.5.8	Electrical characteristics of CAP-based transceivers	157
B.5.8.1	General	157
B.5.8.2	Transmitter/receiver impedance and return loss	157
B.5.8.3	Transceiver reference clock	158
B.5.8.3.1	One pair system clock	158
B.5.8.3.2	Two pair system clock	158
B.5.8.4	Transmitter output characteristics	158
B.5.8.4.1	Total power	158
B.5.8.4.1.1	Two pair system total power	158
B.5.8.4.1.2	One pair system total power	158
B.5.8.4.2	PSD	158
B.5.8.5	Unbalance about earth	160
B.5.8.5.1	Longitudinal Conversion Loss (LCL)	160
B.5.8.5.2	Longitudinal output voltage	160
B.5.9	Performance of individual HDSL transceivers	161
B.5.9.1	Performance requirements	161
B.5.9.2	DLL physical models for laboratory testing	161

B.5.9.3	Jitter and wander	161
B.5.9.3.1	General	161
B.5.9.3.2	Input jitter tolerance at the HDSL transceiver at the NTU	162
B.5.9.3.3	Output jitter limitations of an HDSL transceiver in an NTU	163
B.5.9.3.4	Input jitter tolerance at the HDSL transceiver at the LTU	163
B.5.9.3.5	Output jitter limitation of the HDSL transceiver at the LTU	163
B.6	Common circuitry specification	164
B.6.1	Delay difference buffer	164
B.6.2	Laboratory performance measurement tests	164
B.6.2.1	General	164
B.6.2.2	Test configuration	164
B.6.2.3	Test procedure with random noise source	166
B.6.2.3.1	Low crest factor noise	166
B.6.2.3.2	Truncated Gaussian noise	166
B.6.2.4	Test procedure for impulse noise	166
B.6.2.4.1	Impulse noise test waveform	166
B.6.2.4.2	Impulse noise test measurement	166
B.6.2.4.3	Impulse noise test performance requirements	166
B.6.2.5	Common mode rejection test	167
B.6.2.6	Micro-interruption test	167
B.7	Application specific requirements	168
B.7.1	Application specific requirements for ISDN PRA	168
B.7.1.1	Mapping of 2 048 kbit/s to HDSL	168
B.7.1.2	Mapping of HDSL maintenance functions to the interfaces	168
B.7.1.3	Performance	168
B.7.1.3.1	Performance specification	168
B.7.1.3.2	Signal transfer delay	168
B.7.1.3.3	Clock specification for external interfaces	168
B.7.2	Additional application specific requirements	168
B.8	Power feeding	169
B.9	Environmental requirements	169
Annex C (informative): Transmission system for 1 544 kbit/s two pair system application		170
C.1	Frame structure of the two pair system for 784 kbit/s	170
History	173

Intellectual Property Rights

IPRs essential or potentially essential to the present document may have been declared to ETSI. The information pertaining to these essential IPRs, if any, is publicly available for **ETSI members and non-members**, and can be found in ETSI SR 000 314: "*Intellectual Property Rights (IPRs); Essential, or potentially Essential, IPRs notified to ETSI in respect of ETSI standards*", which is available from the ETSI Secretariat. Latest updates are available on the ETSI Web server (<http://www.etsi.org/ipr>).

Pursuant to the ETSI IPR Policy, no investigation, including IPR searches, has been carried out by ETSI. No guarantee can be given as to the existence of other IPRs not referenced in ETSI SR 000 314 (or the updates on the ETSI Web server) which are, or may be, or may become, essential to the present document.

Foreword

This Technical Specification (TS) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM).

The previous three versions have been published by ETSI as ETR 152 Editions 1, 2 and 3, while version 4 was published as TS 101 135 V1.4.1.

This version provides a correction to an editorial error in figures 32 and B.27.

1 Scope

The present document describes a transmission technique called High bit-rate Digital Subscriber Line (HDSL), as a means for the transportation of several types of applications. The present document defines the requirements for the individual HDSL transmission system, the transmission performance, the HDSL maintenance requirements and procedures and the mapping of information from the dedicated applications.

An individual HDSL transceiver system is a two wire bi-directional transceiver for metallic wires using the echo cancellation method. Three systems may be utilized, one transporting a bit rate of 784 kbit/s over each of three pairs used in parallel, a second with an increased bit rate of 1 168 kbit/s and two pairs in parallel only and a third with a more increased bit rate of 2 320 kbit/s on one pair only.

The line codes of systems specified in the present document are 2B1Q (2 Binary 1 Quaternary) and CAP (Carrierless Amplitude Phase modulation). Systems using a CAP line code are covered in annex B. Annex C summarizes the Committee T1 recommendation for the frame structure of 1 544 kbit/s applications. Only one of the line codes has to be realized in a transmission system.

The present document defines the common circuitry for combining and controlling one, two or three HDSL transceiver systems, depending on the bit rate of the transceiver system used, for the support of applications with a 2 048 kbit/s hierarchy. The common circuitry and the necessary number of HDSL transceiver systems form the HDSL core, which is independent from the different applications defined in the present document.

The applications of HDSL are determined by the functionality of the mapping and interface part, some of which are defined as follows:

- ISDN primary rate access digital section in accordance with ETS 300 233 [1];
- ONP leased line access D2048U based on ETS 300 246 [2] and ETS 300 247 [3];
- ONP leased line access D2048S based on ETS 300 418 [4] and ETS 300 419 [5];
- 2 Mbit/s access to the Synchronous Digital Hierarchy (SDH) via a TU-12.

The HDSL core may be used for applications that are not restrictive to the access portion of the network but this is outside the scope of the present document.

NOTE: If further applications are identified in future the present document may be enhanced to define the relevant interface and mapping requirements as far as these do not violate the specification of the HDSL core.

Special applications of the HDSL core or part of the HDSL core can be:

- fractional installation, which provides reduced access capability only by a reduced number of HDSL transceivers, to cater for an inexpensive system if the total capacity of 30×64 kbit/s is not needed;
- partial operation, which is the persistent operation of the operable HDSL transceiver systems when others become inoperable;
- fractional payload, e.g. H_0 -channel.

The bit-rate at the application interface will also be 2 048 kbit/s in these applications, but not all the time slots in the ITU-T Recommendation G.704 [32] frame may be used, or there may be network specific interfaces used for these applications, the definition of which is outside the scope of the present document.

The present document does not specify all the requirements for the implementation of NTU, LTU or REG. It serves only to describe the functionality needed.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

- [1] ETS 300 233: "Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate".
- [2] ETS 300 246 (1993): "Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased line (D2048U) Network interface presentation".
- [3] ETS 300 247 (1993): "Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased line (D2048U) Connection characteristics".
- [4] ETS 300 418 (1995): "Business Telecommunications (BTC); 2 048 kbit/s digital unstructured and structured leased lines (D2048U and D2048S); Network interface presentation".
- [5] ETS 300 419 (1995): "Business Telecommunications (BTC); 2 048 kbit/s digital structured leased lines (D2048S); Connection characteristics".
- [6] ETR 080 (1993): "Transmission and Multiplexing (TM); Integrated Services Digital Network (ISDN) basic rate access; Digital transmission system on metallic local lines".
- [7] ETS 300 011 (1992): "Integrated Services Digital Network (ISDN); Primary rate user-network interface; Layer 1 specification and test principles".
- [8] CCITT Fascicle I.3: "Definitions".
- [9] ITU-T Recommendation G.823 (1993): "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".
- [10] ITU-T Recommendation G.826 (1993): "Error performance parameters and objectives for international, constant bit rate digital paths at or above the primary rate".
- [11] ETS 300 019 (1992): "Equipment Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment".
- [12] ITU-T Recommendation O.151 (1992): "Error performance measuring equipment operating at the primary rate and above".
- [13] EN 60950 (1992): "Safety of information technology equipment".
- [14] CCITT Recommendation K.17 (1988): "Tests on power-fed repeaters using solid-state devices in order to check the arrangement for protection from external interference".
- [15] ITU-T Recommendation K.20 (1996): "Resistibility of telecommunication switching equipment to overvoltages and overcurrents".
- [16] ITU-T Recommendation K.21 (1996): "Resistibility of subscriber's terminal to overvoltages and overcurrents".

- [17] ETS 300 386-2: "Electromagnetic compatibility and Radio spectrum Matters (ERM); Telecommunication network equipment; ElectroMagnetic Compatibility (EMC) requirements; Part 2: Product family standard".
- [18] ETS 300 386-1: "Equipment Engineering (EE); Telecommunication network equipment; ElectroMagnetic Compatibility (EMC) requirements; Part 1: Product family overview, compliance criteria and test levels".
- [19] ETS 300 166 (1993): "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2 048 kbit/s - based plesiochronous or synchronous digital hierarchies".
- [20] ETS 300 167 (1993): "Transmission and Multiplexing (TM); Functional characteristics of 2 048 kbit/s interfaces".
- [21] ISO 2110 (1991): "Information Technology - Data communication - 25-pole DTE/DCE interface connector and connect number assignments".
- [22] ITU-T Recommendation G.707 (1995): "Network node interface for the synchronous digital hierarchy (SDH)".
- [23] IEEE Transactions on Information Theory, Volume IT-33 (July 1984): "Rotationally Invariant Convolutional Coding with Expanded Signal Space - Part II: Nonlinear Codes" (Lee-Fang Wei).
- [24] IEEE Journal on Selected Areas in Communication, Volume 9, No. 6 (August 1991): "Combined Trellis Coding and DFE Through Tomlinson Precoding" (R. L. Cupo et al).
- [25] ANSI Committee T1 Technical Report No. 28 (February 1994): "A Technical Report on High Bit-Rate Digital Subscriber Lines (HDSL)".
- [26] IEEE Transactions on Circuits and Systems Volume CAS-33 No. 10 (October 1986): "Multitone Signals with Low Crest Factor" (Stephen Boyd).
- [27] ETS 300 012: "Integrated Services Digital Network (ISDN); Basic user-network interface; Layer 1 specification and test principles".
- [28] ETS 300 297: "Integrated Services Digital Network (ISDN); Access digital section for ISDN basic access".
- [29] ITU-T Recommendation Q.552: "Transmission characteristics at 2-wire analogue interfaces of digital exchanges".
- [30] CCITT Recommendation G.711 (1988): "Pulse code modulation (PCM) of voice frequencies".
- [31] ITU-T Recommendation G.821: "Error performance of an international digital connection operating at a bit rate below the primary rate and forming part of an integrated services digital network".
- [32] ITU-T Recommendation G.704 (1998): "Synchronous frame structures used at 1 544, 6 312, 2 048, 8 488 and 44 736 kbit/s hierarchical levels".

3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

2B1Q	2 Binary 1 Quaternary (line code)
AIS	Alarm Indication Signal
BER	Bit Error Ratio
BERTS	Bit Error Ratio Test Set
BT	Bridged Tap (an unterminated twisted pair section bridged across the line)
CAP	Carrierless Amplitude Phase modulation
CRC	Cyclic Redundancy Check
DC	Direct Current
DLL	Digital Local Line
EMC	ElectroMagnetic Compatibility
eoc	embedded operations channel
HDSL	High bit rate Digital Subscriber Line
HOH	HDSL OverHead
ISDN-BA	Integrated Services Digital Network Basic Access
ISDN-PRA	Integrated Services Digital Network Primary Rate Access
IUT	Implementation Under Test
LCL	Longitudinal Conversion Loss
LFA	Loss of Frame Alignment
LOS	Loss of Signal
lsb	least significant bit
LTU	Line Termination Unit
msb	most significant bit
MTIE	Maximum Time Interval Error
NEXT	Near End crosstalk
NNI	Network Node Interface
NTU	Network Termination Unit
O&M	Operation and Maintenance
ONP	Open Network Provision
ppm	parts per million
PRBS	Pseudo-Random Bit Sequence
PSD	Power Spectral Density
PSL	Power Sum Loss
REG	REGenerator
REG-C	NTU side of the regenerator
REG-R	LTU side of the regenerator
rms	root mean square
SDH	Synchronous Digital Hierarchy
TMN	Telecommunications Management Network
TS	Time slot
TU-12	Tributary Unit-12
UI	Unit Interval
UNI	User Network Interface
UTC	Unable To Comply
VC-12	Virtual Container-12

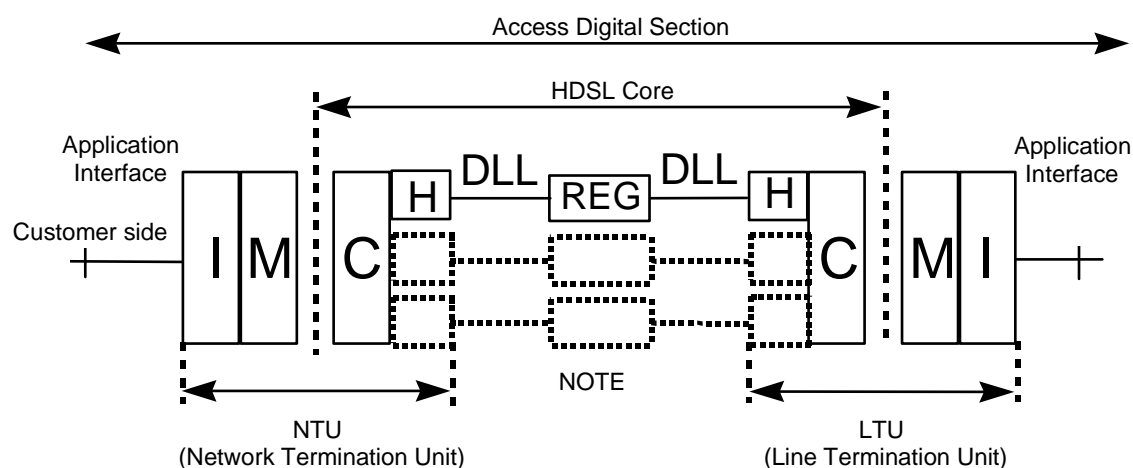
4 Reference configuration and functional description

An access digital section which uses HDSL technology can be considered as a number of functional blocks, (see figure 1). Depending upon the HDSL transceiver (H) transmission rate, a fully equipped HDSL core consists of one 2 320 kbit/s, two 1 168 kbit/s or three 784 kbit/s HDSL transceiver pairs connected by Digital Local Lines (DLLs) (which are linked by some common circuitry (C)). The HDSL core is application independent. Operation with a non-fully equipped HDSL core is also permitted.

If enhanced transmission range is required the HDSL core may contain optional regenerators (REGs). The overall insertion loss of the HDSL core with regenerator shall be less than 1,8 times the value Y of the non-regenerated HDSL core. The regenerator may be inserted at any convenient intermediate point in the HDSL core with the limitation that the insertion loss of each part-DLL shall be less than 0,9 times Y. In addition there may be further restrictions in line length due to power feeding.

An application is defined by the interface (I) and mapping & maintenance (M) functionalities.

The functionalities at the exchange side constitute the Line Termination Unit (LTU) and act as master to the (slave) customer side functionalities, which collectively form the Network Termination Unit (NTU) and the REGs where applicable.



Description of functional blocks:

C = Common circuitry
I = Interface

DLL = Digital Local Line
M = Mapping

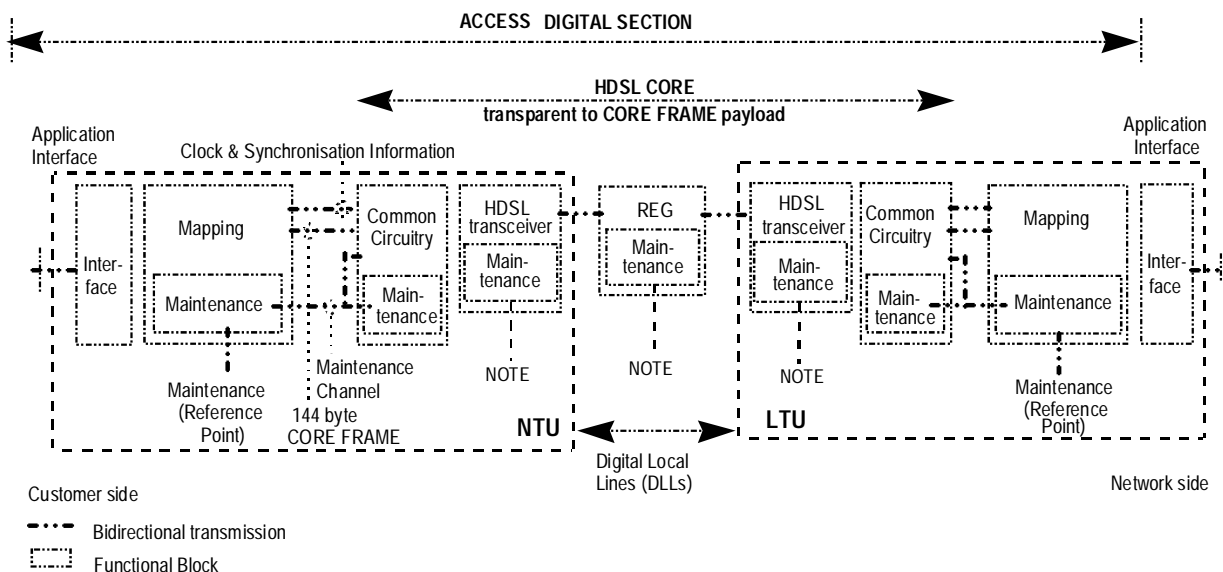
H = HDSL transceiver
REG = Regenerator

NOTE: A fully equipped HDSL core consists of one, two or three H, REG and DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 1: Access digital section employing HDSL technology (simplified configuration)

Throughout the present document, reference is made to the terms REG-C, REG-R and individual HDSL transmission systems. REG-R identifies functionalities located at the LTU side of the regenerator, REG-C identifies functionalities located at the NTU side of the regenerator.

Figure 2 describes the maintenance and other communication functionalities more clearly.



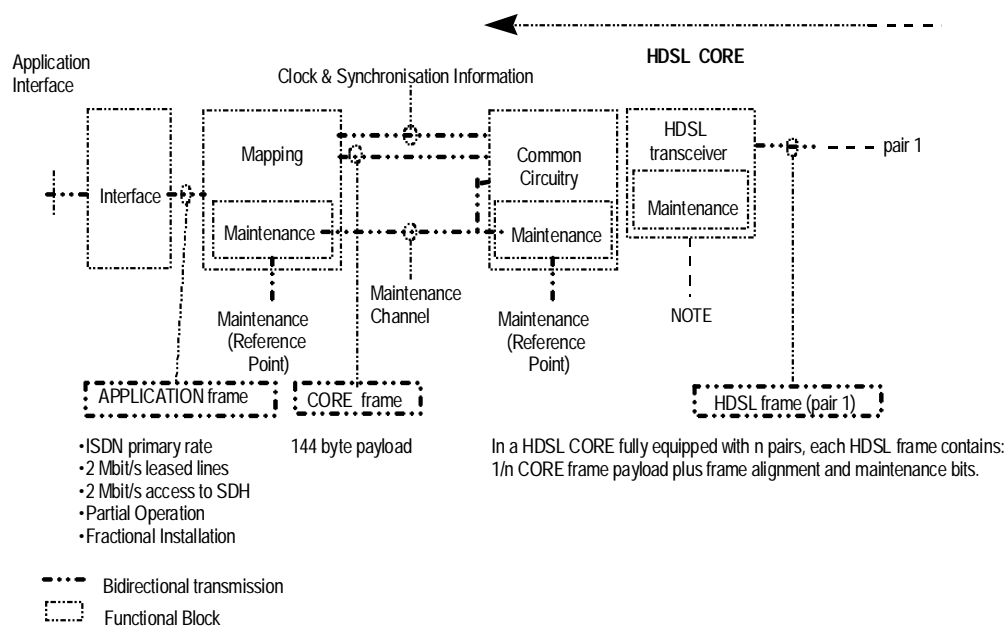
NOTE: A fully equipped HDSL CORE consists of one, two or three H, REG, DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 2: Access digital section employing HDSL technology (detailed configuration)

The information transmitted between the NTU side (slave side) and LTU side (master side) is handled as follows:

- at the application interface (I), the data flow is grouped in **application frames** (e.g. 32 time slot ISDN primary rate frames, as specified in ETS 300 011 [7]);
- the mapping function (part of the M functional block) then takes the application frame and inserts it into a 144 byte **core frame**. (In some applications not all data bytes will contain valid information and may be set to idle patterns);
- the core frame is then given to the common circuitry (C) where it is combined with any necessary alignment bits, maintenance bits and overhead bits, in order to be sent transparently in **HDSL frames** over the DLLs. The use of REGs is optional;
- at the receiving side, data within the HDSL frames is multiplexed by the common circuitry to again form the core frame which is passed to the mapping function where it is mapped into the application frame and transmitted over the application interface (I).

An overview of the different framing procedures can be found in figure 3.



NOTE: A fully equipped HDSL CORE consists of one, two or three H, REG, DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 3: An overview of framing procedures

In addition, there may be maintenance and/or power feeding functions associated with the HDSL core for the support of failure identification, localization and HDSL start-up control, however the presentation of this information at the maintenance reference point is outside the scope of the present document.

The specification of the HDSL core is aimed at interoperability of two equipments from different vendors.

5 HDSL core specification

5.1 Functions

The functions listed below are necessary for the correct operation of the HDSL core.

Functions related to the HDSL core	LTU	NTU/ REG
Transparent transport of core frames (144 bytes)	<---->	
Stuffing and destuffing	<---->	
CRC-6 procedures and transmission error detection	<---->	
Error reporting	<---->	
Failure detection	<---->	
Failure reporting	<---->	
Bit timing	<---->	
Frame alignment	<---->	
HDSL transceiver autonomous start-up control	----->	
Loopback control and co-ordination	----->	
Mapping of core frames into HDSL frames	<---->	
Control of maintenance channel	<---->	
Synchronization and co-ordination of HDSL transceivers	----->	
Identification of pairs	<---->	
Correction of pair identification		(see note)

NOTE: Correction of pairs is a function of the NTU.

Functions related to power feeding	LTU	NTU/ REG
Remote power feeding (optional)		---->
Wetting current (optional)		---->

5.1.1 Transparent transport of core frames

This function provides for the bi-directional transmission of the core frames with 144 bytes over one, two or three parallel HDSL transceiver systems connected by separate pairs.

5.1.2 Stuffing and destuffing

This function provides for the synchronization of the application data clock to the HDSL transceiver system clock, by means of adding zero or two stuffing quats per HDSL frame.

5.1.3 CRC-6 procedures and transmission error detection

This function provides for error performance monitoring of the HDSL transceiver systems in each HDSL frame.

5.1.4 Error reporting

This function provides for the reporting of errors detected by means of CRC-6 procedure.

5.1.5 Failure detection

This function provides for the detection of failures in the HDSL transceiver system.

5.1.6 Failure reporting

This function provides for the reporting of failures detected in the HDSL transceiver systems by means of messages in the maintenance channel realized i.e. by HDSL frame overhead bits.

5.1.7 Bit timing

This function provides bit (signal element) timing to enable the HDSL transceiver systems to recover information from the aggregate bit stream.

5.1.8 Frame alignment

This function provides information to enable the HDSL transceiver systems to recover the HDSL frame and the HDSL frame overhead.

5.1.9 HDSL transceiver autonomous start-up control

This function provides for the recovering of the operational state after first powering or break down of the HDSL transceiver systems.

5.1.10 Loopback control and co-ordination

This function provides for the activation and release of loopbacks in the LTU, the REG and the NTU.

5.1.11 Mapping between core frames and HDSL frames

This function provides for the mapping between the 144 bytes core frame and the HDSL frame(s).

5.1.12 Control of the maintenance channel

This function provides for the control of the maintenance channel formed by the HDSL frame overhead bits.

5.1.13 Synchronization and co-ordination of HDSL transceivers

This function provides for the synchronization of the HDSL transceiver systems, the equalization of different signal delays on the pairs and the correct sequence of the signals coming from the separate pairs.

5.1.14 Identification of pairs

This function provides for the marking of the pairs at the LTU/NTU by means of two or three Z bits per pair to enable the correct identification of the pairs.

5.1.15 Correction of pair identification

This function provides for the realignment of the identification of pairs if an unintentional interchange of pairs has occurred and was detected by the NTU.

5.1.16 Remote power feeding

This optional function provides for remote power feeding of either the NTU (if no REG is provided) or the REG from the LTU via the pairs.

5.1.17 Wetting current

This optional function provides for feeding of a low current on the pairs to mitigate the effect of corrosion of contacts.

5.2 Transmission medium

5.2.1 Description

The transmission medium over which the digital transmission system is expected to operate is the local line distribution network.

A local line distribution network employs cables of pairs to provide services to customers.

In a local line distribution network, customers are connected to the local exchange via local lines.

A metallic local line is able to simultaneously carry bi-directional digital information in the appropriate HDSL format.

To simplify the provision of HDSL, a digital transmission system shall be capable of satisfactory operation over the majority of metallic local lines without requirement of any special conditioning. In order to permit the use of HDSL transmission systems on the maximum possible number of local lines, the restrictions imposed by HDSL requirements are kept to the minimum necessary to guarantee acceptable operation.

5.2.2 Minimum Digital Local Line (DLL) requirements for HDSL applications

No loading coils.

Only twisted pair or quad cable.

No additional shielding necessary.

When bridged taps are present, the maximum number shall be limited to 2 and the length of each to 500 m.

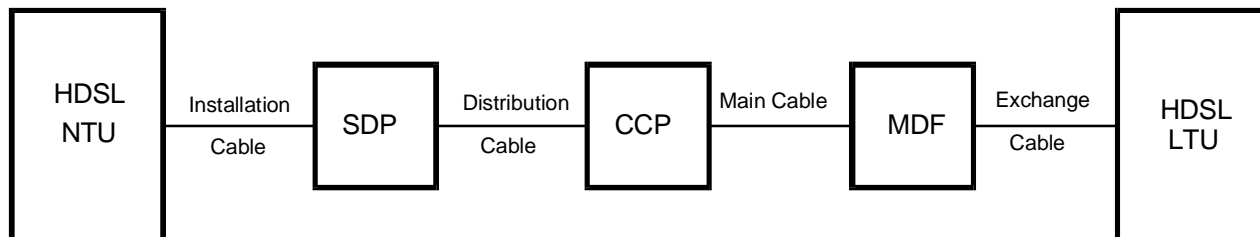
5.2.3 DLL physical characteristics

A DLL is constructed of one or more cable sections that are spliced or interconnected together.

The distribution or main cable is structured as follows:

- cascade of cable sections of different diameters and lengths;
- up to two bridged taps (BTs) may exist at various points in installation and distribution cables.

A general description of the DLL physical model is shown in figure 4 and typical examples of cable characteristics based on ETR 080 [6] are given in table 1.



CCP: Cross Connect Point.
MDF: Main Distribution Frame.
SDP: Subscriber Distribution Point.

Figure 4: DLL physical model

Table 1: Cable characteristics

	Exchange cable	Main cable	Distribution cable	Installation cable
Wire diameter (mm)	0,5; 0,6; 0,32; 0,4	0,3 to 1,4	0,3 to 1,4	0,4; 0,5; 0,6; 0,8; 0,9; 0,63
Structure	SQ (B) or TP (L)	SQ (B) or TP (L)	SQ (B) or TP (L)	SQ or TP or UP
Maximum number of pairs	1 200	2 400 (0,4 mm) 4 800 (0,32 mm)	600 (0,4 mm)	2 (aerial) 600 (in house)
Installation		underground in ducts	underground or aerial	aerial (drop) in ducts (in house)
Capacitance (nF/km at 800 Hz)	55 to 120	25 to 60	25 to 60	35 to 120
Wire insulation	PVC, FRPE	PE, paper pulp	paper, PE, Cell PE	PE, PVC
Key:	TP: Twisted Pairs SQ: Star Quads UP: Untwisted Pairs L: Layer B: Bundles (units)		PE: Polyethylene PVC: Polyvinylchloride Pulp: Pulp of paper Cell PE: Cellular Foam Polyethylene FRPE: Fire Resistant PE	
NOTE:	This table is intended to describe the cables presently installed in the local loop. Not all of the above cable types are suitable for HDSL systems.			

5.2.4 DLL electrical characteristics

The transmitted signal will suffer from impairments due to crosstalk, impulsive noise and the non-linear variation with frequency of DLL characteristics. These impairments are described in more detail in the following subclauses.

5.2.4.1 Principal characteristics

The principal electrical characteristics varying nonlinearly with frequency are:

- insertion loss;

- group delay;
- characteristic impedance, comprising real and imaginary parts.

The maximum value for insertion loss specified for HDSL transmission systems is defined in clause 6, for the one, two and three pair systems.

NOTE: The term group delay is defined in CCITT Fascicle I.3 [8].

5.2.4.2 Differences in physical transmission characteristics between pairs in the DLL

Between the LTU and NTU the characteristics of the pairs may differ. This difference may be in wire diameter, insulation type, length, number and length of bridged taps and exposure to impairments. These differences in transmission characteristics may change with time.

The common circuitry shall compensate for any differences in the transmission time due to these pair differences (see clause 6).

It is recommended that the difference of signal transfer delay between each of the two or three pairs is limited to a maximum of 50 μ s at 150 kHz, corresponding to about 10 km difference in line length between LTU and NTU.

5.2.4.3 Crosstalk characteristics

Crosstalk noise in general results due to finite coupling loss between pairs sharing the same cable, especially those pairs that are physically adjacent. Finite coupling loss between pairs causes a vestige of the signal flowing on one DLL (disturber DLL) to be coupled into an adjacent DLL (disturbed DLL). This vestige is known as crosstalk noise.

Near-end crosstalk (NEXT) is assumed to be the dominant type of crosstalk.

Intersystem NEXT results when pairs carrying different digital transmission systems interfere with each other.

Intrasystem NEXT or self-NEXT results when all pairs interfering with each other in a cable are carrying the same digital transmission system. Intrasystem NEXT noise coupled into a disturbed DLL from a number of DLL disturbers can be represented as being due to an equivalent single disturber DLL with a coupling loss versus frequency characteristics known as Power Sum Loss (PSL). Values for 1 % worst case NEXT loss vary from 40 dB to 70 dB at 150 kHz depending upon the cable type, number of disturbers and environment.

For testing HDSL systems the NEXT is represented by an artificial noise as defined in clause 6.

5.2.4.4 Unbalance about earth

The DLL will have finite balance about earth. Unbalance about earth is described in terms of longitudinal conversion loss (LCL). The expected worst case value is 42,5 dB at 150 kHz decreasing with frequency by 5 dB/decade.

5.2.4.5 Impulse noise

The DLL will have impulse noise resulting from other systems sharing the same cables as well as from other sources. The requirement for tolerance to impulse noise is described in detail in clause 6.

5.2.4.6 Micro-interruptions

A micro-interruption is a temporary line interruption due to external mechanical action on the copper wires constituting the transmission path, for example, at a cable splice. Splices can be hand-made wire-to-wire junctions, and during cable life oxidation phenomena and mechanical vibrations can induce micro-interruptions at these critical points.

The effect of a micro-interruption on the transmission system can be a failure of the digital transmission link, together with a failure of the power feeding (if provided) for the duration of the micro-interruption.

The objective is that in the presence of a micro-interruption of specified maximum length the system should not reset, and the system should automatically reactivate with a complete start-up procedure if a reset occurs due to an interruption. The requirements for tolerance to micro-interruptions, together with guidelines for a laboratory susceptibility test set are given in clause 6.

5.3 Transmission method

5.3.1 General

The transmission system provides for duplex transmission on 2-wire metallic local lines. Duplex transmission shall be achieved through the use of an Echo Cancellation Hybrid (ECH). With the echo cancellation method, illustrated in figure 5, the echo canceller (EC) produces a replica of the echo of the transmitted signal that is subtracted from the total received signal. The echo is the result of imperfect balance of the hybrid and impedance discontinuities, caused e.g. by splicing different kind of cables.

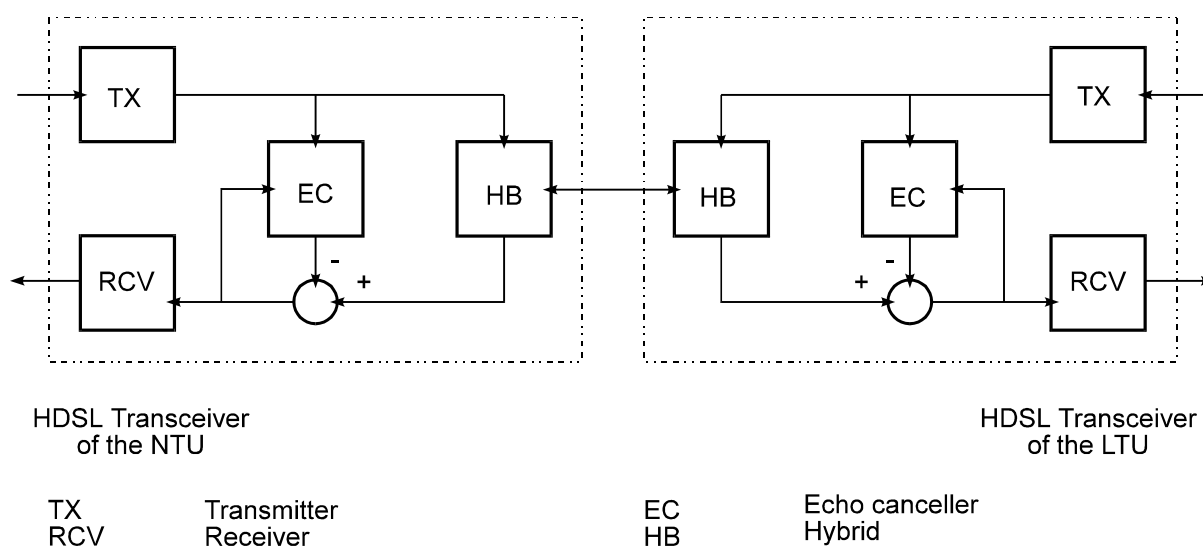


Figure 5: Functional diagram of echo cancellation method

5.3.2 Transmission on three pairs

Transmission on three DLLs is provided by three parallel HDSL transceivers, each operating at 784 kbit/s and using 2B1Q line code.

5.3.3 Transmission on two pairs

Transmission on two DLLs is provided by two parallel HDSL transceivers, each operating at 1 168 kbit/s and using 2B1Q line code.

5.3.4 Transmission on one pair

Transmission on one DLLs is provided by one HDSL transceiver operating at 2 320 kbit/s and using 2B1Q line code.

5.3.5 Transmission on four pairs

The transmission of the complete core frame on four pairs is not excluded, but is not at present treated here.

5.3.6 Line code

The line code shall be 2B1Q.

Before transmission the bit stream in each HDSL transceiver of figure 1, except the synchronization word which has a fixed pattern, shall be grouped into pairs of bits which are converted to quaternary symbols (quats) as specified in table 2. At the receiver, the inverse operations are performed.

Table 2: 2B1Q coding

First bit (sign)	Second bit (magnitude)	Quaternary symbol
1	0	+3
1	1	+1
0	1	-1
0	0	-3

5.3.7 Line baud rate

The baud rate of the HDSL transceiver shall be:

- 392 kbaud \pm 32 ppm for a three pair system;
- 584 kbaud \pm 32 ppm for a two pair system; and
- 1 160 kbaud \pm 32 ppm for a one pair system.

5.4 Frame structure

5.4.1 Core frame

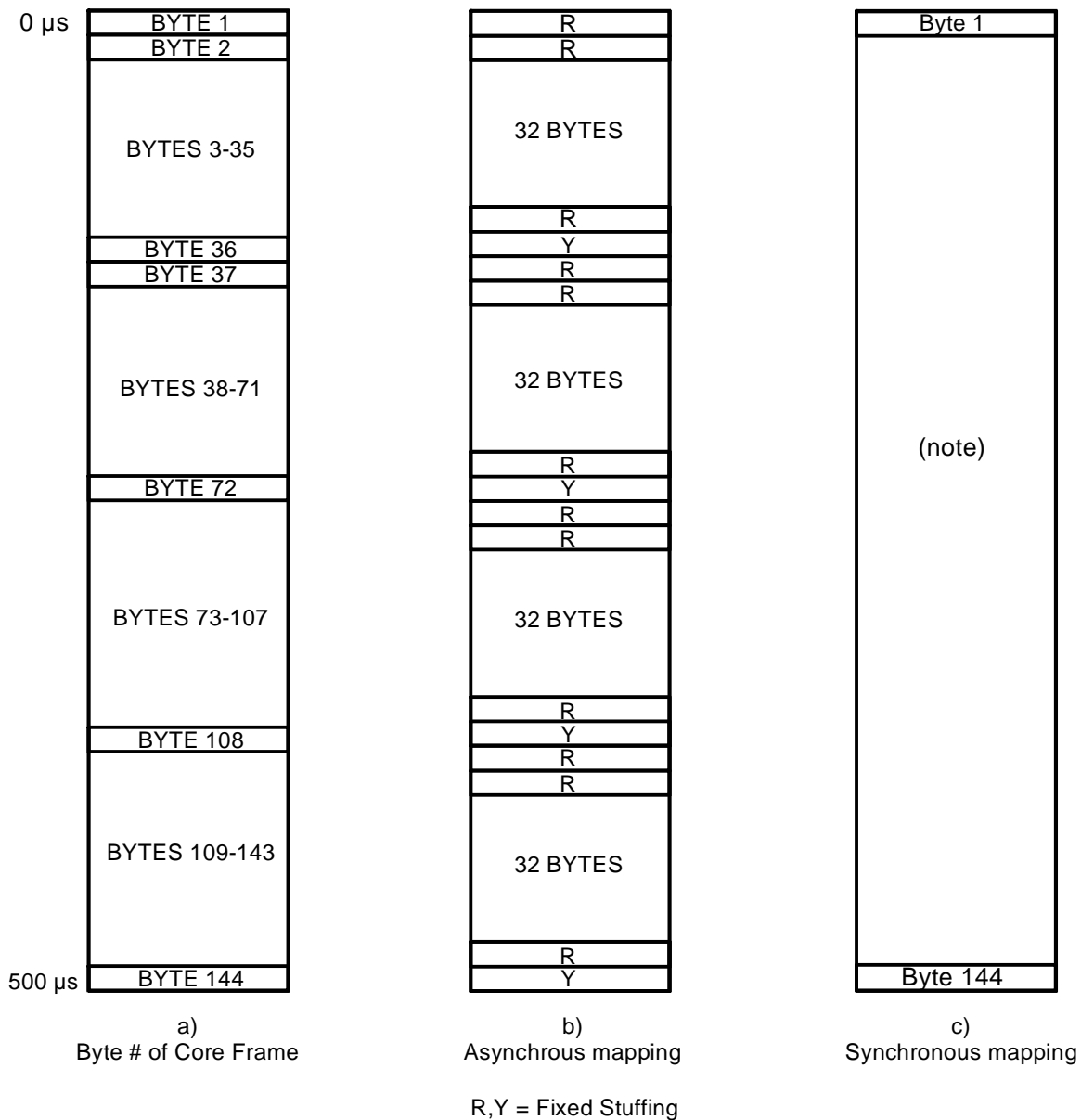
Inside the mapping functional block, as indicated in the reference configuration figure 3, the application dependent frame containing the payload is inserted into a 500 μ s long core frame containing 144 bytes as shown in figure 6. Different mapping options depending on the special applications exist, as shown in figure 6. The details of the mapping procedures for the different applications are described in clause 7. The core frames with 144 bytes/500 μ s form a continuous bit stream with a bit rate of 2 304 kbit/s which in two or three pair systems are split on a byte per byte basis into parallel HDSL frames which are transmitted in each one of the HDSL transceiver systems.

5.4.2 2B1Q HDSL frame

This subclause describes the proposed HDSL frame structure in the binary format before scrambling and encoding. This structure is valid during normal operation after symbol timing synchronization, frame alignment and after all internal transceiver coefficients have been stabilized sufficiently to permit a reliable transport of the signals through the HDSL transceiver systems:

- the nominal HDSL frame length is 6 ms;
- the mean length of the HDSL frame for the three pair system is 2 352 quats (equivalent to 4 704 bits) in 6 ms. Each individual frame contains either 0 or 2 stuffing quats which gives a real length of 2 351 quats in $6 - 1/392$ ms or 2 353 quats in $6 + 1/392$ ms;
- the mean length of the HDSL frame for the two pair system is 3 504 quats (equivalent to 7 008 bits) in 6 ms. Each individual frame contains either 0 or 2 stuffing quats which gives a real length of 3 503 quats in $6 - 1/584$ ms or 3 505 quats in $6 + 1/584$ ms;
- the mean length of the HDSL frame for the one pair system is 6 960 quats (equivalent to 13 920 bits) in 6 ms. Each individual frame contains either 0 or 2 stuffing quats which gives a real length of 6 959 quats in $6 - 1/1\,160$ ms or 6 961 quats in $6 + 1/1\,160$ ms;
- the bit assignment in each HDSL frame in each direction of transmission for all pairs is shown in tables 3, 4 and 5;
- the HDSL transceiver systems shall each independently accommodate differences in the bit timing of the two directions of transmission or of the application data and the HDSL transceiver system by including none or two stuffing quats at the end of the HDSL frame;

- in the LTU the frame rate on the different pairs shall be derived from the same source. The location of the synchronization word, i.e. the start of the HDSL frames in the different pairs shall be synchronized to each other. The maximum delay between the start of the frames shall be less than one symbol period, measured at the line side of each HDSL transceiver;
- the insertion of stuffing quats, if necessary shall be identical for all pairs.



NOTE: The Core Frame and the payload are synchronized. The details of the application dependent time slot allocation are given in the relevant subclauses of clause 7.

Figure 6: Core frame

Table 3: HDSL frame structure for the three pair system

Time	Frame bit #	HOH bit#	Abbreviated name	Full name	Notes
0 ms	1 to 14	1 to 14	SW 1 to 14	Sync word	Double Barker Code
	15	15	losd	loss of input signal at the far end application interface	
	16	16	febe	far end block error	
	17 to 1 180	-----	B01 to B12	Payload block 1 to 12	HDSL payload including Z _{m1} to Z _{m12}
	1 181	17	eoc01	eoc address	
	1 182	18	eoc02	eoc address	
	1 183	19	eoc03	eoc data/opcode	
	1 184	20	eoc04	eoc Odd/Even Byte	
	1 185	21	crc1	cyclic redundancy check	CRC-6
	1 186	22	crc2	cyclic redundancy check	CRC-6
	1 187	23	ps1	NTU power status bit 1	NTU → LTU only
	1 188	24	ps2	NTU power status bit 2	NTU → LTU only
	1 189	25	bpv	bipolar violation	
	1 190	26	eoc05	eoc unspecified	
	1 191 to 2 354	-----	B13 to B24	Payload blocks 13 to 24	HDSL payload including Z _{m13} to Z _{m24}
	2 355	27	eoc06	eoc message bit 1	
	2 356	28	eoc07	eoc message bit 2	
	2 357	29	eoc08	eoc message bit 3	
	2 358	30	eoc09	eoc message bit 4	
	2 359	31	crc3	cyclic redundancy check	CRC-6
	2 360	32	crc4	cyclic redundancy check	CRC-6
	2 361	33	hrp	regenerator present	LTU ← REG → NTU
	2 362	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	2 363	35	rcbe	regenerator central block error	LTU ← REG → NTU
	2 364	36	rega	regenerator alarm	LTU ← REG → NTU
	2 365 to 3 528	-----	B25 to B36	Payload blocks 25 to 36	HDSL payload including Z _{m25} to Z _{m36}
	3 529	37	eoc10	eoc message bit 5	
	3 530	38	eoc11	eoc message bit 6	
	3 531	39	eoc12	eoc message bit 7	
	3 532	40	eoc13	eoc message bit 8	
	3 533	41	crc5	cyclic redundancy check	CRC-6
	3 534	42	crc6	cyclic redundancy check	CRC-6
	3 535	43	rta	remote terminal alarm	NTU → LTU only
	3 536	44	indc/indr	ready to receive	indc=LTU → NTU indr=NTU → LTU
	3 537	45	uib	unspecified indicator bit	
	3 538	46	uib	unspecified indicator bit	
6 - 1/392 ms	3 539 to 4 702	-----	B37 to B48	Payload blocks 37 to 48	HDSL Payload including Z _{m37} to Z _{m48}
	4 703	47	stq1s	stuff quat 1 sign	Frame stuffing
6 ms nominal	4 704	48	stq1m	stuff quat 1 magnitude	Frame stuffing
	4 705	49	stq2s	stuff quat 2 sign	Frame stuffing
6 + 1/392 ms	4 706	50	stq2m	stuff quat 2 magnitude	Frame stuffing

Table 4: HDSL frame structure for the two pair system

Time	Frame bit #	HOH bit#	Abbreviated name	Full name	Notes
0 ms	1 to 14	1 to 14	SW 1 to 14	Sync word	Double Barker Code
	15	15	losd	loss of input signal at the far end application interface	
	16	16	febe	far end block error	
	17 to 1 756	-----	B01 to B12	Payload block 1 to 12	HDSL payload including Z _{m1} to Z _{m12}
	1 757	17	eoc01	eoc address	
	1 758	18	eoc02	eoc address	
	1 759	19	eoc03	eoc data/opcode	
	1 760	20	eoc04	eoc Odd/Even Byte	
	1 761	21	crc1	cyclic redundancy check	CRC-6
	1 762	22	crc2	cyclic redundancy check	CRC-6
	1 763	23	ps1	NTU power status bit 1	NTU → LTU only
	1 764	24	ps2	NTU power status bit 2	NTU → LTU only
	1 765	25	bpv	bipolar violation	
	1 766	26	eoc05	eoc unspecified	
	1 767 to 3 506	-----	B13 to B24	Payload blocks 13 to 24	HDSL payload including Z _{m13} to Z _{m24}
	3 507	27	eoc06	eoc message bit 1	
	3 508	28	eoc07	eoc message bit 2	
	3 509	29	eoc08	eoc message bit 3	
	3 510	30	eoc09	eoc message bit 4	
	3 511	31	crc3	cyclic redundancy check	CRC-6
	3 512	32	crc4	cyclic redundancy check	CRC-6
	3 513	33	hrp	regenerator present	LTU ← REG → NTU
	3 514	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	3 515	35	rcbe	regenerator central block error	LTU ← REG → NTU
	3 516	36	rega	regenerator alarm	LTU ← REG → NTU
	3 517 to 5 256	-----	B25 to B36	Payload blocks 25 to 36	HDSL payload including Z _{m25} to Z _{m36}
	5 257	37	eoc10	eoc message bit 5	
	5 258	38	eoc11	eoc message bit 6	
	5 259	39	eoc12	eoc message bit 7	
	5 260	40	eoc13	eoc message bit 8	
	5 261	41	crc5	cyclic redundancy check	CRC-6
	5 262	42	crc6	cyclic redundancy check	CRC-6
	5 263	43	rta	remote terminal alarm	NTU → LTU only
	5 264	44	indc/indr	ready to receive	indc=LTU → NTU indr=NTU → LTU
	5 265	45	uib	unspecified indicator bit	
	5 266	46	uib	unspecified indicator bit	
6 - 1/584 ms	5 267 to 7 006	-----	B37 to B48	Payload blocks 37 to 48	HDSL payload including Z _{m37} to Z _{m48}
	7 007	47	stq1s	stuff quat 1 sign	Frame stuffing
6 ms nominal	7 008	48	stq1m	stuff quat 1 magnitude	Frame stuffing
	7 009	49	stq2s	stuff quat 2 sign	Frame stuffing
6 + 1/584 ms	7 010	50	stq2m	stuff quat 2 magnitude	Frame stuffing

Table 5: HDSL frame structure for the one pair system

Time	Frame bit #	HOH bit #	Abbreviated name	Full name	Notes
0 ms	1 to 14	1 to 14	SW 1 to 14	Sync word	
	15	15	losd	loss of input signal at the far end application interface	
	16	16	febe	far end block error	
	17 to 3 484	-----	B01 to B12	Payload blocks 1 to 12	HDSL payload including Z_{m1} to Z_{m12}
	3 485	17	eoc01	eoc address	
	3 486	18	eoc02	eoc address	
	3 487	19	eoc03	eoc data/opcode	
	3 488	20	eoc04	eoc/Odd/Even Byte	
	3 489	21	crc1	cyclic redundancy check	CRC-6
	3 490	22	crc2	cyclic redundancy check	CRC-6
	3 491	23	ps1	NTU power status bit 1	NTU → LTU only
	3 492	24	ps2	NTU power status bit 1	NTU → LTU only
	3 493	25	bpv	bipolar violation	
	3 494	26	eoc05	eoc unspecified	
	3 495 to 6 962	-----	B13 to B24	Payload blocks 13 to 24	HDSL payload including Z_{m13} to Z_{m24}
	6 963	27	eoc06	eoc message bit 1	
	6 964	28	eoc07	eoc message bit 2	
	6 965	29	eoc08	eoc message bit 3	
	6 966	30	eoc09	eoc message bit 4	
	6 967	31	crc3	cyclic redundancy check	CRC-6
	6 968	32	crc4	cyclic redundancy check	CRC-6
	6 969	33	hrp	regenerator present	LTU ← REG → NTU
	6 970	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	6 971	35	rcbe	regenerator central block error	LTU ← REG → NTU
	6 972	36	rega	regenerator alarm	LTU ← REG → NTU
	6 973 to 10 440	-----	B25 to B36	Payload blocks 25 to 36	HDSL payload including Z_{m25} to Z_{m36}
	10 441	37	eoc10	eoc message bit 5	
	10 442	38	eoc11	eoc message bit 6	
	10 443	39	eoc12	eoc message bit 7	
	10 444	40	eoc13	eoc message bit 8	
	10 445	41	crc5	cyclic redundancy check	CRC-6
	10 446	42	crc6	cyclic redundancy check	CRC-6
	10 447	43	rta	remote terminal alarm	NTU → LTU only
	10 448	44	indc/indr	ready to receive	indc = LTU → NTU indr = NTU → LTU
	10 449	45	uib	unspecified indicator bit	
	10 450	46	uib	unspecified indicator bit	
6 - 1/1 160 ms	10 451 to 13 918	-----	B37 to B48	Payload blocks 37 to 48	HDSL payload including Z_{m37} to Z_{m48}
	13 919	47	stq1s	stuff quat 1 sign	Frame stuffing
6 ms nominal	13 920	48	stq1m	stuff quat 1 magnitude	Frame stuffing
	13 921	49	stq2s	stuff quat 2 sign	Frame stuffing
6 + 1/1 160 ms	13 922	50	stq2m	stuff quat 2 magnitude	Frame stuffing

5.4.2.1 2B1Q HDSL frame structure

5.4.2.1.1 Frame structure of the three pair system

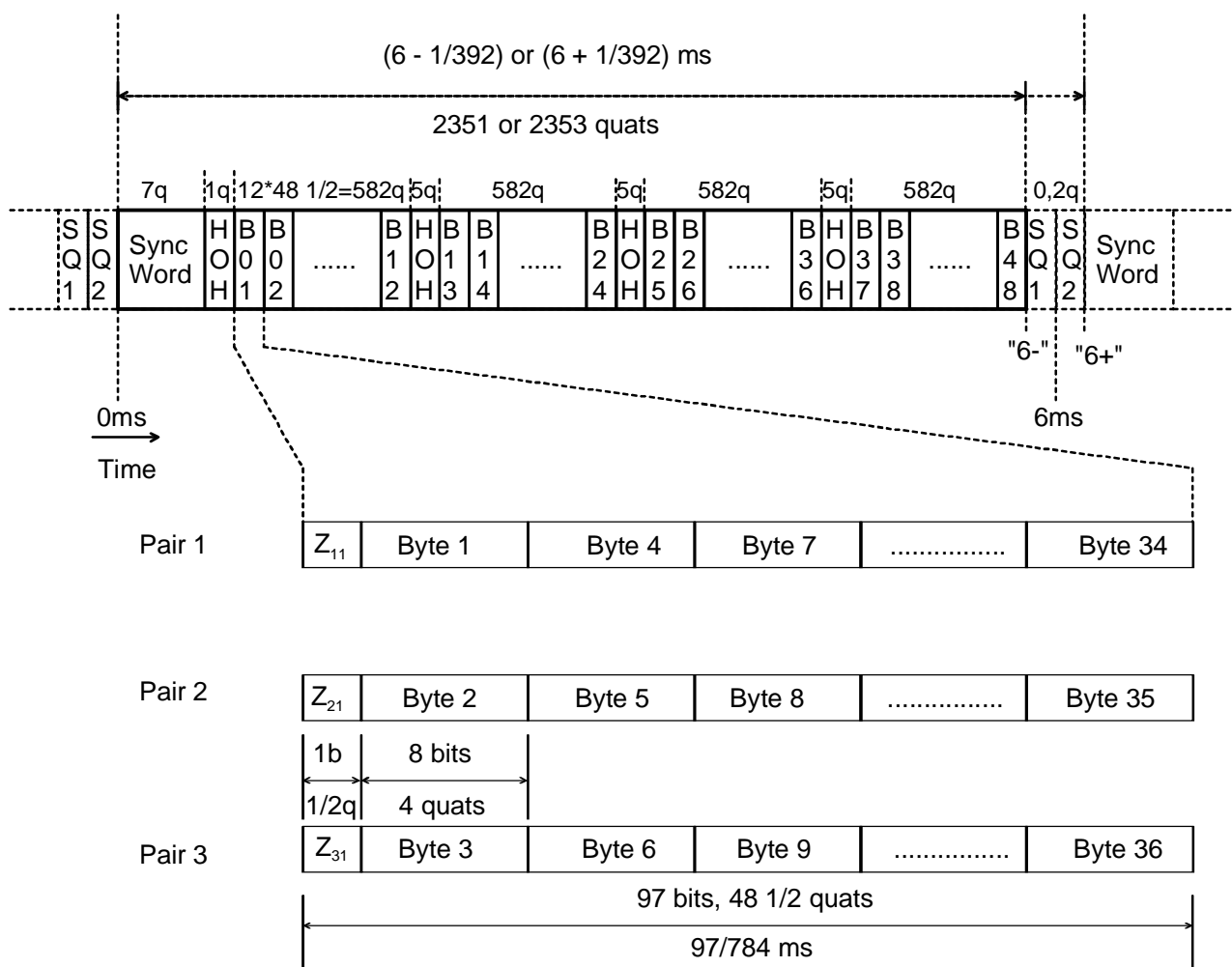
Figure 7 illustrates the HDSL frame structure composed of quaternary symbols (quats) and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the seven symbols long synchronization word followed by one HDSL overhead quat and 12 blocks of HDSL payload, each consisting of 48,5 quats, equivalent to 97 bits, containing one overhead-bit Z_{mn} and 12 bytes of the core frame. The Z_{mn} -bits ($m = 1$ to 3 indicates one of the three pairs; $n = 1$ to 48 is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which 48 bits per frame of each HDSL transceiver system at a capacity of 8 kbit/s are available.

The first eight Z-bits (Z_{m1} to Z_{m8}) are reserved for core applications. Bits Z_{m1} to Z_{m3} are used for pair identification (see subclause 6.2), whereas Z_{m4} to Z_{m8} are reserved for future use and are presently set to ONE.

The Z-bits 9 to 48 (Z_{m9} to Z_{m48}) are application dependent and are transparently transported through the HDSL core. The use of these bits is described in clause 7 for the application specific requirements.

The three groups following the first group have an equal structure. Each consists of five HDSL overhead quats and 12 HDSL payload blocks as described above. So one frame contains a synchronization word, 16 HDSL overhead quats, 48 Z-bits and 576 bytes of the core frame.

At the end of the frame the possibility of 2 stuffing quats is foreseen. These quats are used always together, this means either none or two stuffing quats are inserted, depending on the relation of the timing. The length of the HDSL frame is either 2 353 quats, which equals $6 + 1/392$ ms for the nominal HDSL clock frequency, or 2 351 quats corresponding to $6 - 1/392$ ms and the average will tend to 2 352 quats or 6 ms. The receiver is able to evaluate the length of an incoming frame by detection of the sync word in the following frame and to adjust the demultiplexing of the data stream.



HDSL Payload Block (48 per HDSL frame)

Symbol	Name, function
B01 to B48	HDSL system payload blocks
Byte n	Byte n from core frame (n = 1 to 144)
HOH	HDSL overhead (sw, eoc, crc,...)
quat	Quaternary symbol
SQ1, SQ2	Stuff quats
Sync word	7-symbol Barker codes, "double Barker" → 14 bits
"6-", "6+"	6 - 1/392 ms, 6+1/392 ms
Z _{mn}	Additional overhead bits (Z-bits)
m	Indicating corresponding pair (m = 1 to 3)
n	Indicating number of payload block (n = 1 to 48)

Figure 7: Frame structure of the three pair system

5.4.2.1.2 Frame structure of the two pair system

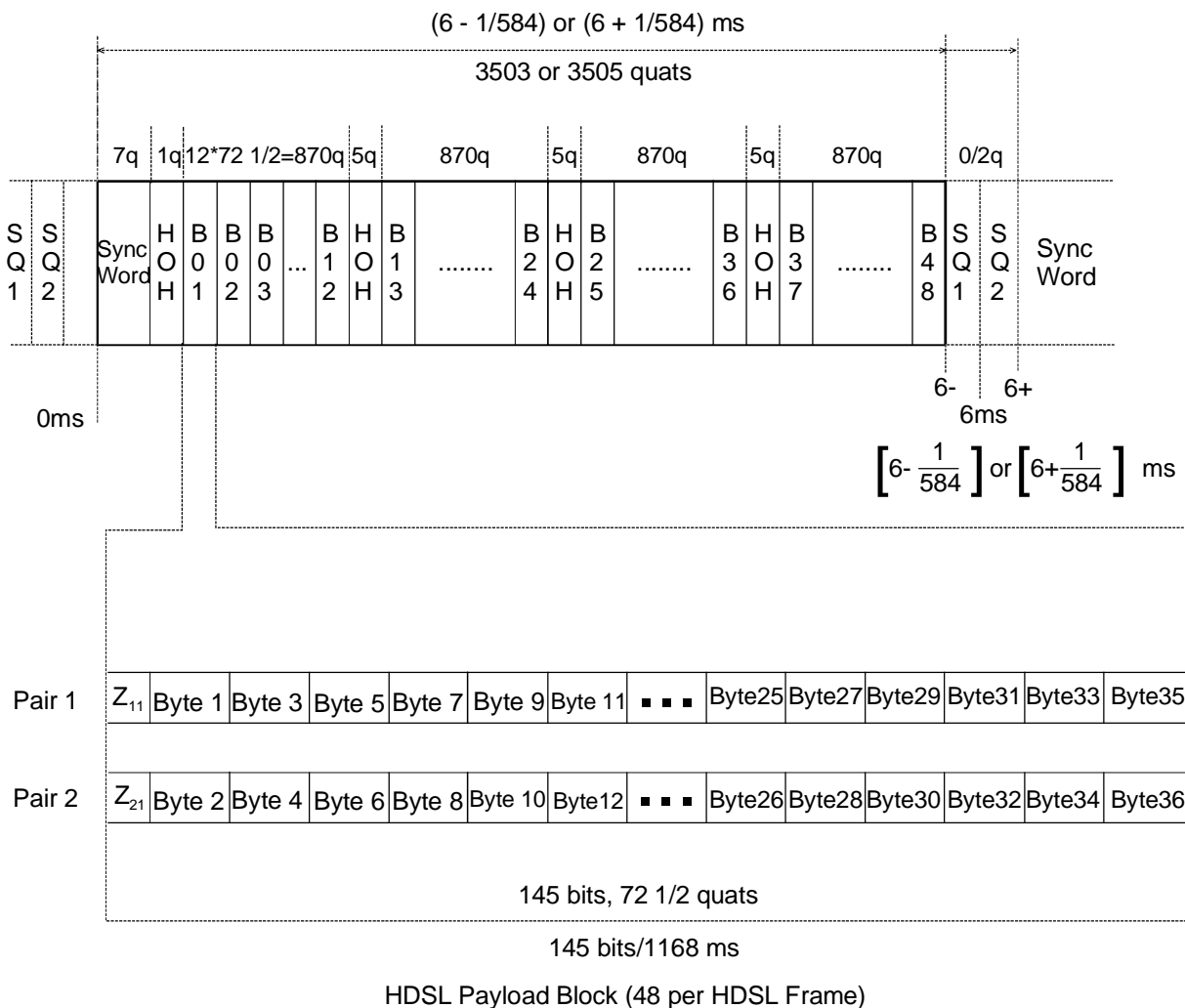
Figure 8 illustrates the HDSL frame structure composed of quaternary symbols (quats) and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the seven symbols long synchronization word followed by one HDSL overhead quat and 12 blocks of HDSL payload, each consisting of 72,5 quats, equivalent to 145 bits, containing one overhead-bit Z_{mn} and 18 bytes of the core frame. The Z_{mn}-bits (m = 1, 2 indicates one of the two pairs; n = 1 to 48 is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which 48 bits per frame of each HDSL transceiver system at a capacity of 8 kbit/s are available.

The first eight Z-bits (Z_{m1} to Z_{m8}) are reserved for core applications. Bits Z_{m1}, Z_{m2} are used for pair identification (see subclause 6.2), whereas Z_{m3} to Z_{m8} are reserved for future use and are presently set to ONE.

The Z-bits 9 to 48 (Z_{m9} to Z_{m48}) are application dependent and are transparently transported through the HDSL core. The use of these bits is described in clause 7 for the application specific requirements.

The three groups following the first group have an equal structure. Each consists of five HDSL overhead quats and 12 HDSL payload blocks as described above. So one frame contains a synchronization word, 16 HDSL overhead quats, 48 Z-bits and 864 bytes of the core frame.

At the end of the frame the possibility of 2 stuffing quats is foreseen. These quats are used always together; this means either none or two stuffing quats are inserted, depending on the relation of the timing. The length of the HDSL frame is either 3 505 quats, which equals $6 + 1/584$ ms for the nominal HDSL clock frequency, or 3 503 quats corresponding to $6 - 1/584$ ms and the average will tend to 3 504 quats or 6 ms. The receiver is able to evaluate the length of an incoming frame by detection of the sync word in the following frame and to adjust the demultiplexing of the data stream.



Symbol	Name, function
B01 to B48	HDSL system payload blocks
Byte n	Byte n from core frame (n = 1 to 144)
HOH	HDSL overhead (sw, eoc, crc,...)
quat	Quaternary symbol
SQ1, SQ2	Stuff quats
Sync word	7-symbol Barker codes, "double Barker" → 14 bits
"6-", "6+"	6 - 1/584 ms, 6+1/584 ms
Z _{mn}	Additional overhead bits (Z-bits)
m	Indicating corresponding pair (m = 1 to 2)
n	Indicating number of payload block (n = 1 to 48)

Figure 8: Frame structure of the two pair system

5.4.2.1.3 Frame structure of the one pair system

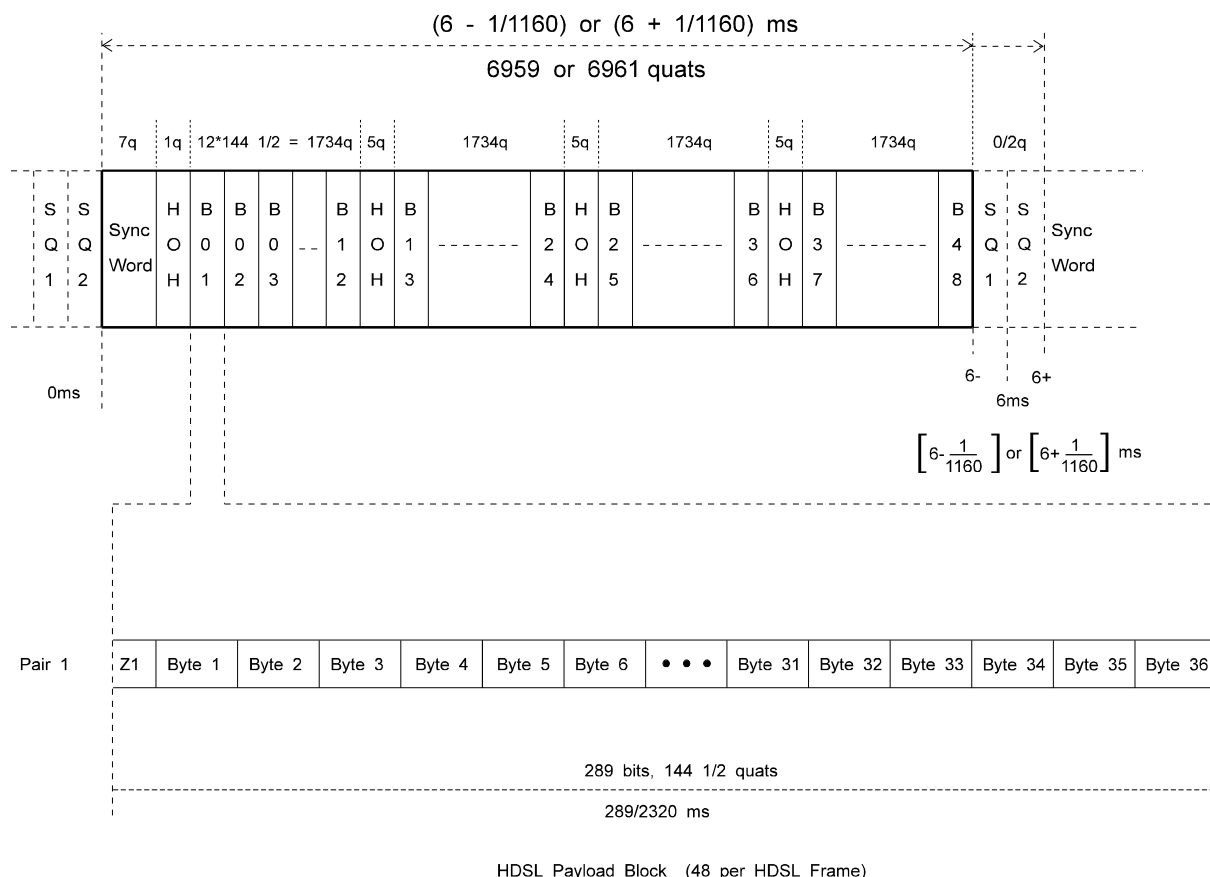
Figure 9 illustrates the HDSL frame structure composed of quaternary symbols (quats) and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the seven symbols long synchronization word followed by one HDSL overhead quat and 12 blocks of HDSL payload, each consisting of 144,5 quats, equivalent to 289 bits, containing one overhead-bit Z_n and thirty-6 bytes of the core frame. The Z_n -bits ($n = 1$ to 48 is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which 48 bits of the HDSL frame at a capacity of 8 kbit/s are available.

The first eight Z-bits (Z_1 to Z_8) are reserved for future core applications and presently set to ONE.

The Z-bits 9 to 48 (Z_9 to Z_{48}) are application dependent and are transparently transported through the HDSL core. The use of these bits is described in clause 7 for the application specific requirements.

The three groups following the first group have an equal structure. Each consists of five HDSL overhead quats and 12 HDSL payload blocks as described above. So one frame contains a synchronization word, 16 HDSL overhead quats, 48 Z-bits and 1 728 bytes of the core frame.

At the end of the frame the possibility of 2 stuffing quats is foreseen. These quats are used always together, this means either none or two stuffing quats are inserted, depending on the relation of the timing. The length of the HDSL frame is either 6 961 quats, which equals $6 + 1/160$ ms for the nominal HDSL clock frequency, or 6 959 quats corresponding to $6 - 1/160$ ms and the average will tend to 6 960 quats or 6 ms. The receiver is able to evaluate the length of an incoming frame by detection of the sync word in the following frame and to adjust the demultiplexing of the data stream.



Symbol	Name, function
B01 to B48	HDSL system payload blocks
Byte n	Byte n from core frame (n = 1 to 144)
HOH	HDSL overhead (sw, eoc, crc,...)
quat	Quaternary symbol
SQ1, SQ2	Stuff quats
Sync word	7-symbol Barker codes, "double Barker" → 14 bits
"6-", "6+"	6 - 1/1 160 ms, 6+1/1 160 ms
Z _n	Additional overhead bits (Z-bits)
n	Indicating number of payload block (n = 1 to 48)

Figure 9: Frame structure of the one pair system

5.4.2.2 Frame bit assignments

In tables 3, 4 and 5 the bit sequence of the HDSL frame prior to scrambling at the transmit side and after descrambling at the receive side is presented. While the frame structures are identical in both directions of transmission, the functional assignments of individual bits in the direction LTU to NTU or NTU to LTU are different. Unused bits in either direction are set to ONE. For example the proposed NTU power status bits are defined only in the frame transmitted towards the LTU and the corresponding bit positions in the reverse direction have no assignment. The bit assignments are identical in each of the pairs.

The following gives a short description of the currently defined overhead bits.

- Sync word:

The synchronization words (sync words) enable the HDSL receivers to acquire quat and bit timing so that the incoming signals can be decoded into their original binary forms. The synchronization words shall be seven-quat Barker code sequences as shown in table 6. The same sequence is used in both directions on all pairs.

Table 6: Seven-quat Barker code synchronization word sequence

Quat #	sequence
01	+3
02	+3
03	+3
04	-3
05	-3
06	+3
07	-3

NOTE 1: The coding in table 6 will preserve the 2,50 V (one pair) or 2,64 V (two and three pair) peak symbol levels for the sync words on the line.

- losd-bit (loss of signal):

If there is no signal from the application interface, the losd-bit shall be set to ZERO in the next frame towards the far end. Under normal conditions, this bit shall be set to ONE.

- febe-bit (far end block error):

The febe-bit shall be set to ZERO in the following frame towards the far end, when the local receiver detects a CRC error in the HDSL frame. When there is no febe bit value ready (due to different frame lengths in the two directions) or no failure has been detected in the previous frame, the febe bit shall be set to ONE.

- eoc-bits (embedded operations channel):

13 bits (eoc01 to eoc13) are provided as a separate maintenance channel. For a description of codes and the used procedures in this channel, see subclause 5.5.

- crc-bits:

The HDSL frame shall have six bits assigned to a cyclic redundancy check (CRC) code on both directions for each pair.

The CRC code block is calculated for the previous HDSL frame in the given direction except for the fourteen sync word bits, the six crc-bits and any stuff quat bits.

The six crc-bits transmitted in the (N+1)th frame shall be determined as follows:

- 1) All bits of the Nth frame except the 14 sync word bits, the six crc-bits and any stuffing bits, for a total of m bits (m equals 4 682 for the three pair system, 6 986 for the two pair system and 13 888 for the one pair system), are used, in order of occurrence, to construct a polynomial in "X" such that the bit "0" of the Nth frame is the coefficient of the term X^{m-1} and bit m-1 of the Nth frame is the coefficient of the term X^0 .
- 2) The polynomial is multiplied by the factor X^6 , and the result is divided, modulo 2, by the generator polynomial $X^6 \oplus X \oplus 1$. The coefficients of the remainder polynomial are used, in order of occurrence, as the ordered set of check bits, crc1 through crc6, for the (N+1)th frame. The ordering is such that the coefficient of the term X^5 in the remainder polynomial is check bit crc1 and the coefficient of the term X^0 in the remainder polynomial is check bit crc6.
- 3) The check bits, crc1 through crc6, contained in a frame are those associated with the content of the preceding frame. When there is no immediately preceding frame, the check bits may be assigned any value.

- ps1-bit, ps2-bit (power supply bits):

The power supply bits ps1 and ps2 are used to indicate the status of the primary and secondary power supply in the NTU. The power status bit function definitions are shown in table 7.

Table 7: Coding of power status

NTU power status	ps1	ps2
All power normal	1	1
Secondary power out	1	0
Primary power out	0	1
Power loss	0	0

On loss of power at the NTU, there shall be enough power left to communicate three "Power loss" messages towards the LTU.

- **bpv-bit (bipolar violation):**

Whenever during one HDSL frame period, a line coding violation is detected at the application interface, the bpv-bit is set to ZERO in the following frame towards the far end. Under normal conditions, this bit shall be set to ONE.

- **hrp-bit (HDSL regenerator present):**

If a regenerator is present, the hrp-bit shall be set to ZERO by the regenerator in both directions towards the NTU and the LTU. The NTU and the LTU set the hrp bit to ONE in the outgoing frames.

- **rrbe-bit (regenerator remote block error):**

The rrbe-bit shall be set to ZERO by the regenerator towards the LTU and NTU in the next outgoing frame, when a CRC error has been detected by the receiver located at the LTU-side in the regenerator. If no failure has been detected, this bit shall be set to ONE.

- **rcbe-bit (regenerator central block error):**

The rcbe-bit shall be set to ZERO by the regenerator towards the LTU and NTU in the next outgoing frame, when a CRC error has been detected by the receiver located at the NTU-side in the regenerator. If no failure has been detected, this bit shall be set to ONE.

- **rta-bit (remote terminal alarm):**

The rta-bit is set to ZERO by the NTU to signal internal alarm conditions to the LTU. The LTU, after detecting the rta-bit, may read the status register of the NTU and evaluate the reason for the failure condition. With no alarm pending in the NTU, the rta-bit is set to ONE.

- **rega-bit (internal alarm in the regenerator):**

The rega-bit is set by the REG to signal internal alarm conditions. The LTU, after detecting the rega-bit, may read the status register of the REG and evaluate the reason for the failure condition. With no alarm pending in the REG, the rega-bit is set to ONE.

- **uib-bits (unspecified indicator bits):**

These bits are reserved for future use. They shall be set to ONE.

- **stq (stuffing quats):**

These quats (stq1_m, stq1_s, stq2_m, stq2_s) are always used together. Either none or two stuffing quats are inserted, depending on the relation of the timing between the two transmit directions. The values of the stuffing quats used are left as a choice to the individual vendors. Stuffing bits are not scrambled.

- **indc- and indr-bit (ready to receive indicator at the LTU and NTU respectively):**

These bits are set to ZERO by the respective HDSL transceiver to indicate to the distant HDSL transceiver that it is ready to receive data, in all other conditions the indc-and indr-bit will be set to ONE.

NOTE 2: The indc- and indr-bit in the HDSL frame overhead are different and not to be confused with the status indicators INDC and INDR used inside the HDSL transceivers during the start-up procedure as described in subclause 5.6.

5.4.3 Scrambling method

The HDSL transceiver systems use the same self synchronizing scrambling procedure as the 2B1Q transmission system for ISDN-BA as defined in ETR 080 [6], annex A. The data stream with exception of the 14 bits of the sync word and the stuffing bits is scrambled by means of a 23rd-order polynomial prior to encoding.

- For the direction NTU → LTU the polynomial shall be $x^{-23} \oplus x^{-18} \oplus 1$, where the sign \oplus stands for modulo 2 summation.
- For the direction LTU → NTU the polynomial shall be $x^{-23} \oplus x^{-5} \oplus 1$.
- The binary data stream is recovered in the receiver by applying the same polynomial to the scrambled data. Figure 10 illustrates block diagrams for the scramblers and descramblers.

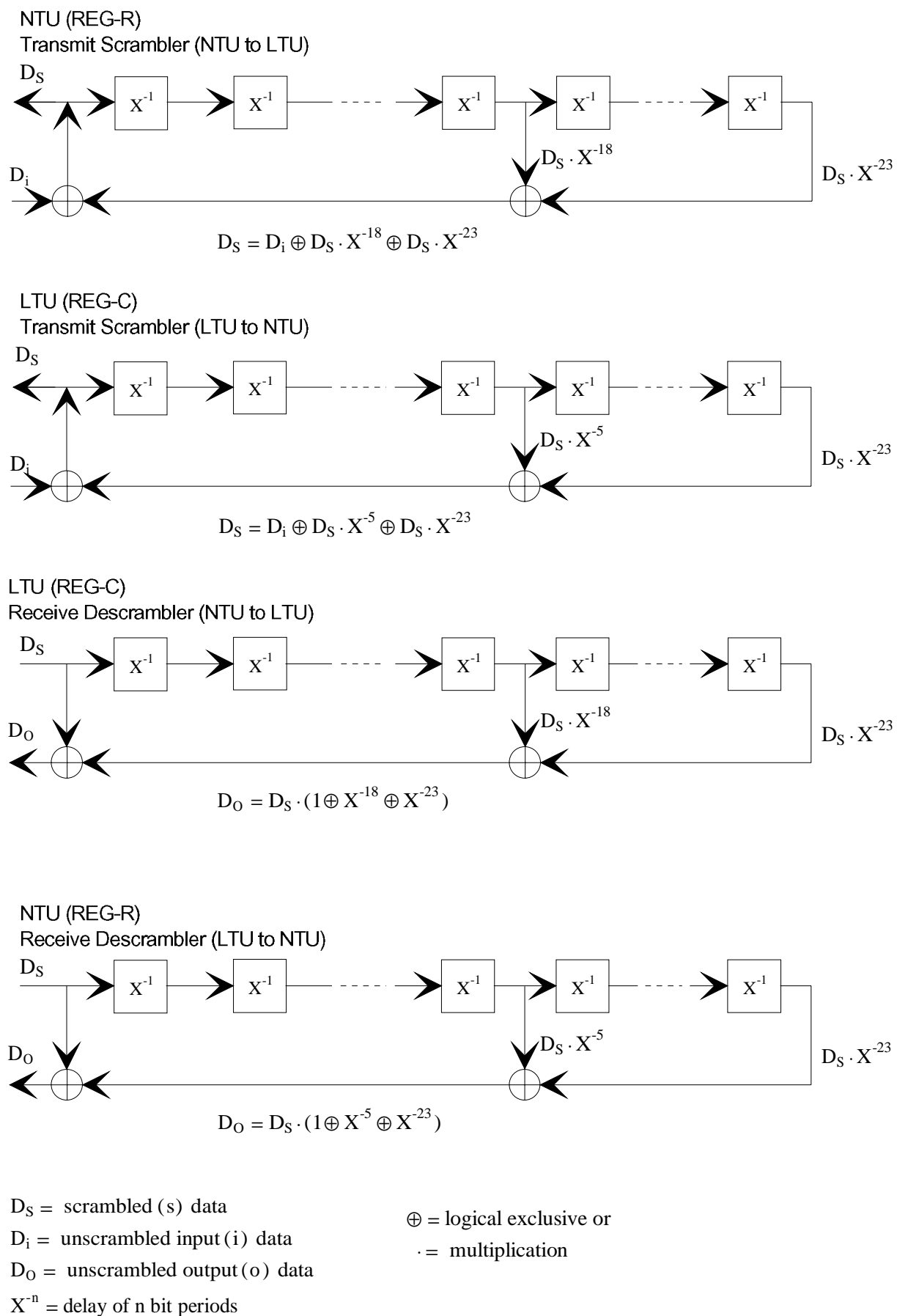


Figure 10: Scramblers and descramblers

5.5 HDSL embedded operations channel (eoc)

This subclause specifies the requirements for the embedded operations channel. 13 of the available 50 HDSL overhead bits (HOH) as shown in tables 3, 4 and 5 are used for the eoc-application and present a complete eoc-frame synchronized to the corresponding HDSL frame. The structure of each single eoc-frame is as shown in table 8 and discussed below.

Table 8: HDSL eoc frame structure

Bit position	# of bits	Description	Remarks
1, 2	2	Address	Can address 4 locations
3	1	Data (ZERO)/ Message (ONE) Indicator	
4	1	Odd (ONE)/Even (ZERO) Byte	Multibyte transmission
5	1	Unused	
6 -13 (see note)	8	Information field	256 Opcodes, 8 bits data

NOTE: eoc06 contains the MSB and eoc13 the LSB of the opcode/data as described in tables 9 to 11.

1) The address field:

- the first two bits (eoc01 & eoc02) allow for unique addressing of four network elements. The present document specifies requirements for only three locations, NTU, REG and LTU;
- the LTU address is "11" and can be considered as the eoc-master;
- the NTU and REG (if present) addresses are "00" and "10" (eoc01, eoc02) respectively, and can be considered as the addresses of the slaves;
- the address in a return echo should be set to that of the responding unit.

2) The data/message indicator bit:

- the data/message indicator bit shall be set to ONE when the information field contains the operation code for an HDSL eoc message;
- the data/message indicator bit shall be set to ZERO when the information field contains data, either binary or ASCII.

3) Odd/Even Byte:

- the "Odd Byte"/"Even Byte" field is used as follows:
 - for the first byte of data to be either read or written, the eoc04 bit is set to ONE to indicate "Odd Byte", for the next byte eoc04 is set to ZERO to indicate "Even Byte" and so on, alternately. This field is used to speed up data read and write by eliminating the need for intermediate codes to indicate to the far end that the previous byte was successfully received.

4) Unused bit:

- set to one.

5) Information field:

- up to 256 different messages or 8 bit of binary or ASCII data may be encoded in the information field.

5.5.1 Functions of the HDSL eoc

The LTU (master) sends commands to the NTU/REG (slave) to perform certain functions. Some of these functions require the slave to activate changes in the circuitry (e.g. to either loopback or send crc bits that are corrupted). Other functions can be invoked to read from and write to data registers located in the slave.

Some of these commands are "latching", meaning that a subsequent command will be required to release from this state. Thus multiple HDSL eoc-initiated actions can be in effect simultaneously. A separate command "Return to Normal"

together with the appropriate address shall be used to unlatch all latched states in the REG or the NTU. If no message is pending for both the NTU and the REG (idle state), the "Return to Normal" message shall be sent by the LTU together with the NTU-address "00". If no opcode has to be sent during a latched state the LTU may send the "Hold State" message.

The NTU, if not properly addressed, shall insert the "Hold State" message with the NTU-address "00" in the direction NTU → LTU. Normally if the REG has been addressed and its eoc-unit is working properly, this NTU message will be overwritten in the REG. In the case, the eoc-unit in the REG is unable to react (due to improper function), receiving the "Hold State" message from the NTU indicates to the LTU, that the REG is not working properly, although the messages are transported over the whole link down to the NTU.

The regenerator REG is transparent to all messages in the direction LTU → NTU, including messages addressing the regenerator itself. In the direction NTU → LTU the regenerator is transparent as long as no messages addressing the regenerator, are received. In this case, any message from the NTU in the direction NTU → LTU is overwritten, depending on the action required by the eoc message for the regenerator.

The complete set of commands is listed in table 9 and described in subclause 5.5.5.

5.5.2 HDSL eoc acknowledgement protocol

The LTU is the master of the HDSL eoc and always issues the commands. The slave responds to properly addressed messages by acknowledging to the master that the message was received correctly. Thus, the HDSL eoc protocol operates in a command/response mode with the master issuing the command and the slave responding.

Pair-specific messages shall be transmitted and acknowledged on the addressed pair only. In the slave (NTU/REG) the evaluation and the acknowledgement is carried out separately for each HDSL transceiver system (subsystem), i.e. every subsystem echoes the received eoc message independently of the code on the other subsystems.

This subsystem oriented handling of the eoc-protocol allows for a regenerator implementation based on independent modules for each pair. This general principle is also provided in the NTU, i.e. messages which require an action on a single pair (e.g. all CRC-functions, read noise margin) are executed only on those pairs, where the message has been received correctly.

Global messages, not addressing functions of a single pair, like loopback in the NTU, may be sent over all pairs in parallel or over one single pair, as selected by the LTU. The NTU will evaluate the message on one single pair only, which may be selected by monitoring the eoc for a valid global message or by any performance monitoring. The NTU, after receiving three consecutive valid messages on the selected pair, enters the corresponding state and performs the appropriate action. The acknowledgement of the received messages shall be sent over all pairs in parallel and the LTU evaluates the acknowledgement on one single pair only. So the LTU and the NTU may evaluate the messages on different pairs. In the REG, due to the pair-specific implementation, no difference exists between global and pair-specific messages. The LTU has to take care, that all individual loopbacks are activated before indicating an active loopback 1A.

Three types of responses are allowed from the slave, and thus there are three protocol states allowed on the HDSL eoc. At any time the HDSL eoc will be in one of the three protocol states, and can switch from one state to another during a message.

The three protocol states are:

- 1) message/echo-response protocol state;
- 2) message/unable to comply (UTC)-response protocol state;
- 3) message/data-response protocol state.

5.5.2.1 Message/echo response protocol state

To acknowledge a properly addressed message from the LTU, the slave (NTU or REG) responds to a received HDSL eoc message by returning identical HDSL eoc frames back to the LTU. This response procedure is termed "echoing" the HDSL eoc message. The combination of the LTU sending the HDSL eoc frame and the slave echoing the frame back comprises the message/echo-response protocol state.

To assure the validity of the message, the slave shall receive three identical, and consecutive HDSL eoc frames before activating the requested function. In this way, the transmitted HDSL eoc messages received by the slave can be assumed to be correct with high probability.

For the LTU to confirm correct reception of the message by the slave, the message is repeated until the LTU receives three identical and consecutive echoes. This serves as an implicit acknowledgement to the LTU that the slave has correctly received the transmitted message and is acting on it. This completes the command/response protocol mode.

In summary, the HDSL eoc protocol requires that the LTU transmits a message continuously until it receives three identical and consecutive echoes of the HDSL eoc frame originally transmitted.

The LTU cannot start sending a new message to the slave until the previous message on the HDSL eoc is acknowledged and the command/response protocol for that message is completed. This "one message outstanding" rule automatically eliminates HDSL eoc contention problems that may occur between NTU and REG.

An HDSL core divides the payload between two or three pairs. The rules stated previously, requiring three consecutive identical receptions of a message or an acknowledgement, apply to a single pair. That is, the message or acknowledgement shall be received three times consecutively and identically over the same pair.

Thus the following requirements apply:

- 1) only one message, under the control of the LTU, shall be outstanding (not yet acknowledged and confirmed) on the HDSL eoc at any time;
- 2) in order to cause the desired action in the slave, the LTU shall continue to send the message until it receives at least three identical consecutive HDSL eoc frames from the slave over one pair. This shall constitute an acknowledgement to the LTU that the slave received the transmitted message correctly;
- 3) for non-latching conditions the LTU shall after the receipt of the three valid echoes continuously send the activating message or, alternatively, it shall switch to sending the "Hold State" message;
- 4) the slave shall initiate action when, and only when, three identical, consecutive, and properly addressed HDSL eoc frames, that contain a message recognized by the slave, have been received over the one pair;
- 5) the slave shall respond to all properly addressed received messages. The response shall be an echo of the received HDSL eoc frame towards the LTU;
- 6) any reply or echoed HDSL eoc frame shall be sent in the next available returning HDSL eoc frame;
- 7) the loopback (in the NTU/REG) and request/notify corrupted CRC commands shall be latching, permitting multiple HDSL eoc-initiated actions to be in effect simultaneously;
- 8) to unlatch all latched conditions, the message "Return to Normal" shall be transmitted by the LTU. When the slave correctly receives the "Return to Normal" message from the LTU (three times identically and consecutively), it shall unlatch all currently latched conditions initiated by prior HDSL eoc messages;
- 9) the slave shall not send autonomous messages.

5.5.2.2 Unable To Comply (UTC) mode of operation

When the slave does not support a properly addressed message that it has received three times identically and consecutively over the active pair, the slave responds with the UTC HDSL eoc response message instead of a third identical and consecutive echo. The slave shall then switch over to the message/UTC-response protocol state.

The slave also enters the message/UTC-response control state, if a message has been received that is not applicable in the current status of the command/response mode of operation, e.g. if a "Next Byte" message is detected without having received a "Read Data Register" opcode.

An error in transmission could corrupt the UTC response. This would make the LTU conclude that it was a proper message and was acknowledged. To reduce the probability of this happening, the UTC code is selected to have a Hamming distance of at least two from all other codes except the idle code.

Thus, the following requirements apply:

- 1) if the NTU/REG does not support the message in a properly addressed HDSL eoc frame, it shall return the UTC message with its own address rather than echo on the third and all subsequent consecutive reception of that same correctly addressed HDSL eoc frame;
- 2) the sending by the NTU/REG and the subsequent receipt by the LTU of three identical, consecutive, properly addressed UTC messages shall constitute notification to the LTU that the NTU/REG does not support the requested function, at which time the LTU may abandon its attempt;
 - the LTU may, of course, abandon the attempt at any time before the UTC is received (for example, if the "Return to Normal" or "Hold State" message is sent by the LTU);
- 3) the NTU/REG exits the UTC mode of operation only after receiving three consecutive "Return to Normal" messages from the LTU.

5.5.3 The HDSL eoc data read/write mode

For data transmission, bit three and bit four are used in combination. Bit three will be set to data (ZERO) only when data (rather than an opcode) are transmitted. Bit four makes multi-byte data transmission more efficient. It will denote whether the data byte being transmitted is an "Odd Byte" or "Even Byte". As described in the next subclause, with this procedure there is a message/echo response state to access the register, and following that one byte of data can be transferred for each message/data response state. The LTU can either write data into the NTU/REG memory, or read data from the NTU/REG.

5.5.3.1 Data read protocol

If the LTU is reading data from the NTU/REG it will send an appropriate read opcode message to the NTU/REG that specifies the register to be read. After receiving three identical and consecutive acknowledgements, the LTU will request for the first byte to be sent from the NTU/REG by sending "Next Byte" messages with bit four set to ONE indicating a request for an "Odd Byte". The NTU/REG will respond to these "Next Byte" messages by echoing them until it has received three such messages consecutively and identically. Beginning with the third such reception, the NTU/REG will respond by sending the first byte of the register in an HDSL eoc data frame with bit four set to ONE to indicate "Odd Byte". (A data frame that contains data in the information fields is distinguished from a frame containing an opcode by setting bit three to ZERO.) The LTU continues to send the "Next Byte" message byte with bit four set to "Odd Byte", and the NTU/REG continues to respond with a data frame containing the first byte of data and bit four equal to "Odd Byte", until the LTU has received three consecutive and identical data frames with bit four set to "Odd Byte".

If there is more data to be read, the LTU requests the second byte of data by sending "Next Byte" messages with bit four set to ZERO ("Even Byte"). The NTU/REG echoes all messages received until three such "Next Byte" messages have been received, and on the third consecutive and identical "Next Byte" message, the NTU/REG starts sending data frames containing the second byte of the register with bit four set to ZERO. The LTU continues to send the "Next Byte" message with bit four set to "Even Byte", and the NTU/REG continues to respond with a data frame containing the second byte with bit four set to "Even Byte", until the LTU has received three consecutive and identical data frames with bit four set to "Even Byte". Once the NTU/REG is in the Data Read mode, to continue reading data, the only message that the LTU is allowed to send is the "Next Byte" message with bit four toggling.

If the LTU wants to end the data read mode (either normally or abnormally), it shall send the "Hold State" or "Return to Normal" message depending upon if the LTU wants to retain any latched state or not. If the NTU/REG receives any other message, three times consecutively and identically, it shall go into the UTC mode.

The process continues for the third and all subsequent bytes with the value of bit four toggling from "Odd Byte" to "Even Byte" or vice versa, on each succeeding byte. Each time bit four is toggled, the NTU/REG echoes for two correct frames, and starts sending the data frame on the third reception. The process ends only when all data in the register have been read. If the LTU continues to send the "Next Byte" message, with the fourth bit toggled, then the NTU/REG will send an "End of Data" message. It is assumed that the LTU knows how many bytes of data to expect, but this is a safety measure to end the process. Thus, each time a data byte is received satisfactorily by the LTU, the LTU will send a "Next Byte" code with bit four set appropriately until it is satisfied that it has received all the bytes, or, until it has received three identical and consecutive "End of Data" messages with bit three set to ONE indicating opcode. Thus, it is possible to accommodate data of many bytes.

The data read mode ends, and the NTU/REG releases the register, when the LTU switches over to a known state with the "Hold State" message or "Return to Normal" message depending on whether it wants the latched conditions held or not.

5.5.3.2 HDSL eoc data read mode requirements

The protocol state sequence for the data read mode is as follows:

- 1) message/echo-response protocol state:
 - a) the HDSL eoc shall enter the data read mode of operation when the LTU sends a "Read Data" message for a specific register;
 - b) the response to this message shall be the echo response.
- 2) message/data-response protocol state:
 - a) upon receiving three identical and consecutive echo responses that match the register-specific "Read Data" message, the LTU shall send the "Next Byte" message. At this time, bit three shall be set to ONE to indicate an opcode message, and bit four shall be set to ONE to indicate "Odd Byte";
 - b) on receiving the "Next Byte" message, the NTU/REG shall echo the message until it receives it three times consecutively and identically. On the third identical and consecutive reception, the NTU/REG response shall change from the echo response to an HDSL eoc data frame containing the data byte requested. For this frame, bit three shall be set to ZERO to indicate that the information field contains data, and bit four shall be set to ONE;
 - c) if the data requested by the LTU is retrieved from a one byte register, when the LTU has received three identical and consecutive HDSL eoc data frames containing the data byte, the "Return to Normal" message or "Hold State" message shall end the data read mode;
 - d) if the data requested by the LTU is contained in a register two or more bytes long, the LTU shall initiate additional HDSL eoc protocol states. It shall continue sending the "Next Byte" message with bit three set to ONE, but bit four will be toggled between ZERO and ONE as each byte of data is successfully received (three identical, consecutive echoes). Each time there is a change in bit four the NTU/REG shall start echoing the message, while remaining in the data read mode. On the third identical and consecutive reception, the NTU/REG shall switch to sending a data frame with the next byte of data in the information field.
- 3) message/echo-response protocol state:
 - when the LTU has completed its requirements for reading data, it shall start sending the "Hold State" message or "Return to Normal" message to end the data read mode.

5.5.3.3 Data write protocol

If the LTU wants to write data into the NTU/REG's memory, it will send a "Write Data" message to the NTU/REG that identifies the required register to be written to. When the NTU/REG acknowledges with an echo message, three times identically and consecutively, the LTU will send the first byte of data. The NTU/REG will acknowledge the receipt of the byte with an echo of the message. After the LTU is satisfied with three identical and consecutive correct echo responses, it will start sending the next byte of data. Each time the LTU receives three identical and consecutive correct data echo responses, it will switch to sending the next byte of data. It will also toggle the odd/even bit accordingly. There is no need for sending "Next Byte" messages in the write mode. The LTU will end the write mode with the "End of Data" message indicating to the NTU/REG to release the register and to end the data write mode.

The contents of the addressed register in the NTU/REG are overwritten only, if the number of transmitted bytes equals the size of the addressed register and if the data write mode has been properly finished by sending the "End of Data" message by the LTU.

In any other case, i.e. if the number of transmitted bytes is higher or lower than defined or if the data write mode is not properly finished, the NTU/REG enters the UTC mode and the content of the corresponding register remains unchanged.

If the LTU abnormally wants to end the data write mode, it shall send the "Hold State" or "Return to Normal" message, depending upon if the LTU wants to retain any latched state or not. If the NTU/REG receives any other message, three times consecutively and identically, it shall enter the UTC mode.

5.5.3.4 HDSL eoc data write mode requirements

The protocol state for the data write mode is always message/echo-response. The message field can contain a command or data.

- 1) message (command)/echo (command)-response protocol state:
 - a) the HDSL eoc shall enter the data write mode of operation when the LTU sends a "Write Data" message for a specific register;
 - b) the response by the NTU/REG to this message shall be the echo response;
 - c) this protocol state shall be repeated until the LTU receives three identical and consecutive HDSL eoc frames containing the correct echo response.
- 2) message (Data)/echo (Data)-response protocol state:
 - a) upon receiving three identical consecutive echo responses that match the register-specific "Write Data" message, the LTU shall send a data frame with the first byte of data and with bit three set to ZERO (indicating that the information field contains data) and bit four set to ONE (indicating "Odd Byte");
 - b) the NTU/REG shall respond to this transmission with the echo response;
 - c) the data byte shall be written by the NTU/REG unit upon receiving the data byte three times identically and consecutively;
 - d) this protocol state shall be repeated until the LTU receives three identical and consecutive HDSL eoc frames containing the correct echo response;
 - e) if the LTU is writing to a one byte register, the data write mode shall be completed upon the LTU receiving three identical and consecutive echoes of the data byte it had transmitted;
 - f) if the LTU is writing to a multi-byte register, the LTU shall continue sending additional bytes of data, while toggling bit four for each byte of data sent successfully;
 - g) when the LTU has no more bytes of data to write, the LTU shall send a "End of Data" message to release the NTU/REG from the data write protocol state.

5.5.4 HDSL eoc message list

The HDSL eoc protocol uses various messages listed in table 9 for activating various functions at the NTU/REG. The "Read Data" and "Write Data" commands can support up to 16 registers each. The commands and the corresponding encoding used in the present document, are shown in tables 10 and 11. The register that a "Read Data" or "Write Data" message operates on is specified as a subfield of the "Read Data" or "Write Data" opcode. Additional message opcodes have been reserved for future standardization.

Some actions initiated in the NTU/REG by HDSL eoc messages, such as loopbacks, and intentional corrupted CRC are latching. Latching means that a different message is required to cancel the function. This permits the HDSL eoc to exercise multiple functions simultaneously, in spite of the "one message outstanding" rule. All latched functions may be unlatched with the "Return to Normal" HDSL eoc message. The "Return to Normal" message returns the NTU/REG to a known state. Repetition of this message continues to hold the NTU/REG in this known state. Hence, the "Return to Normal" message is also defined as the "idle code" for the NTU/REG. On the other hand, if all the latched functions were to be maintained in their latched state, the "Hold State" command is sent.

- 1) The LTU shall continuously send the activating message after the receipt of the three valid echoes or, alternatively, it shall switch to sending the "Hold State" message if it wants to maintain latched conditions.
- 2) The "Loopback" and "Request/Notify corrupted CRC" commands shall be latching, permitting multiple HDSL eoc-initiated actions to be in effect simultaneously.
- 3) To release all latched conditions, a separate message "Return to Normal" shall be transmitted by the LTU. When the NTU/REG correctly receives the "Return to Normal" message from the LTU (three times identically and consecutively), it shall unlatch all currently latched conditions initiated by prior HDSL eoc messages.

5.5.5 HDSL eoc message set requirements

The HDSL eoc message set is shown in table 9. The actions taken by the NTU/REG and LTU in response to correctly received HDSL eoc messages shall be as follows:

- 1) Unable to Comply (UTC):
 - the NTU/REG shall send this message when it receives an HDSL eoc message (three times consecutively and identically) that the NTU/REG cannot perform, either because it does not recognize or has not implemented the command, or because the command is unexpected given the current state of the HDSL eoc operations (e.g. the command indicates that the information field contains data, but the command was not preceded by a "Write Data" command).
- 2) Return to Normal:
 - this message shall release all outstanding latched conditions at the NTU/REG initiated by prior HDSL eoc messages. The function of the "Return to Normal" message may be used as an eoc reset function for the NTU/REG. Therefore, the proper evaluation of this message in a single NTU/REG subsystem results in a reset of all pending functions in this subsystem. This code sent with the NTU-address "00" shall also be sent during idle states.
- 3) Loopback of Application Frame at NTU:
 - this message shall direct the NTU to loopback the application bit stream toward the LTU until cancelled by a "Return to Normal" message.
- 4) Hold State:
 - this message shall be sent by the LTU to maintain the NTU/REG HDSL eoc processor and any active HDSL eoc controlled operations in their present state.
- 5) Analogue Loopback 1A in REG:
 - this function directs the REG to loopback the user-data bitstream toward the LTU. This is a transparent loopback. Since this is a function of each individual subsystem REG, the LTU shall take care, that these messages are acknowledged by each individual subsystem.
- 6) Request Corrupted CRC (note 1):

- sometimes the appearance of error free transmission may result because the CRC circuit is not functioning properly. Hence, when the performance monitoring circuit is suspected of malfunction, corrupted CRCs can be sent to test the CRC logic as well as the circuits that collect, process and store performance data.

6a) Request Corrupted CRC NTU (note 2):

- No REG Present:
 - corrupted CRCs are requested to be sent from the NTU to test the CRC checking circuit at the LTU until cancelled with the "Request End of Corrupted CRC NTU" message.
- REG Present:
 - corrupted CRCs are requested to be sent from the NTU to test the CRC checking circuit at the REG-C until cancelled with the "Request End of Corrupted CRC NTU" message. This results in the transmission of an active rcbe-bit by the REG towards the LTU and NTU as soon as corrupted CRCs are detected.

6b) Request Corrupted CRC REG-R (note 2):

- corrupted CRCs are requested to be sent from the REG towards the LTU to test the CRC checking circuit at the LTU until cancelled with the "Request End of Corrupted CRC REG-R" message.

6c) Request Corrupted CRC REG-C:

- corrupted CRCs are requested to be sent from the REG towards the NTU to test the CRC checking circuit at the NTU until cancelled with the "Request End of Corrupted CRC REG-C" message. This results in the transmission of an active febe-bit by the NTU towards the LTU as soon as corrupted CRCs are detected.

7a) Request End of Corrupted CRC NTU (note 2):

This message shall request the NTU to stop sending corrupted CRCs towards the REG or LTU as applicable.

7b) Request End of Corrupted CRC REG-R (note 2):

This message shall request the REG to stop sending corrupted CRCs towards the LTU.

7c) Request End of Corrupted CRC REG-C:

This message shall request the REG to stop sending corrupted CRCs towards the NTU.

8a) Notify Corrupted CRC NTU (note 2):

- No REG Present:
 - This message shall notify the NTU that intentionally corrupted CRCs will be sent towards the NTU by the LTU. This message shall be used in the NTU to disable any alarm indication circuitry activated by the detection of corrupted CRCs. The febe-bit towards the LTU shall be still active however.
- REG Present:
 - this message shall notify the NTU that intentionally corrupted CRCs will be sent towards the NTU by the REG. This message shall be used in the NTU to disable any alarm indication circuitry activated by the detection of corrupted CRCs. The febe-bit towards the LTU shall be still active however.

8b) Notify Corrupted CRC REG-R (note 2):

- this message shall notify the REG that intentionally corrupted CRCs will be sent towards the REG by the LTU. This message shall be used in the REG to disable the transmission of an active rrbe-bit towards the NTU, as soon as corrupted CRCs are detected from the LTU. The rrbe-bit towards the LTU shall be still active however.

8c) Notify Corrupted CRC REG-C:

- this message shall notify the REG that intentionally corrupted CRCs will be sent towards the REG by the NTU. This message shall be used in the REG to disable the transmission of an active rcbe-bit towards the NTU, as soon as corrupted CRCs are detected from the NTU. The rcbe-bit towards the LTU shall be still active however.

9a) Notify End of Corrupted CRC NTU (note 2):

- this message shall notify the NTU that the LTU or REG has stopped sending intentionally corrupted CRCs and that the NTU may enable again any alarm circuitry detecting corrupted CRCs.

9b) Notify End of Corrupted CRC REG-R (note 2):

- this message shall notify the REG that the LTU has stopped sending intentionally corrupted CRCs and that the REG may enable again the transmission of a valid rcbe-bit towards the NTU when detecting corrupted CRCs from the LTU.

9c) Notify End of Corrupted CRC REG-C:

- this message shall notify the REG that the NTU has stopped sending intentionally corrupted CRCs and that the REG may enable again the transmission of a valid rcbe-bit towards the NTU when detecting corrupted CRCs from the NTU.

10) End of Data:

- this message shall be sent by the LTU after it has written all bytes of data to the NTU/REG and by the NTU/REG when the LTU requests more bytes than are available in the NTU/REG register during a data read procedure.

11) Next Byte:

- this message shall be sent by the LTU in the data read mode after the NTU/REG has acknowledged the previously sent "Read Data" command. This message shall be continually sent by the LTU when it is in the Data Read mode until all data have been read. This message, coupled with the toggling of bit four, allows multi-byte data to be read.

12) Write Data (Register #):

- this message shall be sent by the LTU to set the NTU/REG in a mode to receive data in the register specified. The number of the register at the NTU/REG that shall receive data is encoded in the command itself. After receiving this message correctly, the NTU/REG shall enter the data write mode, ready to receive the data contained in the data messages to follow, and store the data in the register number encoded in the command.

13) Read Data (Register #):

- this message shall be sent by the LTU to set the NTU/REG in a mode to read the data in the register specified. The number of the register at the NTU/REG from which the data are to be read is encoded in the command itself. After receiving this message correctly, the NTU/REG shall enter in the data read mode and transmit data from the register encoded in the command, one byte at a time, in response to successive "Next Byte" messages (with changes in bit four) from the LTU.

NOTE 1: No specific algorithm for the corruption is to be defined.

NOTE 2: For the messages signed by indices a and b the same opcode is used. The equipment concerned is indicated by the address contained in the message.

Table 9: eoc opcode messages

Hex-code	Opcode description
06	Unable to Comply (UTC)
07	Return to Normal
08	Loopback of application frame at NTU (see note 1)
10	Hold State
19	Analogue Loopback in REG (see notes 1 and 2)
20	Request Corrupted CRC NTU/REG-R (see notes 1 and 3)
22	Request Corrupted CRC REG-C (see note 1)
28	Request End of Corrupted CRC NTU/REG-R (see note 3)
29	Request End of Corrupted CRC REG-C
3F	Notify Corrupted CRC NTU/REG-R (see notes 1 and 3)
50	Notify Corrupted CRC REG-C (see note 1)
5F	Notify End of Corrupted CRC NTU/REG-R (see note 3)
60	Notify End of Corrupted CRC REG-C
9F	End of Data
AF	Next Byte
D0-DF	Write Data Register (numbers 0 to F) NTU/REG (see note 3)
E0-EF	Read Data Register (numbers 0 to F) NTU/REG (see note 3)
F0-F3	Vendor defined
NOTE 1: Latching; this means that a release message is required to cancel the function.	
NOTE 2: Due to the used transmission system, separate loopbacks for each pair have to be set-up in the regenerator. The O&M unit in the LTU has to assure that the individual loopback is closed, before acknowledging the proper operation to the application interface.	
NOTE 3: This opcode is used for messages concerning the NTU or the REG. A distinction between both is possible by the address contained in the message.	
NOTE 4: No need has been identified for the messages 18, 30, 38, 6F, 7F in Europe. They may be used by network operators outside Europe, e. g. in North America as defined in the ANSI Committee T1 Technical Report [25]. All other messages are reserved for future applications.	

5.5.6 Data registers in the NTU and in regenerators

The NTU and the regenerator each contain 16 registers. These registers can be used for read only or for read and write operations. The registers used inside Europe are defined in tables 10 and 11. The registers 1 to 9 may be used by network operators outside Europe, e. g. in North America as defined in the ANSI Committee T1 Technical Report [25]. The register F is not used at present. Only the registers E in the NTU and C, D and E in the REG are individual for each transceiver of a two or three pair system. All other registers contain equipment relevant data and are available over all pairs in parallel. Individual registers (register D) at the REG are required for equipment identification when separate regenerators are used in each pair.

Table 10: eoc data registers for the NTU

Reg# (HEX)	Use	Length	Name	Description
A	R	(see note)	NTU status	NTU status information bits
B	R/W	(see note)	NTU configuration	NTU configuration bits
D	R	(see note)	equipment identification	
E	R	1 byte	noise margin	
NOTE: The number of bytes and the contents of the register, as well as the encoding of the different bits, is left to the individual network operator.				

Table 11: eoc data registers for regenerators

Reg# (HEX)	Use	Length	Name	Description
A	R	(see note)	REG-status	REG status information bits
C	R	1 byte	noise margin REG-C	
D	R	(see note)	equipment identification	
E	R	1 byte	noise margin REG-R	
NOTE:	The number of bytes and the contents of the register, as well as the encoding of the different bits, is left to the individual network operators.			

5.5.7 Noise margin

5.5.7.1 General

For the evaluation of the noise margin a Gaussian noise is assumed. The noise value is calculated based on a sample taken each second for each pair separately. The evaluating range is between +27 dB and -5 dB, where 0 dB indicates the noise margin for which a BER of 10^{-7} for each pair is expected. The accuracy of the values shall be 1 dB in the range between +5 dB and -5 dB.

5.5.7.2 Coding of the noise margin values

The coding shall use a logarithmic law and have an increment of 0,5 dB. It uses one byte from which the first bit (msb) and the second bit are identical and indicate the sign. The remaining six bits are used for the value of the noise margin, as shown in table 12.

Table 12: Coding of noise margin values

Noise margin	msb								lsb	Remark
	1	2	3	4	5	6	7	8		
+31,5 dB	0	0	1	1	1	1	1	1	1	not relevant
+27,5 dB	0	0	1	1	0	1	1	1	1	
+27,0 dB	0	0	1	1	0	1	1	0	0	expected BER < 10^{-7}
+0,5 dB	0	0	0	0	0	0	0	0	1	
0 dB	0	0	0	0	0	0	0	0	0	expected BER 10^{-7}
-0,5 dB	1	1	1	1	1	1	1	1	1	expected BER > 10^{-7}
-5,0 dB	1	1	1	1	0	1	1	0	0	
-5,5 dB	1	1	1	1	0	1	0	1	1	not relevant
-31,5 dB	1	1	0	0	0	0	0	0	1	

5.6 Start-up procedure

5.6.1 General

5.6.1.1 Start-up

The start-up procedure is designed as a local procedure for each pair, it is a process characterized by a sequence of signals produced by the NTU, the LTU and the REG. Start-up results in an establishment of two-way transmission (if possible) between the application interfaces, i.e. synchronization of the receivers, training of the echo cancellers and training of the equalizers to the point that the requirements for reliable communications are met. Also, tip-ring polarity reversal and pair interchanges are automatically detected and compensated at the NTU. It is the task of the operation and maintenance block to detect when the start up procedure for all pairs is completed and to initiate a transparent transmission of user data.

5.6.1.2 Activation of HDSL transceiver pairs

Activation is the process for the establishment of duplex communication over a single pair. This process is established between the HDSL transceivers at the LTU and the NTU, or between the LTU and the REG-R and the REG-C and the NTU respectively.

5.6.1.3 Transparency

Prior to the completion of activation the transmission is not transparent, the signals that are present at the line interfaces of the HDSL transceivers are special start-up patterns generated by the HDSL transceivers. Each HDSL transceiver shall provide transparent transmission of data to the core function after completion of the individual activation procedure. The output signal of receivers that have not yet entered the Active-Rx State as defined in subclauses 5.6.5 and 5.6.6 shall be set to all ONES.

The operational status is determined by the application.

NOTE: Transceivers in a REG are at no time fully transparent in so far as some HOH-bits will be overwritten.

5.6.1.4 Noise margin

The noise margin is estimated at the receivers of LTU, NTU and REG (if provided). This value is used to estimate the bit error ratio (BER) of the received data.

For applications according to the present document the noise margin is compared to a value of -5 dB during the start-up procedure.

NOTE: This value does not allow data transmission, it is chosen to be in compliance with existing equipment using the noise margin as a criteria for start-up.

5.6.2 Control and status signals

The following virtual control and status signals are involved in the activation procedure. They are related to the operation of the individual HDSL transceiver.

5.6.2.1 Control signals

5.6.2.1.1 QUIET

QUIET = ONE will cause a transition of the HDSL transceiver from any state (except the Inactive State) to the Deactivated State, where no energy -except remote powering- is transmitted to the line. The QUIET = ONE command will not cause any change if the HDSL transceiver is in the Inactive State.

5.6.2.1.2 ACTREQ

Activation Request (ACTREQ) defaults to ONE at power up. The HDSL transceiver at the LTU will begin the activation process only if ACTREQ is equal to ONE.

5.6.2.2 Status signals

All of the following status signals are defined per pair.

5.6.2.2.1 LOSW

The absence of the *Loss of Sync Word* signal (LOSW = ZERO) indicates that HDSL frame synchronization is completed. When LOSW = ONE the receiver has not yet acquired frame synchronization, or it has lost it (refer to figures 13 to 15).

5.6.2.2.2 LOSWT

LOSWT = ONE indicates that the frame synchronization has been lost for more than 2 seconds.

5.6.2.2.3 LOS

The *Loss of Signal* signal (LOS = ONE) in the NTU indicates that no signal is detected on the line from the LTU. LOS = ZERO indicates that a signal from the LTU has been detected.

5.6.2.2.4 LOST

The LOST = ONE in the LTU indicates that no signal is detected on the line from the NTU for more than 1 second.

5.6.2.2.5 INDC

When an HDSL transceiver at the LTU is ready to receive data the indicator INDC is set (INDC = ONE). The condition for INDC = ONE is:

$$((\text{LOSW} = \text{ZERO}) \ \& \ (\text{noise margin} > -5 \text{ dB})) \ \text{or} \ ((\text{LOSW} = \text{ZERO}) \ \& \ (\text{T-Act expired}))$$

Because of the low noise margin defined for applications referring to the present document the noise margin condition is met in any case, which results in the simple condition:

$$\text{INDC} = \text{ONE} \ \text{is effectively identical to} \ \text{LOSW} = \text{ZERO}.$$

The reason for keeping the above mentioned multiple condition is to achieve compatibility with existing circuits.

5.6.2.2.6 INDR

When an HDSL transceiver at the NTU is ready to receive data the indicator INDR is set (INDR = ONE). The condition for INDR = ONE is:

$$((\text{LOSW} = \text{ZERO}) \ \& \ (\text{noise margin} > -5 \text{ dB})) \ \text{or} \ ((\text{LOSW} = \text{ZERO}) \ \& \ (\text{T-Act expired}))$$

Because of the low noise margin defined for applications referring to the present document the noise margin condition is met in any case, which results in the simple condition:

$$\text{INDR} = \text{ONE} \ \text{is effectively identical to} \ \text{LOSW} = \text{ZERO}.$$

The reason for keeping the above mentioned multiple condition is to achieve compatibility with existing circuits.

NOTE: The internal status indicators INDC and INDR are different from the *indc*- and *indr*-bit in the overhead channel as defined in tables 3, 4 and 5.

5.6.3 Transmitted signals

The following is the description of the transmitted signals during activation:

5.6.3.1 Silent

No signal is transmitted to the line.

5.6.3.2 S0 signal

The S0 signal is a two level signal including the sync word and stuff symbols. The polarity of the stuff quats is arbitrary. The sequence of the stuffing steps is also arbitrary. However, not more than four consecutive frames with the same (plus or minus) stuffing shall be used. The remainder of the two level signal are derived from scrambling an all ONEs sequence and only the sign bit is used to select the level of the signal. The scrambler is operating at the line bit rate and is disabled during the transmission of the HDSL frame sync word and the stuffing bits. The transmitted levels of all symbols (including the stuff quats) in the S0 signal are +3 and -3.

5.6.3.3 S1 signal

The S1 signal shall be a framed four level scrambled signal. The frame shall consist of the HDSL frame sync word, the stuffing bits, the HOH and the payload blocks. The payload blocks shall contain an all ONEs signal replacing the Z-bit and the payload. The scrambler is operating at the full bit rate and is disabled during the transmission of the sync word

and the stuffing bits. The transmitted levels are +3, +1, -1 and -3. All HOH-bits transmitted by the LTU and the NTU shall be valid. The REGs shall insert only those HOH-bits originated by themselves, all other HOH-bits shall be set to ONE, until the REG-R enters the Active-R State or REG-C the Active-C State, as defined in subclause 5.6.6, but as long as the REGs are in Active-R and Active-C State respectively, they shall be transparent for these HOH-bits.

5.6.3.4 2B1Q data

The 2B1Q data signal shall be a framed and scrambled four level signal. The frame shall consist of the HDSL frame sync word, the stuffing bits, the valid HOH bits and payload blocks. The payload blocks shall contain valid Z-bits and the payload, which is however application and implementation dependant until the start-up procedure is completed for all used transceiver pairs and the pair identification procedure is completed. The scrambler is operating at the full bit rate and is disabled during the transmission of the sync word and the stuffing bits. The transmitted levels are +3, +1, -1 and -3.

5.6.4 Timers

The following timers are involved in the activation procedure of the HDSL transceivers. The timeline of the activation sequence is given in figure 11 and the timer values are given in table 13. The precise role of the timers in the start-up procedure is described in subclause 5.6.5.

5.6.4.1 T1

T1 is the duration which the HDSL transceiver at the LTU continues to transmit a S0 signal after it has detected a S0 signal from the NTU.

5.6.4.2 T2

T2 is the duration between the time that the HDSL transceiver at the NTU detects signal from the HDSL transceiver at the LTU and the time that it starts to transmit the S0 signal.

5.6.4.3 T3

T3 is the duration between the time that the HDSL transceiver at the NTU detects the S1 signal from the HDSL transceiver at the LTU and the time that it starts to transmit the S1 signal.

5.6.4.4 T4

T4 is the duration between the HDSL transceiver at the NTU starts to transmit the S0 signal and guaranteed stable timing.

5.6.4.5 T-Act

The activation time for the HDSL transceivers (T-Act) is the time in which the activation procedure in the HDSL transceivers at the LTU, the REG or the NTU should have successfully been completed, starting from the point in time where the HDSL transceiver at the LTU, the REG or the NTU starts to transmit the S0 signal.

5.6.4.6 Timer values

The timer values are listed in table 13.

Table 13: Timer values

Lower bound		Timer		Upper bound
5 s	≤	T1	≤	10 s
1,9 s	≤	T2	≤	2,1 s
		T3	≤	4 s
		T4	≤	4 s
27	≤	T-Act	≤	31 s

5.6.5 Activation state diagrams

The following describes the activation timeline, (see figure 11), and the state diagrams for the HDSL transceivers at the LTU and at the NTU, (see figures 13 and 14 respectively). The flow diagram of figure 11 describes the complete start-up sequence of the link between LTU and NTU without a regenerator.

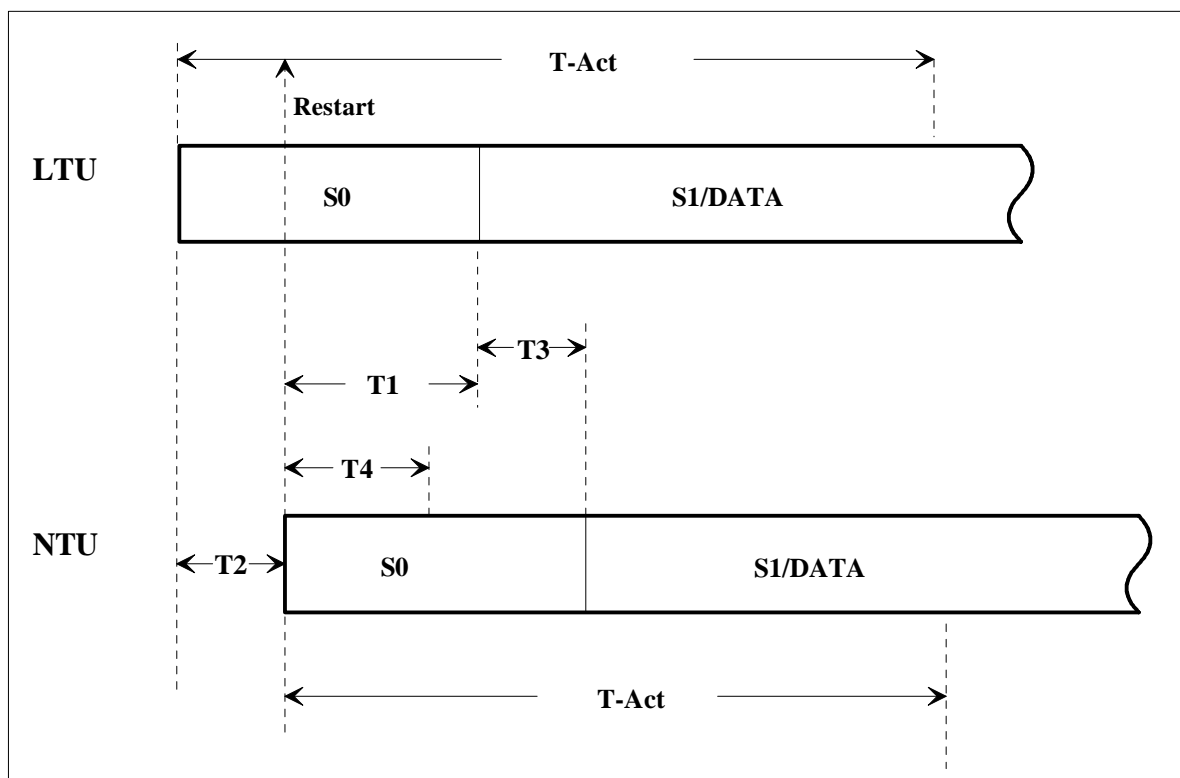


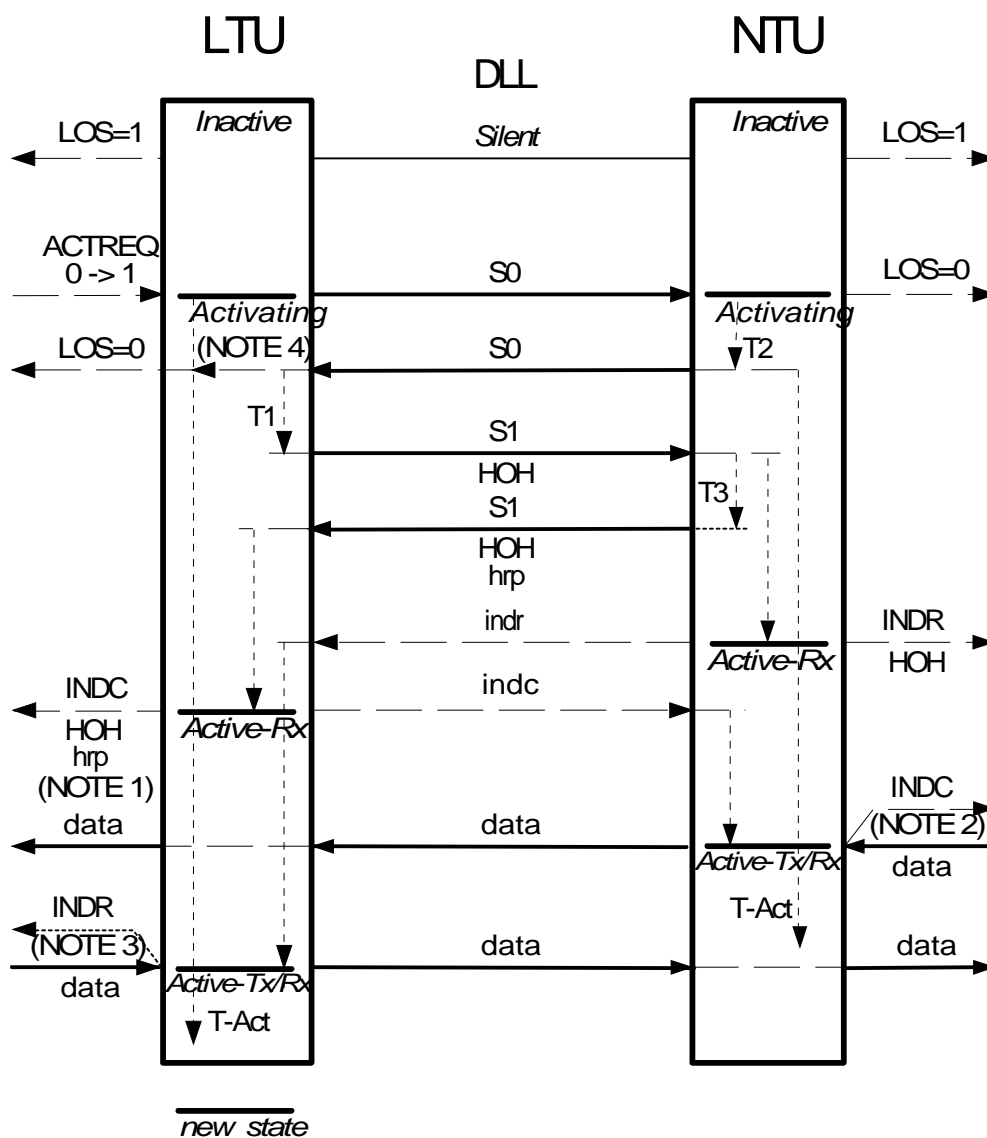
Figure 11: Activation timeline

5.6.5.1 HDSL transceiver states at the NTU

Figure 13 shows a state diagram for the activation of the NTU. When powered on, the NTU is initially in the Inactive State, where its transmitter is silent. When signal power is detected from the LTU, the NTU proceeds to the Activating State and executes the timeline shown in figure 11.

It waits $T2 = 2$ s while transmitting no signal and then starts the timer T-Act and the transmission of S0 and monitors the received signal for S1. Within T4 s from beginning of transmission the timing within the NTU should have reached a stable timing phase. When the NTU detects a valid framed four level data signal it sets LOSW = ZERO, stops timer T-Act and starts timer T3. Before expiry of T3 it has to begin transmitting S1 signal. If the timer T-Act expires before synchronization has been achieved the unit will cease transmission and move to the Deactivated State.

When the receiver in the NTU is ready to accept 2B1Q data, it sets the indicator INDR = ONE and moves to the Active-Rx State. The condition for INDR = ONE is, as described in subclause 5.6.2.2.6, that synchronization is reached (LOSW = ZERO), because the noise margin condition is for applications according to the present document met in any case, due to the low value of -5 dB defined for the noise threshold.



NOTE 1: After having detected the status indicator INDC, the LTU starts to evaluate the indr- and hrp-bit. If an hrp-bit set to ONE is received no regenerator is present.

NOTE 2: If the indc = 0 has been received six times consecutively, the NTU becomes transparent for payload blocks.

NOTE 3: If the indr = 0 has been received six times consecutively, the LTU becomes transparent for payload blocks.

NOTE 4: Timer T-Act is restarted after reception of S0 from the NTU.

NOTE 5: Timer T4 is an NTU internal timer and therefore it is not shown in this figure.

Figure 12: Flow diagram for start-up

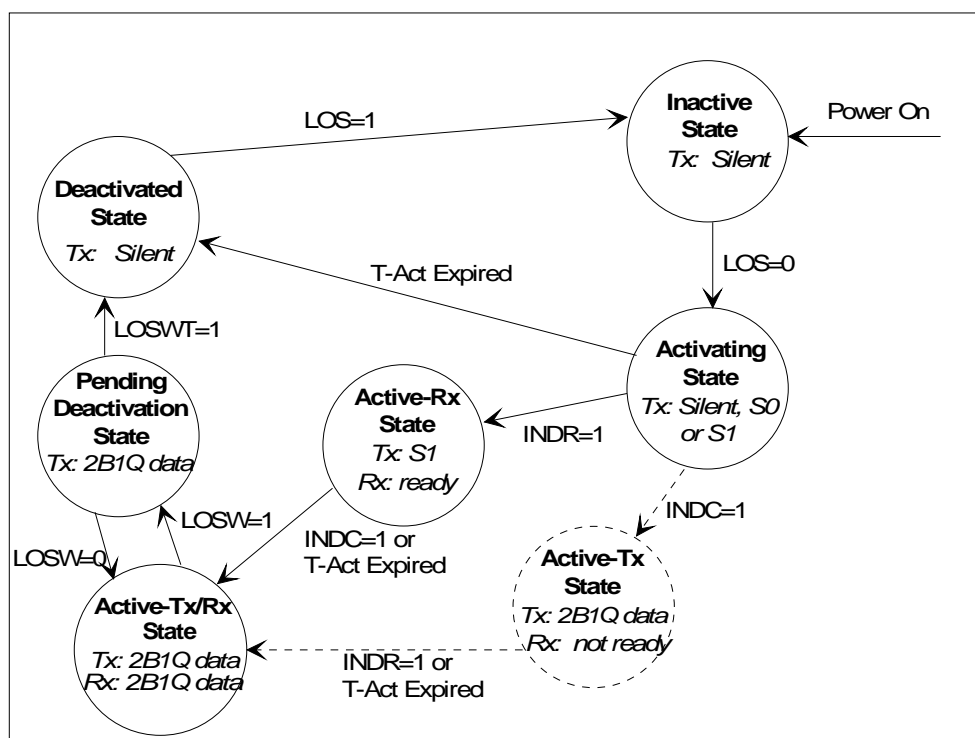


Figure 13: NTU activation state diagram

When the overhead channel in the transmitted S1 signal becomes available in the preceding start-up procedure, the status INDR = ONE is conveyed to the LTU by setting the indicator bit $indr = 0$. In the LTU an identical process takes place and $indc = 0$ is received by the NTU in the overhead channel if the LTU has reached its Active-Rx State and is ready to receive 2B1Q data. After the reception of six consecutive indicator bits $indc = 0$ the status indicator INDC is set to ONE and the NTU moves to the Active-Tx/Rx state, where it is fully active, both transmitting and receiving 2B1Q data.

If it does not detect INDC = ONE before timer T-Act expires, then it will move to the Active-Tx/Rx State anyway where either synchronization is still being maintained or it is not. If the NTU has lost synchronization and $LOSW = ONE$, the system will proceed to the Pending Deactivation State. On the other hand, if synchronization is present at both ends and the LTU has not failed the timeline and not reached its Deactivated State, the timer at the LTU will promptly force that unit into its Active-Tx/Rx State and set INDC = ONE. When INDC = ONE is detected at the NTU, the system will be operational in the Active-Tx/Rx State. If the LTU does not have synchronization, it will move to its Pending Deactivation State and ultimately to the Deactivated State, where it will go to Silent. At this point the NTU will lose synchronization and move to its own Pending Deactivation State.

Once in the Active-Tx/Rx State, the unit will remain there unless synchronization is lost or the unit is signalled to go to the QUIET mode or is powered off. If the unit is signalled to go to QUIET mode, it will go to the Deactivated State. If synchronization is lost ($LOSW = ONE$), the unit will move to the Pending Deactivation State. While in the Pending Deactivation State, the unit attempts to regain synchronization for nominally 2 s. If synchronization is regained in this time ($LOSW = ZERO$), the unit returns to the Active-Tx/Rx State. If not, $LOSWT$ is set to ONE and the unit enters the Deactivated State.

After entering the Deactivated State, either due to a period of synchronization word loss ($LOSW = ONE$) or due to expiration of the timer T-Act, the transmitter in the NTU goes silent and the NTU begins to look for a loss of signal power from the LTU. When a loss of signal ($LOS = ONE$) is detected, the unit moves immediately to the Inactive State. When signal power is detected from the LTU ($LOS = ZERO$), the unit will proceed once again to the Activating State, where another attempt is made at the start-up process.

For applications outside the scope of the present document, which will use a more sensitive noise margin during the start-up procedure, a more complicated procedure will be necessary, which is nevertheless compatible with the simplified method according to the present document.

Firstly the unit can set INDR = ONE even if the defined noise margin is not reached, when it is synchronized and timer T-Act has expired. The purpose of using this condition is straightforward. The units will indicate the receivers are ready for data when they are synchronized and the timers for completing start-up have expired, to allow the units to pass data as best they can, even when normally desired reliability limits are not achieved, in support of applications that can use a less reliable channel and for diagnostics. (The overhead channel contains an indication of the system margin, so that an individual application can determine whether the margin achieved is suitable for its own use or not).

Secondly a parallel way, indicated in figure 13 by dotted lines, is possible to reach the Active-Tx/Rx State. If the NTU detects INDC = ONE from the LTU before it sets INDR = ONE it will move to the Active-Tx State. In this state its receiver is not ready to receive data, but it begins to transmit 2B1Q data in direction to the LTU, which is ready to receive it. When the NTU sets INDR = ONE it moves from the Active-Tx State to the Active-Tx/Rx State. From the Active-Tx State the only way the NTU can fail to set INDR = ONE is to lose synchronization, but in this case the expiration of timer T-Act forces it to move to the Active-Tx/Rx State anyway and with LOSW = ONE the NTU will move immediately to the Pending Deactivation State.

5.6.5.2 HDSL transceiver states at the LTU

Figure 14 shows a state diagram for the activation of the LTU. When powered on, the LTU is initially in the Inactive State, where its transmitter is silent. If the activation request signal ACTREQ is set to ONE, which is normally the default when powering on, the LTU proceeds immediately to the Activating State and executes the timeline shown in figure 11.

It starts the timer T-Act and the transmission of S0 and monitors the receive line for signal power from the NTU. When it detects signal power it starts timer T1 and restarts timer T-Act. On expiry of T1 it begins to transmit S1 and to wait for the framed four level signal S1 from the NTU to gain synchronization. If synchronization is detected LOSW is set to ZERO. If timer T-Act expires before synchronization is achieved LOSW is set to ONE and the unit moves to the Deactivated State and ceases transmission. The NTU will therefore also be forced to the Deactivated State, as described above, and LOST = ONE will appear after a period of 1 s and the Inactive State will be entered. If ACTREQ is still set to ONE the start-up procedure will be reinitiated.

When the receiver in the LTU is ready to accept 2B1Q data, it sets the indicator INDC = ONE and moves to the Active-Rx State. The condition for INDC = ONE is, as described in subclause 5.6.2.2.5, that synchronization is reached (LOSW = ZERO), because the noise margin condition is for applications according to the present document met in any case, due to the low value of -5 dB defined for the noise threshold.

When the overhead channel in the transmitted S1 signal becomes available in the preceding start-up procedure, the status INDC = ONE is conveyed to the NTU by setting the indicator bit *indc* = 0. In the NTU an identical process takes place, as described above, and *indr* = 0 is received by the LTU in the overhead channel if the NTU has reached its Active-Rx State and is ready to receive 2B1Q data. After reception of six consecutive indicator bit *indr* = 0 the status indicator INDR is set to ONE and the LTU moves to the Active-Tx/Rx state, where it is fully active, both transmitting and receiving 2B1Q data.

If it does not detect INDR = ONE before timer T-Act expires, then it will move to the Active-Tx/Rx State anyway where either synchronization is still being maintained or it is not. If the LTU has lost synchronization and LOSW = ONE, the system will proceed to the Pending Deactivation State. On the other hand, if synchronization is present at both ends and the NTU has not failed the timeline and not reached its Deactivated State, the timer at the NTU will promptly force that unit into its Active-Tx/Rx State and set INDR = ONE. When INDR = ONE is detected at the LTU, the system will be operational in the Active-Tx/Rx State. If the NTU does not have synchronization, it will move to its Pending Deactivation State and ultimately to the Deactivated State, where it will go to Silent. At this point the LTU will lose synchronization and move to its own Pending Deactivation State.

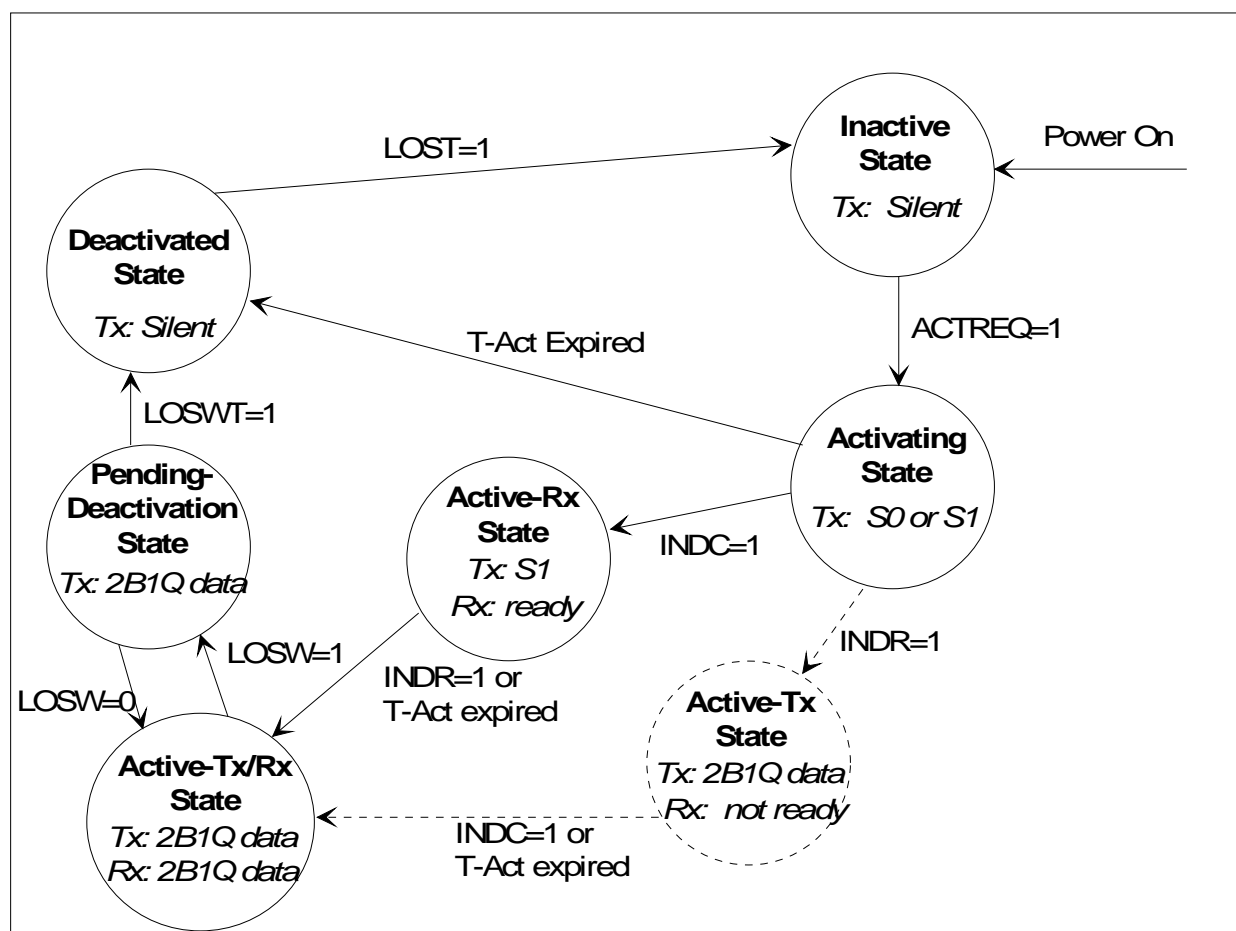


Figure 14: LTU activation state diagram

Once in the Active-Tx/Rx State, the unit will remain there unless synchronization is lost or the unit is signalled to go to the QUIET mode or is powered off. If the unit is signalled to go to QUIET mode, it will go to the Deactivated State. If synchronization is lost ($LOSW = ONE$), the unit will move to the Pending Deactivation State. While in the Pending Deactivation State, the unit attempts to regain synchronization for nominally 2 s. If synchronization is regained in this time ($LOSW = ZERO$), the unit returns to the Active-Tx/Rx State. If not, $LOSWT$ is set to ONE and the unit enters the Deactivated State.

After entering the Deactivated State, either due to a period of synchronization word loss ($LOSW = ONE$) or due to expiration of the timer T-Act, the transmitter in the LTU goes silent and the LTU begins to look for a loss of signal power from the NTU. When a loss of signal ($LOS = ONE$) is detected for 1 s, $LOST$ is set to ONE and the unit moves immediately to the Inactive State. When $ACTREQ$ is set again to ONE, the unit will proceed once again to the Activating State, where another attempt is made at the start-up process.

For applications outside the scope of the present document, which will use a more sensitive noise margin during the start-up procedure, a more complicated procedure will be necessary, which is nevertheless compatible with the simplified method according to the present document.

Firstly the unit can set $INDC = ONE$ even if the defined noise margin is not reached, when it is synchronized and timer T-Act has expired. The purpose of using this condition is straightforward. The units will indicate that the receivers are ready for data when they are synchronized and the timers for completing start-up have expired, to allow the units to pass data as best they can, even when normally desired reliability limits are not achieved, in support of applications that can use a less reliable channel and for diagnostics. (The overhead channel contains an indication of the system margin, so that an individual application can determine whether the margin achieved is suitable for its own use or not).

Secondly a parallel way, indicated in figure 14 by dotted lines, is possible to reach the Active-Tx/Rx State. If the LTU detects INDR = ONE from the NTU before it sets INDC = ONE it will move to the Active-Tx State. In this state its receiver is not ready to receive data, but it begins to transmit 2B1Q data in direction to the NTU, which is ready to receive it. When the LTU sets INDC = ONE it moves from the Active-Tx State to the Active-Tx/Rx State. From the Active-Tx State the only way the LTU can fail to set INDC = ONE is to lose synchronization, but in this case the expiration of timer T-Act forces it to move to the Active-Tx/Rx State anyway and with LOSW = ONE the LTU will move immediately to the Pending Deactivation State.

5.6.5.3 The HDSL synchronization state machine

The HDSL synchronization state machine is shown in figure 15. When the HDSL transceiver is powered on and is initially detecting S0 signal or when it loses synchronization during one of the Active-Tx/Rx States as shown in figures 13 and 14, it enters the Out of Sync State. In this state it sets LOSW = ONE and searches for the sync word in the received signal. If it detects the sync word for the first time, it moves to State 0. If the sync word is discovered again in the next frame at the correct position, the HDSL transceiver is deemed to be synchronized, the In Sync State is entered and LOSW = ZERO; if not, the HDSL transceiver moves back to the Out of Sync State.

To move from the In Sync State to the Out of Sync State the HDSL transceiver has to pass through five intermediate states, named State 1 to State 5. The transition to higher numbered state occurs if the sync word is again not discovered in a succeeding frame. So the sync word has to be lost six times in series before loss of synchronization is deemed and the Out of Sync State is entered. If however in one of the five intermediate states the sync word is discovered, then the HDSL transceiver moves back to the In Sync State immediately.

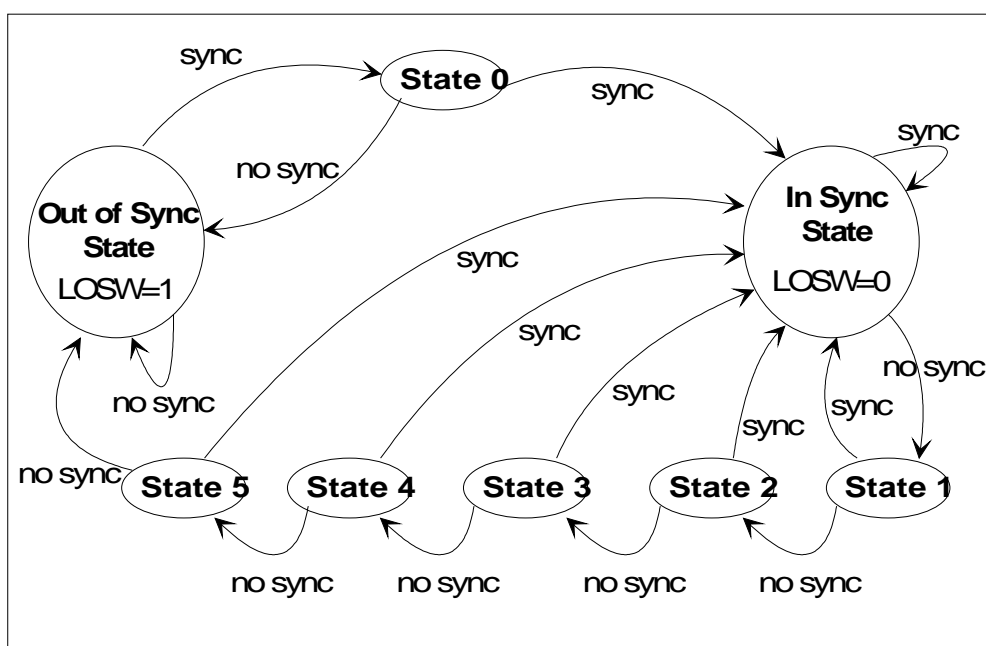


Figure 15: HDSL synchronization state machine

5.6.6 Regenerator related procedures

In order to achieve data transmission over distances that are greater than can be achieved by a single HDSL system, a regenerator (REG) is necessary.

A separate REG shall be provided for each pair. The REG consists of two parts, REG-R for interfacing with the LTU, and REG-C for interfacing with the NTU. An internal connection between the REG-R and REG-C provides the communication between the two parts during start-up and normal operation.

A connection which uses a regenerator has two separated HDSL links which roughly follow the start-up principles described above for the LTU/NTU start-up procedure. The difference is that the regenerator does not evaluate and insert the indc/indr-bits and also does not perform the path identification procedure based on the Z-bits.

The link between the LTU and the REG is the first to be activated. After the completion of the start-up procedure of this link the second link between the REG and the NTU will be activated.

The flow diagram of figure 16 and the regenerator activation state diagram of figure 17 explain the complete start-up sequences for the link between the LTU and the NTU containing a regenerator.

5.6.6.1 Activation state diagrams for the REG

The activation procedures with regenerators follow the same principles as described for the LTU and NTU only. As the *indc/indr*-bits reflect the status of the LTU- and NTU-receiver only, the evaluation and insertion of these bits in the REG, however, are not necessary. This results in a less complex state diagram for the REG-C and REG-R side in the REG as shown in figure 17. When the system is powered on, the REG-C as well as the REG-R enters its Inactive State, after completing self-tests.

5.6.6.1.1 HDSL transceiver states at the REG-R

During the Inactive-R State the HDSL transceiver at the REG-R is silent, *LOSW-R* = ONE and *LOS-R* = ONE. Upon the detection of a signal from the HDSL transceiver at the LTU (*LOS-R* = ZERO) it changes to the Activating-R State and follows the timeline shown in figure 11 for the NTU.

It waits $T_2 = 2$ s while transmitting no signal then starts the timer *T-Act* and the transmission of *S0* and monitors the received signal for *S1*. When the REG-R detects a valid framed four level data signal from the LTU it sets *LOSW-R* = ZERO, starts timer *T3* and proceeds to the Active-R State. If the synchronization fails, this means if *T-Act* expires before *LOSW-R* = ZERO, the REG-R moves to the Deactivated-R State, ceases transmission and forces REG-C into the Deactivated-C State. The further behaviour is described below.

On expiry of *T3* the REG-R begins to transmit *S1* signal.

Upon entering the Active-R State the *T-Act* timer is deactivated and an activation request signal *ACTREQ* = ONE is sent to the REG-C. In this state the receiver is fully synchronized and in the direction REG → LTU, the REG-specific overhead bits (*eoc*, *rrbe*, *rega*, *hrp*, *crc*) are active, all other overhead bits, as well as the payload data, are transferred transparently. This finally results in transparent transmission of both the overhead bits and the payload data in the REG-R in the directions REG-R → REG-C and REG-R → LTU, except the REG specific overhead bits which are handled as described in subclause 5.7.

If the REG-R loses synchronization (*LOSW-R* = ONE) it starts a 2 second timer and moves to the Pending Deactivation-R State, where the signal as received from the REG-C transceiver is transmitted. If the synchronization is regained before the 2 second timer expires, then *LOSW-R* is set to ZERO and the HDSL transceiver at the REG-R returns to the Active-R State. If however the 2 s timer expires, then *LOSWT-R* is set to ONE and the HDSL transceiver at the REG-R changes to the Deactivated-R State.

During the Deactivated-R State, the HDSL transceiver at the REG-R is silent and looks for signal power from the HDSL transceiver at the LTU. When no power is detected (*LOS-R* = ONE) it changes to the Inactive State. Entering the Deactivated-R State results in forcing the REG-C to the Deactivated-C state, if the REG-C is in one of the states Activating-C, Active-C or Pending Deactivation-C.

5.6.6.1.2 HDSL transceiver states at the REG-C

During the Inactive-C State the HDSL transceiver at the REG-C is silent and *LOSW-C* = ONE. If the *ACTREQ* = ONE command from the REG-R transceiver indicates that the REG-R has entered the Active-R state it moves to the Activating-C State and follows the timeline shown in figure 11 for the LTU.

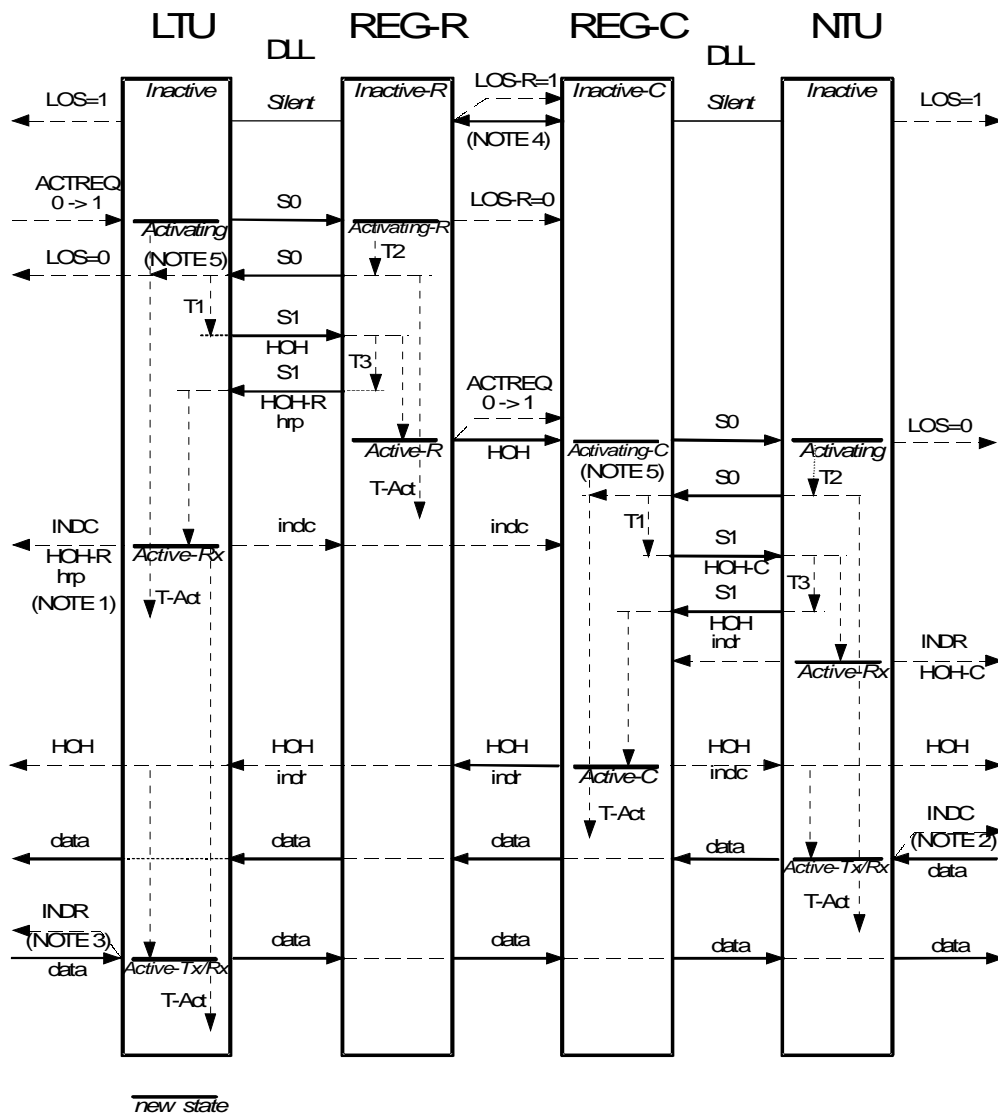
When the HDSL transceiver at the REG-C enters this state from the Inactive-C State, it starts timer *T-Act* and transmission of the *S0* signal. During the transmission of the *S0* signal, when it detects signal power from the HDSL transceiver at the NTU it starts timer *T1* and restarts timer *T-Act*. When the *T1* timer expires the HDSL transceiver at the REG-C starts to transmit the *S1* signal. The data transmitted in the payload and the overhead bits during the Activating-C State are ONE, in both directions REG-C → NTU and REG-C → REG-R. During the transmission of the *S1* signal it waits for the framed *S1* signal to gain synchronization. If the HDSL frame synchronization is detected then *LOSW-C* = ZERO and the REG-C enters the Active-C State and deactivates the timer *T-Act*. If the *T-Act* timer expires before *LOSW-C* becomes ZERO, the HDSL transceiver at the REG-C changes to the Deactivated-C State, ceases transmission and forces the REG-R into the Deactivated-R State. The further behaviour is as described below.

During the Active-C State both the overhead and payload data are transmitted transparently in both directions REG-C → NTU and REG-C → REG-R except the regenerator specific overhead bits, which are handled inside the REG. If

the HDSL frame synchronization is lost LOSW-C is set to ONE and the HDSL transceiver at the REG-C changes to the Pending Deactivated-C State and a 2 second timer is started.

During the Pending Deactivation-C State the signal transmitted is the same as received from REG-R. If synchronization is regained then LOSW-C is set to ZERO and the HDSL transceiver at the REG-C returns to the Active-C State. If the 2 second timer expires without synchronization, then LOSWT-C is set to ONE and the HDSL transceiver at the REG-C changes to the Deactivated-C State.

During the Deactivated-C State, the HDSL transceiver at the REG-C is silent and looks for signal power from the HDSL transceiver at the NTU. Entering the Deactivated-C State results in forcing the REG-R to the Deactivated-R State. When no power is detected (LOS-C = ONE) a 1 second timer is started and after this timer expires (LOST-C = ONE) the HDSL transceiver at the REG-C changes to the Inactive-C State.



NOTE 1: After having detected the status indicator INDC, the LTU starts to evaluate the indr- and hrp-bit. If an hrp-bit set to ONE is received no regenerator is present.

NOTE 2: If the indc = 0 has been received six times consecutively, the NTU becomes transparent for payload blocks.

NOTE 3: If the indr = 0 has been received six times consecutively, the LTU becomes transparent for payload blocks.

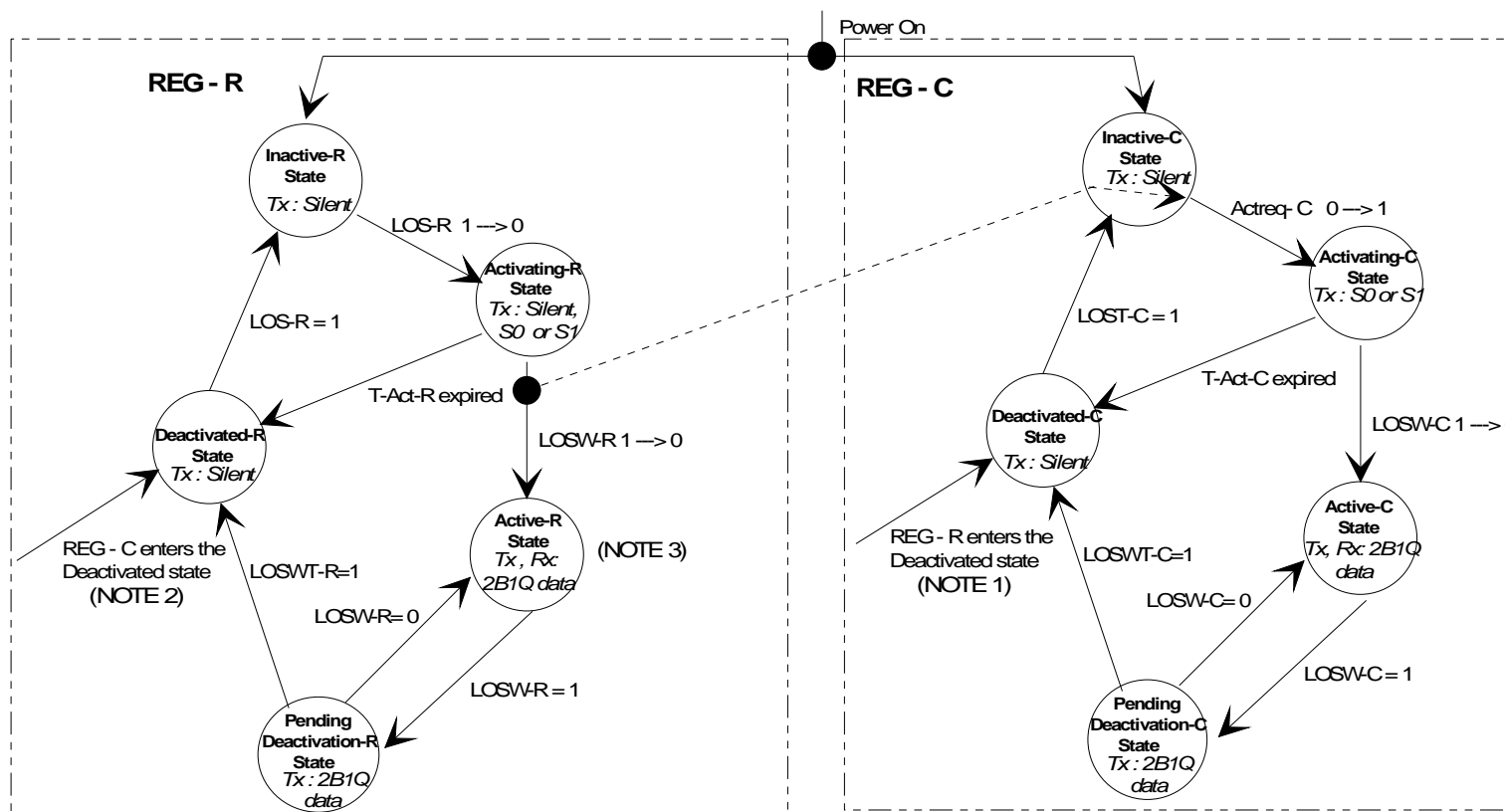
NOTE 4: Transceivers provide an all-ONE signal in the payload block and HOH to the succeeding circuitry as long as their receivers have not entered the active state.

NOTE 5: Timer T-Act is restarted after reception of S0 from the NTU, or REG-R, respectively.

NOTE 6: Timer T4 is an NTU/REG internal timer and is therefore not shown in this diagram.

NOTE 7: HOH indicates that all HOH-bits are active, while HOH-R and HOH-C indicate that only those HOH-bits are active, which are originated by the REG-R or REG-C respectively, all others are set to ONE.

Figure 16: Flow diagram for start-up with regenerator



NOTE 1: The REG-R entering the Deactivated-R State forces the REG-C to enter the Deactivated-C State, if the REG-C is in one of the states Activating-C, Active-C or Pending Deactivation-C.

NOTE 2: The REG-C entering the Deactivated-C State forces the REG-R to enter the Deactivated-R State, if the REG-R is in one of the states Activating-R, Active-R or Pending Deactivation-R.

NOTE 3: As long as the REG-C transceiver has not entered the Active-C State, only REG specific overhead bits are transmitted to the LTU. All other transmitted bits are ONE.

Figure 17: REG activation state diagram

5.7 Operation and Maintenance (O&M)

This subclause deals with operation and maintenance for transmission systems using HDSL technique. The O&M aspects for such systems are separated between the O&M functions of the HDSL core and those supported by the applications.

The following subclauses are divided with respect to the applications supported. Commands and responses of the system can either be transmitted through the application interfaces or via external O&M interfaces at maintenance reference points at the NTU and LTU as appropriate. Only the functionality of these O&M reference points will be specified in the present document.

The support of partial operation in a failure situation and of fractional installation shall be possible as an option.

5.7.1 Functions at the LTU external O&M reference point

These O&M functions requested by an external O&M entity are originated within the O&M functional block (maintenance) at the LTU. The network elements addressed by these commands are identified in table 14.

5.7.2 Functions at the NTU external O&M reference point

The NTU external O&M reference point may be implemented as an option and is not completely specified in the present document.

Only the use of visible indications towards the customer are dealt with. The use of a data interface for reporting to/from the customer is not foreseen. Access to the operators TMN system via this reference point shall not be possible.

Examples of reporting towards the customer at the NTU may be:

- indication of power;
- indication of severe failures;
- indication of testing from the network side.

Table 14: Control functions at the external O&M interface

Function	HDSL transceiver pair	Addressed network element (see note 2)
Loopback control	all	LTU/REG
Loopback control of application frame	(see note 5)	NTU (see note 3)
Start-up control	all	LTU
Reset control	all	LTU/NTU/REG
CRC error reporting on each pair	all	LTU/NTU/REG (see note 1)
Set corrupted CRC on each pair	all	LTU/NTU/REG
Response from each pair for corrupted CRC	all	LTU/NTU/REG
Request for transmission quality on each pair (see note 7)	all	LTU/NTU/REG
Response for transmission quality from each pair (see note 7)	all	LTU/NTU/REG
Set configuration	(see note 5)	LTU/NTU (interface block)
Read configuration	(see note 5)	LTU/NTU (interface block)
Status report	(see note 6)	LTU/NTU/REG
Excessive error ratio on each pair	all	LTU/NTU/REG (interface block) (see note 4)
Identification of equipment	(see note 5)	LTU/NTU/REG
Other failure indications	all	LTU/NTU/REG
NOTE 1: The calculation of these parameters is based on the CRC-6 procedure inside each subsystem.		
NOTE 2: The use of a regenerator is optional.		
NOTE 3: The location of the loopback of the application frame shall be as near as possible to the application interface. The loopback shall be complete.		
NOTE 4: The excessive error rate indication may be set if 150 errored frames out of 166 frames (1 second) are detected.		
NOTE 5: This function is transported transparently through the HDSL core. This note is not relevant if a regenerator is addressed.		
NOTE 6: The status report of network elements within the access digital section shall reflect the status of the HDSL core and the application.		
NOTE 7: Transmission quality is represented by noise margin as defined in subclause 5.5.7 or by signal quality as defined in annex B.		

5.7.3 O&M messages and functions supported by the HDSL core

In this subclause messages are described which are conveyed inside the HDSL frame for O&M purposes. In addition O&M functions are defined which have to be located inside the HDSL core. These messages and functions are listed in table 15.

Table 15: O&M messages and functions supported by the HDSL core

Messages/functions	O&M core	local	Core related function	available on each pair	HOH- bit [additional OH-bits in payload]	eoc-message	addressed element		
							L T U	R E G	N T U
Reset control	→	*	y	n			*		
Start-up control	→	*	y	n			*		
Pair identification detection	←	*	y	y			*		*
Loopback control for LTU line side	→	*	y	n			*		
Loopback control for REG	→		y	n		*		*	
Loopback control for application frame	→		n	n		*			*
CRC error detected at LTU	←	*	y	y			*		
CRC error detected at REG-R	←		y	y	rrbe			*	
CRC error detected at REG-C	←		y	y	rcbe			*	
CRC error detected at NTU	←		y	y	febe				*
Corrupted CRC at LTU	→	*	y	y			*		
Corrupted CRC at REG-R	→		y	y		*		*	
Corrupted CRC at REG-C	→		y	y		*		*	
Corrupted CRC at NTU	→		y	y		*			*
LOS/LFA at LTU line side (see note 1)	←	*	y	y			*		
LOS/LFA at REG-R (see note 1)	←		y	y				*	
LOS/LFA at REG-C (see note 1)	←		y	y				*	
LOS/LFA at line side of NTU (see note 1)	←		y	y					*
Pair identification for two pair systems and three pair systems	→		y	y	[Z11 to Z33] [Z11 to Z22]		*		
Request transmission quality LTU	→	*	y	y			*		
Request transmission quality REG-R (REG-C)	→		y	y		*		*	
Request transmission quality NTU	→		y	y		*			*
Transmission quality LTU	←	*	y	y			*		
Transmission quality REG-R (REG-C)	←		y	y		*		*	
Transmission quality NTU	←		y	y		*			*
Request status REG	→		y	y		*		*	
Request status NTU	→		y	n		*			*
REG status (see note 2)	←		y	y		*		*	
NTU status (see note 2)	←		y	n		*			*
Read NTU configuration (see note 3)	→		n	n		*			*
Write NTU configuration (see note 3)	→		n	n		*			*
NTU configuration	←		n	n		*			*
Request equipment identification REG	→		y	y		*		*	
Request equipment identification NTU	→		n	n		*			*
Equipment identification REG	←		n	y		*		*	
Equipment identification NTU	←		n	n		*			*
Internal alarm in NTU (see note 4)	←		y	n	rta				*
Internal alarm in REG (see note 4)	←		y	y	rega			*	
LOS at the application interface of the LTU (see note 5)	→		n	n	losd (LTU → NTU)		*		
LOS at the application interface of the NTU (see note 5)	←		n	n	losd (NTU → LTU)				*
Bipolar violation at the application interface of the LTU (see note 6)	→		n	n	bpv (LTU → NTU)		*		

Messages/functions	O&M core	local	Core related function	available on each pair	HOH- bit [additional OH-bits in payload]	eoc-message	addressed element		
							L T U	R E G	N T U
Bipolar violation at the application interface of the NTU (see note 6)	←		n	n	bpv (NTU → LTU)			*	
NOTE 1: LOS or LFA at the line side of the LTU, NTU or REG leads to a deactivation of the respective path after 2 seconds and therefore always results in an LOS message from the HDSL core to the O&M functional block in the LTU. The LTU O&M unit cannot determine however the location of the fault.									
NOTE 2: The status register contains single bits representing the current status of the equipment. This information can be used to get detailed information, e. g. after receiving internal alarm bits rta or rega.									
NOTE 3: The configuration register of the NTU contains dedicated bits which allow for remote configuration of the equipment by the LTU. Examples are transparent/non-transparent mode, masking of alarms, equipment behaviour during fault conditions (e.g. transmitting of AIS).									
NOTE 4: The internal alarm bits are used for signalling equipment internal failure conditions, which are not covered by separate indicator bits. Possible events are:									
<ul style="list-style-type: none"> - Loss of internal clock sources; - Max delay difference between pairs exceeded; - ROM/RAM test negative. 									
NOTE 5: The use of this function is application dependent.									
NOTE 6: The general need for this function has not been identified. It is left to the network operators to request this functions for particular applications.									

5.7.4 Power feeding related O&M functions

Table 16: Power feeding related functions

Function	O&M P	local	HOH-bits	eoc-messages	location		
					LTU	REG	NTU
NTU power source 1 failure	←		ps1				
NTU power source 2 failure	←		ps2				

5.7.5 Regenerator behaviour

5.7.5.1 Response to LOS/LFA

A regenerator shall respond to LOS/LFA. When LOS/LFA is recognized the behaviour of the REG shall be as follows.

Both sides of the REG shall be deactivated autonomously by the REG when LOS/LFA is detected on any HDSL line interface. The conditions for detecting LOS/LFA are described in subclause 5.6.

NOTE: This will finally result in deactivation of the subsystem after detection of LOS/LFA anywhere in the subsystem and both LTU and NTU will identify LOS/LFA for this subsystem. The LOS/LFA detection is a function of the individual HDSL transceivers.

5.7.5.2 Operation of loopback 1A

The activation of loopback 1A in any subsystem of the transceiver is initiated by the LTU by the appropriate eoc message as described in subclause 5.5. The loopback request may be started simultaneously with the beginning of the start-up procedure or during an already active HDSL link.

In the first case the loopback request may be transmitted toward the REG as soon as signal S1 according to subclause 5.6 is transmitted in the direction LTU → NTU. After the eoc message has been detected in the REG the loopback is closed accordingly.

In the second case of an already active link the control unit in the REG closes the loop as soon as the eoc-message has been detected. The detailed procedure of reaching the synchronous loopback state is up to the vendor. (It may be necessary to reset the REG-C transceiver, so that its equalizer and echo canceller coefficients may converge under the loopback conditions).

A successfully closed loopback may be detected in the LTU by evaluating the valid received Z-bits used for path identification. The loopback is transparent, i.e. the looped back signal is also transmitted toward the NTU.

During an active loopback 1A the operation of the HDSL overhead bits shall be as follows:

- the eoc channel is not looped back but is fully operating between the LTU and the REG as described in subclause 5.5 as long as the messages sent by the LTU contain the REG address "10". When detecting any other address the REG inserts the "Hold State" message with its own address in the direction REG → LTU;
- all indicator bits, except the REG specific bits hrp, rega, rrbe and rcbe which are operating normally, are looped back.

To deactivate loopback 1A the LTU transmits the "Return to Normal" message together with the address "10" in the eoc channel. After detecting this message the REG control unit deactivates autonomously the REG-C transceiver and cancels the loopback operation.

If the HDSL link between the LTU and the REG is still active the REG control unit immediately starts to activate the link between the REG and the NTU as described in subclause 5.6. The successful completion of the start-up procedure may be detected by the LTU by evaluating the Z-bits used for path identification.

5.8 Electrical characteristics of a single 2B1Q transceiver

5.8.1 General

This subclause describes the electrical characteristics of a single HDSL transceiver.

The electrical characteristics of a HDSL transceiver shall be such as to enable the performance requirements of the applications listed in clause 7 to be met. In addition, the following specific electrical characteristics are required.

Means should be provided in order to enable the testing of the electrical characteristics of a single 2B1Q transceiver.

5.8.2 Transmitter/Receiver impedance and return loss

The nominal driving point impedance at the line side of an HDSL transceiver shall be 135 Ω .

The minimum return loss with respect to 135 Ω over a frequency band of 1 kHz to 1 MHz shall be:

- 16 dB from 40 kHz to 196 kHz as shown in figure 18 for 392 kbaud systems;
- 16 dB from 40 kHz to 292 kHz as shown in figure 19 for 584 kbaud systems; and
- 16 dB from 80 kHz to 485 kHz as shown in figure 20 for 1 160 kbaud systems;

with a slope of 20 dB/decade below and above these frequencies respectively.

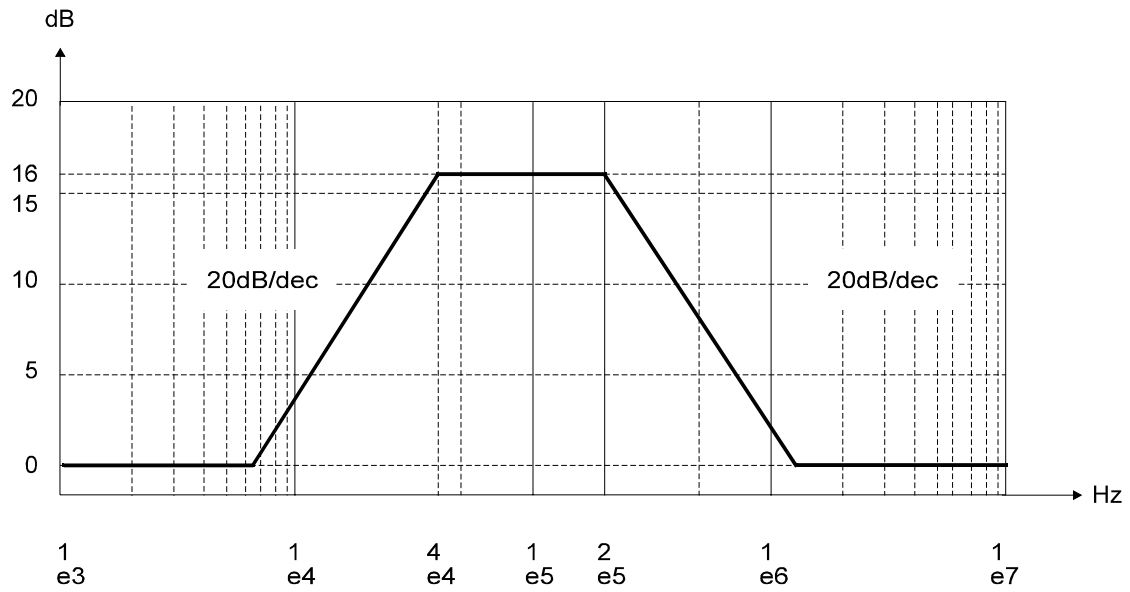


Figure 18: Minimum return loss of a 392 kbaud system

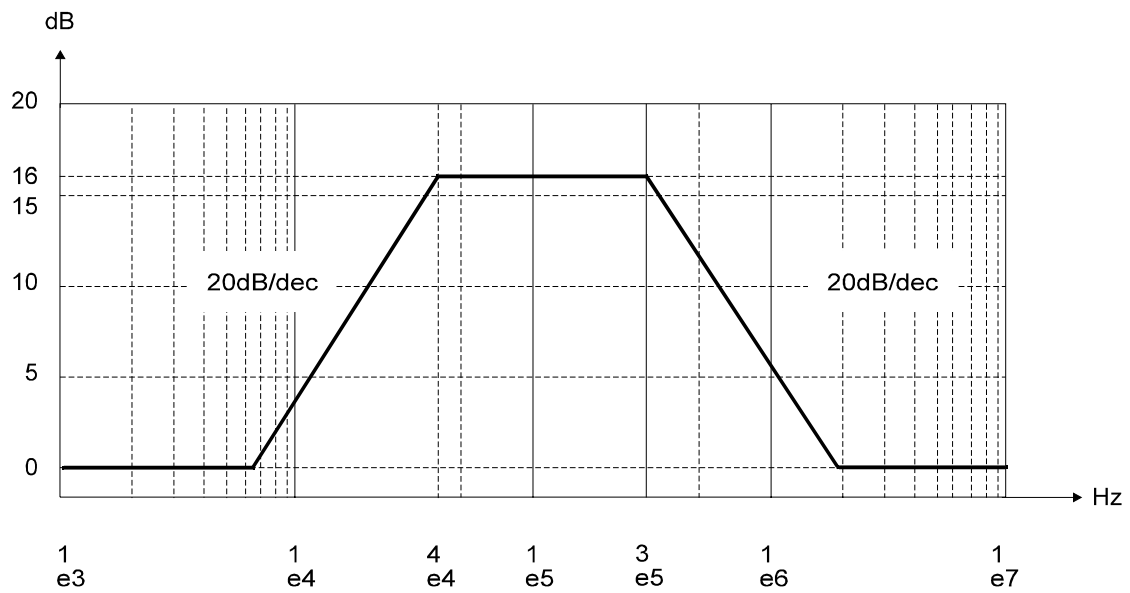


Figure 19: Minimum return loss of a 584 kbaud system

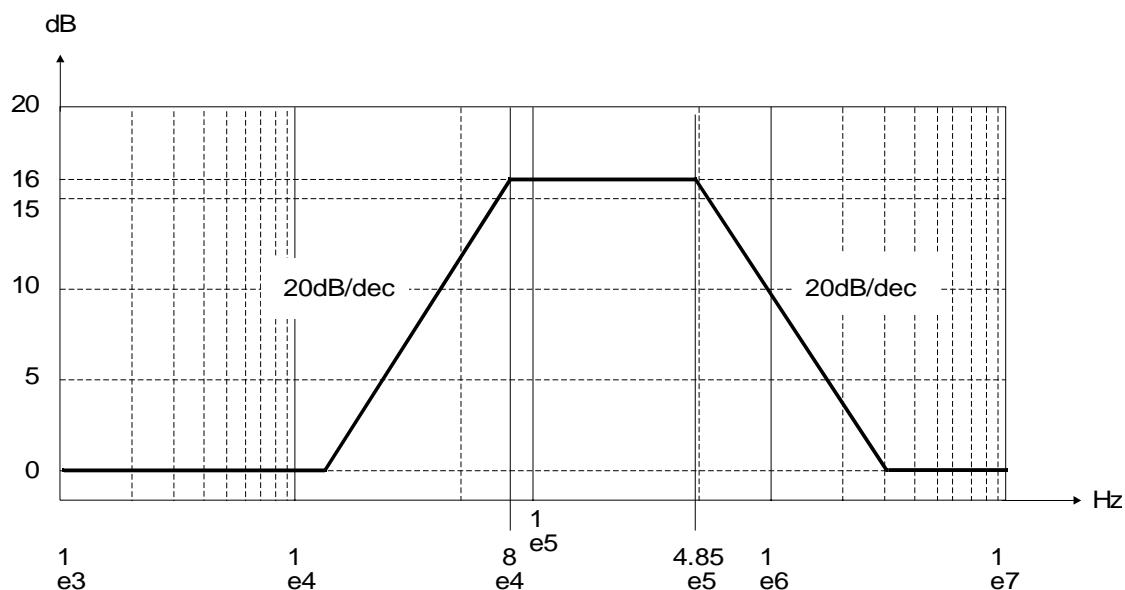


Figure 20: Minimum return loss of a 1 160 kbaud system

5.8.3 Transceiver reference clock

The reference clock shall be:

- for one pair 2 320 kHz \pm 32 ppm;
- for two pair 1 168 kHz \pm 32 ppm;
- for three pair 784 kHz \pm 32 ppm.

5.8.4 Transmitter output characteristics

Unless otherwise indicated, the following specification apply with a resistive load impedance corresponding to the nominal.

5.8.4.1 Pulse amplitude

The nominal peak of the largest pulse shall be 2,64 V for the three and two pair system and 2,50 V for the one pair system.

5.8.4.2 Pulse shape

The transmitted pulse shall have the shape specified in figure 21 for the three and two pair system and in figure 22 for the one pair system.

The pulse mask for the four quaternary symbols shall be obtained by multiplying the normalized pulse mask shown in figure 21 by 2,64 V, 0,88 V, -0,88 V or -2,64 V and in figure 22 by 2,50 V, 0,833 V, -0,833 V and -2,50 V.

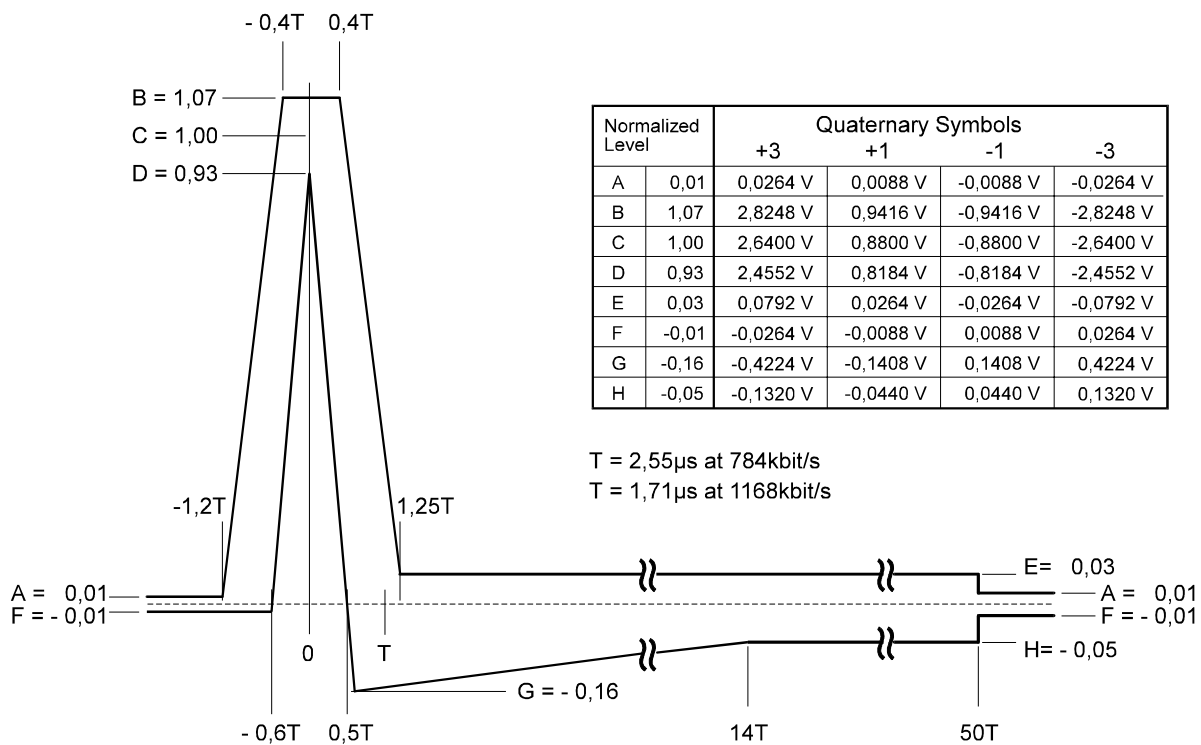


Figure 21: Transmit pulse for two and three pair systems; normalized pulse mask

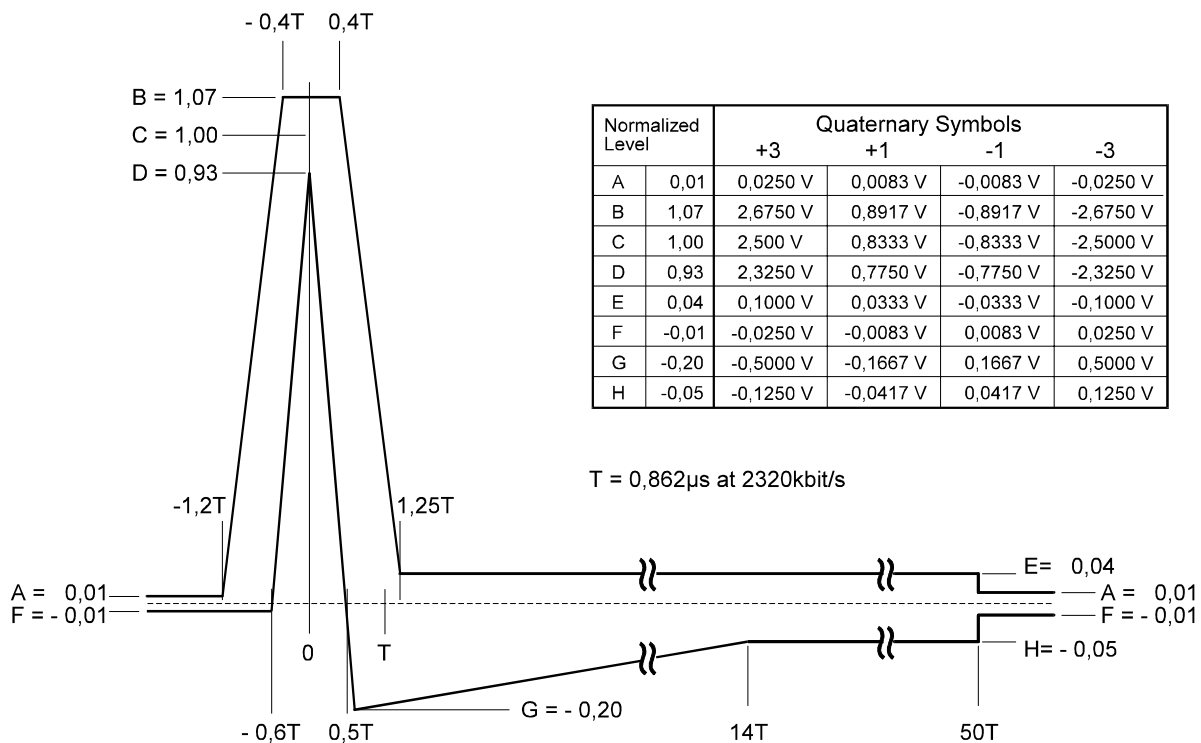


Figure 22: Transmit pulse for a one pair system; normalized pulse mask

5.8.4.3 Power Spectral Density (PSD)

5.8.4.3.1 PSD for 392 kbaud systems

The upper bound of the average PSD of the signal transmitted by the HDSL transmitter shall be as described in figure 23:

- -37 dBm/Hz from 0 Hz to 196 kHz;
- -80 dB/decade fall from -37 dBm/Hz at 196 kHz to -117 dBm/Hz at 1,96 MHz;
- -117 dBm/Hz above 1,96 MHz.

5.8.4.3.2 PSD for 584 kbaud systems

The upper bound of the average PSD of the signal transmitted by the HDSL transmitter shall be as described in figure 24:

- -39 dBm/Hz from 0 Hz to 292 kHz;
- -80 dB/decade fall from -39 dBm/Hz at 292 kHz to -119 dBm/Hz at 2,92 MHz;
- -119 dBm/Hz above 2,92 MHz.

5.8.4.3.3 PSD for 1 160 kbaud systems

The upper bound of the average PSD of the signal transmitted by the HDSL transmitter shall be as described in figure 25:

- -41,5 dBm/Hz from 0 Hz to 485 kHz;
- -80 dB/decade fall from -41,5 dBm/Hz at 485 kHz to -121,5 dBm/Hz at 4,85 MHz;
- -121,5 dBm/Hz above 4,85 MHz.

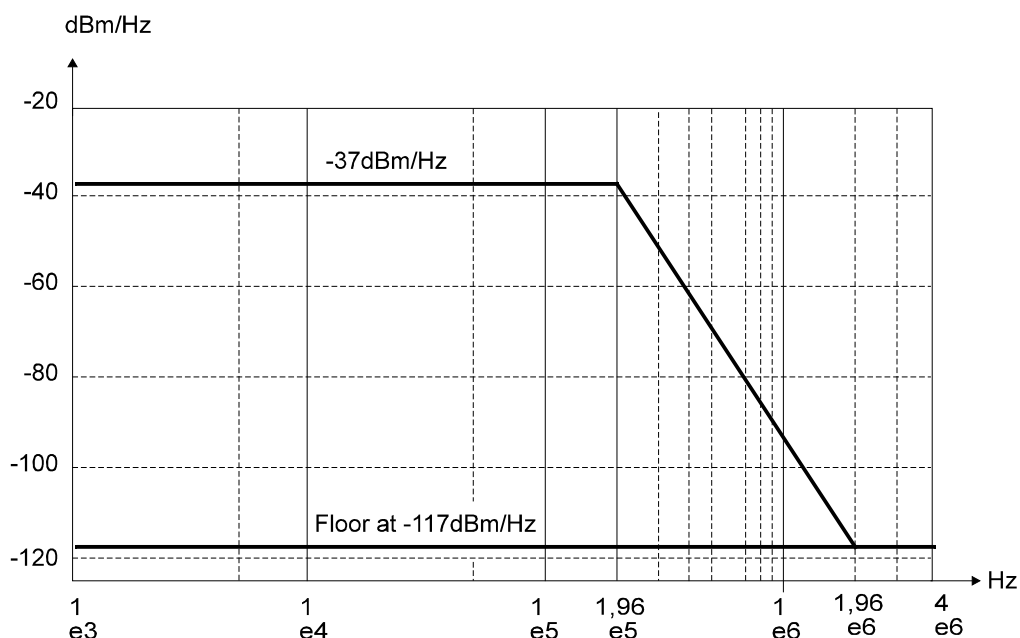


Figure 23: Upper bound of the average PSD of a 392 kbaud system

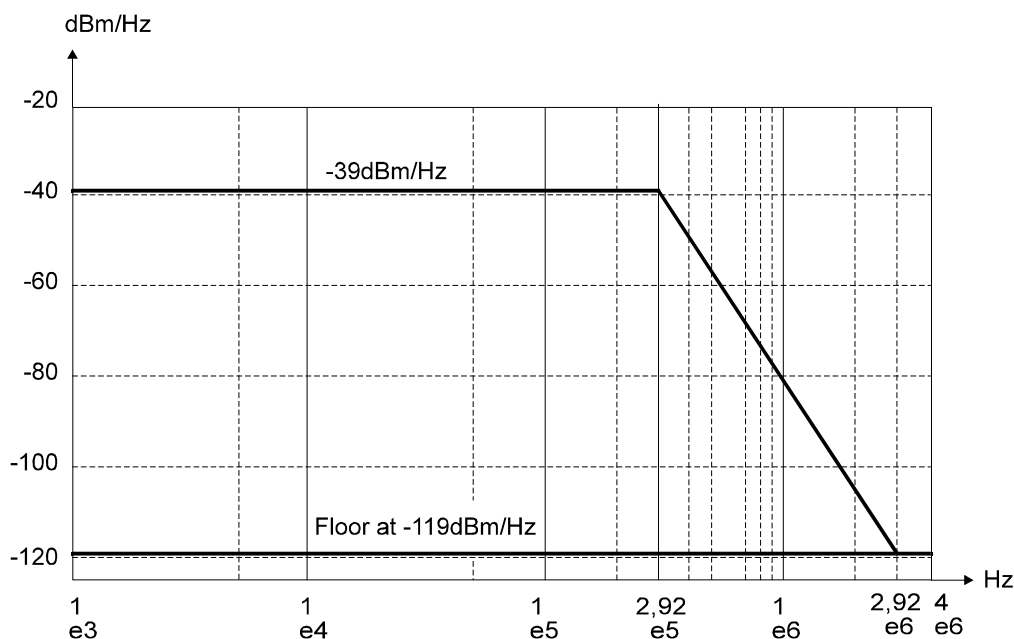


Figure 24: Upper bound of the average PSD of a 584 kbaud system

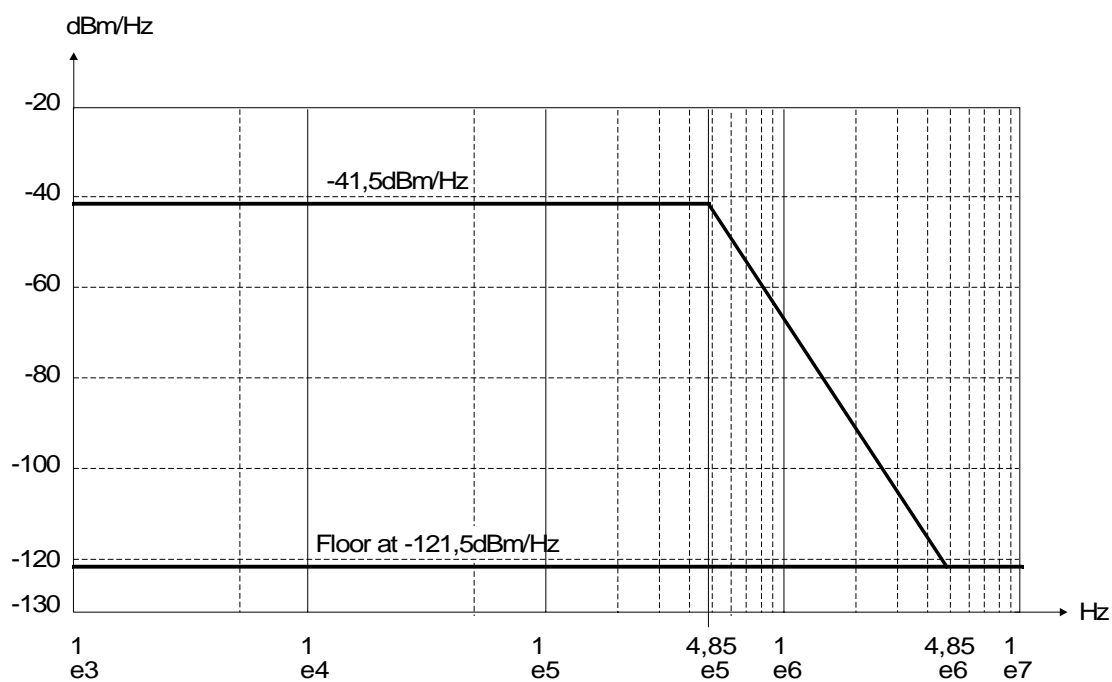


Figure 25: Upper bound of the average PSD of a 1 160 kbaud system

5.8.4.4 Total power

The average power of a signal (excluding remote power feeding) consisting of a framed sequence of symbols with a frame word and equiprobable symbols in all other positions should be between 13,0 dBm and 14,0 dBm over the frequency band from 0 Hz to 784 kHz for 392 kbaud systems, from 0 Hz to 1 168 kHz for 584 kbaud systems and from 0 Hz to 2 320 kHz for 1 160 kbaud systems.

5.8.5 Unbalance about earth

5.8.5.1 Longitudinal Conversion Loss (LCL)

$$\text{LCL} = 20 \log (e_l/e_m) \text{ [dB]}$$

where e_l is the applied longitudinal voltage referenced to the building ground and e_m is the resultant metallic voltage appearing across a 135 Ω termination.

The LCL of the system shall meet the requirement of:

- 50 dB between 5 kHz and 196 kHz for a 392 kbaud system as shown in figure 26;
- 50 dB between 5 kHz and 292 kHz for a 584 kbaud system as shown in figure 27; and
- 50 dB between 5 kHz and 485 kHz for a 1 160 kbaud system as shown in figure 28.

This requirement ensures that the overall LCL is not significantly worse than that of the DLLs alone.

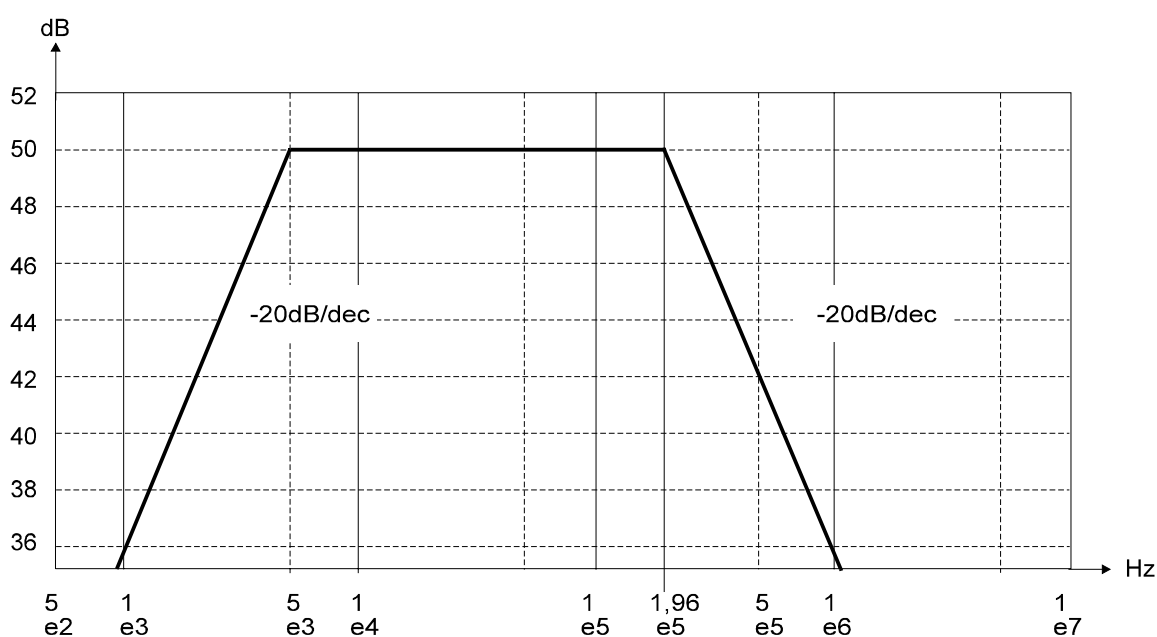


Figure 26: Minimum LCL for a 392 kbaud system

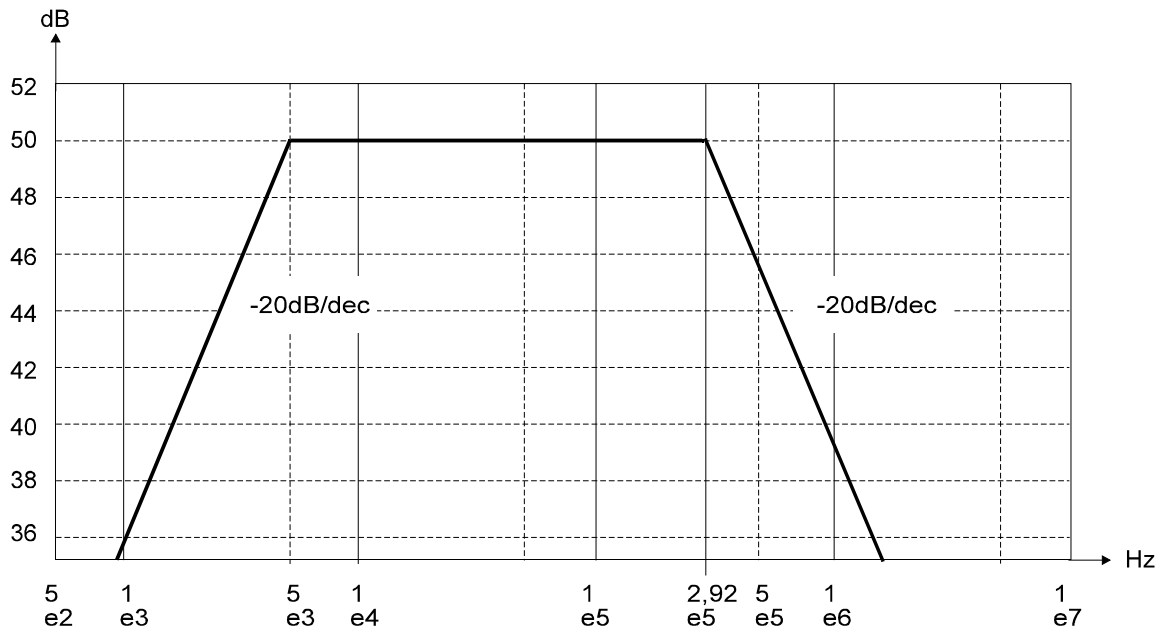


Figure 27: Minimum LCL for a 584 kbaud system

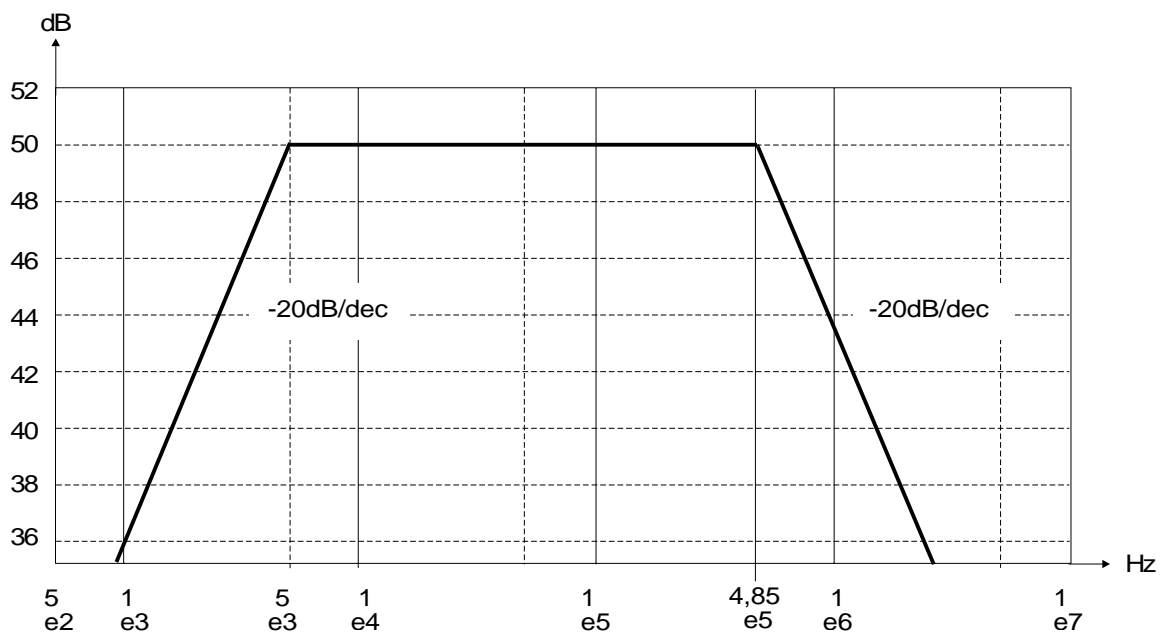
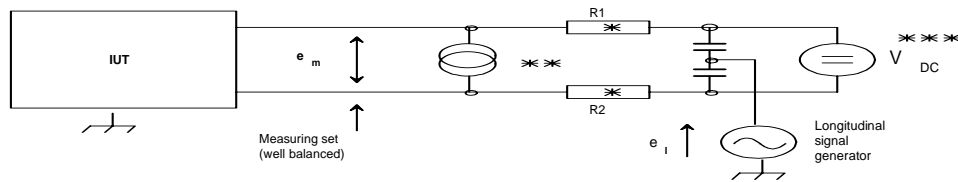


Figure 28: Minimum LCL for a 1 160 kbaud system

Figure 29 defines a measurement method for LCL. For direct use of this configuration, measurement should be performed with the Implementation Under Test (IUT) powered up but inactive (no transmitted signal; driving 0 V).



NOTE 1: * These resistors have to be matched: $R1 = R2 = 135/2 \Omega$ and $R1/R2 = 1 \pm 0,1 \%$.

NOTE 2: ** For LTU test only if remote power feeding is supplied.

NOTE 3: *** For NTU test only if remote power feeding is required.

NOTE 4: During regenerator test (where required) each wire on the side which is not under test shall be connected to ground by a terminating impedance having the value of $135/2 \Omega$ in series with a capacitance of $0,33 \mu\text{F}$.

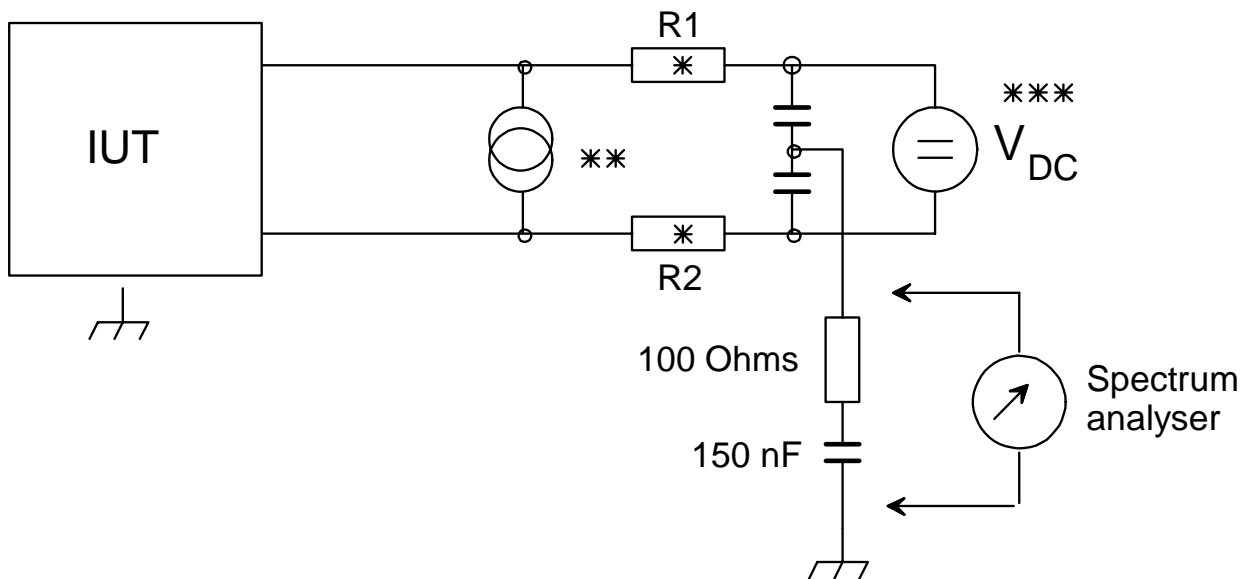
Figure 29: Measurement method for LCL

5.8.5.2 Longitudinal output voltage

The longitudinal component of the output signal shall have an rms voltage, in any 4 kHz equivalent bandwidth averaged in any second period, $< -50 \text{ dBV}$ over the frequency range 100 Hz to 400 kHz. Compliance with this limitation is required with a longitudinal termination having an impedance of 100Ω in series with $0,15 \mu\text{F}$ nominal. The Electromagnetic Compatibility (EMC) requirements of subclause 9.4 shall also be met.

Figure 30 defines a measurement method for longitudinal output voltage. For direct use of this test configuration, the IUT should be able to generate a signal in the absence of a signal from the far end.

The ground reference for these measurements shall be the building ground.



NOTE 1: * These resistors have to be matched: $R1 = R2 = 135/2 \Omega$ and $R1/R2 = 1 \pm 0,1 \%$.

NOTE 2: ** For LTU test only if remote power feeding is supplied.

NOTE 3: *** For NTU test only if remote power feeding is required.

NOTE 4: During regenerator test (where required) each wire on the side which is not under test has to be connected to ground by a terminating impedance having the value of $135/2 \Omega$ in series with a capacitance of $0,33 \mu\text{F}$.

Figure 30: Measurement method for longitudinal output voltage

5.9 Performance of individual HDSL transceivers

5.9.1 Performance requirements

Performance limits for the overall system are defined in clause 7. The performance of the individual HDSL transceivers shall be such that these overall performance limits are met. As the binary signal of the individual transceivers is not available at an external interface for testing, it is not considered feasible to test the performance of the individual HDSL transceivers. For the purpose of conformance, each HDSL system is required to have an individual performance such that the overall application performance requirements defined in clause 7 for the appropriate application are met.

5.9.2 DLL physical models (test loops)

Some representative models of DLLs (test loops) for evaluating the performance of transceivers for transmission systems are defined in figure 32.

5.9.3 Jitter and wander

5.9.3.1 General

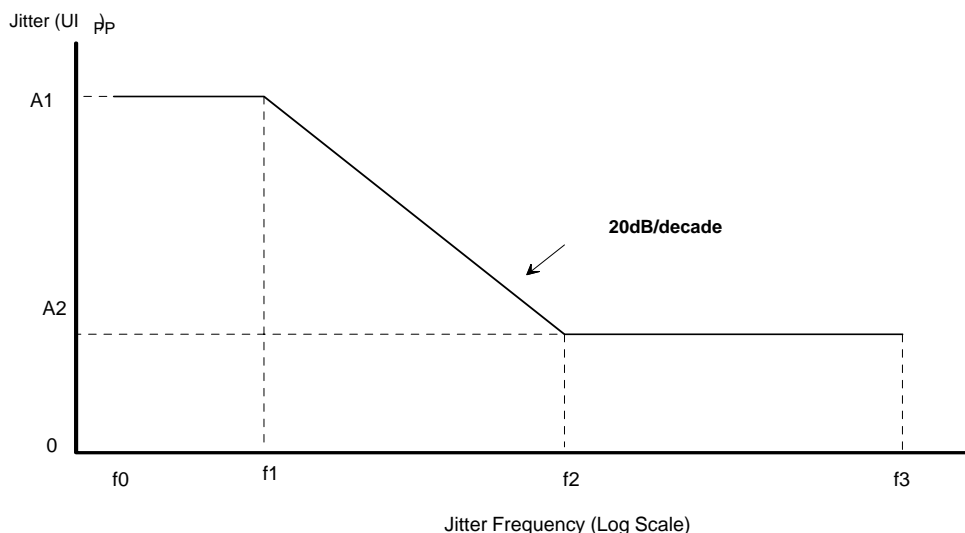
The jitter and performance limits specified in clause 7 shall be supported by the jitter limits of the individual HDSL transmission systems. However, due to the bi-directional transmission on the two-wire line and due to severe intersymbol interference no well defined signal transitions are available on the two-wire signal. It will therefore be necessary to provide clock interfaces to enable the following requirements to be tested. The jitter limits given below shall be satisfied regardless of the length of the local line and the inclusion of regenerators, provided that they are covered by the transmission media characteristics of subclause 6.3. The limits shall be met regardless of the transmitted signal. In this subclause, jitter is specified in terms of unit intervals (UI) of the nominal line baud rate which is 392 kbaud (2,55 μ s) for the three pair system and 584 kbaud (1,71 μ s) for the two pair system and 1 160 kbaud (0,862 μ s) for the one pair system.

5.9.3.2 Input jitter tolerance at the HDSL transceiver at the NTU

The NTU shall meet the performance objectives specified in clause 7 with wander/jitter sinusoidal characteristics as indicated in figure 31, and with values as defined in table 17 below for single jitter frequencies in the range of 0,1 Hz to 100 kHz superimposed on the test clock source, and with the received signal baud rate in the range of ± 32 ppm.

Table 17: Values for wander/jitter characteristics

A1	A2	f0	f1	f2	f3
0,15 UIpp	0,015 UIpp	0,1 Hz	0,5 Hz	5 Hz	100 kHz



NOTE: Unit Interval (UI) = 2,55 μ s for 392 kbaud systems.
 Unit Interval (UI) = 1,71 μ s for 584 kbaud systems.
 Unit Interval (UI) = 0,862 μ s for 1 160 kbaud systems.

Figure 31: Range of permissible sinusoidal input jitter

5.9.3.3 Output jitter limitations at the HDSL transceiver at the NTU

The jitter on the transmitted 2B1Q signal of the NTU towards the LTU in the absence of input jitter shall be less than A2 when measured with a band pass filter having a 20 dB/decade roll off with cut off frequencies at f2 and f3.

The maximum (peak) departure of the phase of the output signal from its average phase measured over 1/f0 seconds shall not exceed A1.

5.9.3.4 Input jitter tolerance at the HDSL transceiver at the LTU

The LTU shall meet the performance objectives specified in clause 7 with wander/jitter of A2 for single jitter frequencies in the range of f0 to f3 superimposed on the test clock source, and with the signal baud rate in the range ± 32 ppm.

5.9.3.5 Output jitter limitation of the HDSL transceiver at the LTU

The jitter on the transmitted 2B1Q signal of the LTU towards the NTU shall be less than A2 when measured with a band pass filter having a 20 dB/decade roll off with cut off frequencies at f2 and f3.

6 Common circuitry specification

6.1 Delay difference buffer

In order to compensate for any difference in total transmission time of the HDSL frames on different pairs, due to the pair differences described in subclause 5.2.4.2, as well as to delays due to signal processing in the HDSL transceivers in the LTU, NTU and possible REG, a delay difference buffer shall be implemented in the common circuitry. The function of this delay difference buffer is to align the HDSL frames so that the core frames can be correctly reassembled. This buffer should be capable of absorbing a maximum delay difference of 60 μ s.

6.2 The pair identification mechanism

The pair identification procedure provides for the correct information of the NTU on the pair numbers selected by the LTU in a two or three pair system. It is based on the use of the Z-bits. The following is a definition of a pair identification mechanism that has to be completed for each installed pair separately, and agrees with the local procedures for activation. The pair identification procedure is operated only between the LTU and the NTU, the optional REG transfers the related information transparently.

6.2.1 Pair identification initial values

At the beginning of the start-up procedure, each HDSL transceiver in the LTU is assigned with a pair identification number, which may be 1, 2 or 3 for three pair systems or 1 or 2 for two pair systems. The HDSL transceivers in the NTU are not assigned, but defined by the received Z-bits according to tables 18 and 19. When an HDSL transceiver at the LTU reaches the Active-Tx/Rx State in the activation procedure, as described in subclause 5.6.5 the common circuitry sets the indicator bits Z_{m1} , Z_{m2} and Z_{m3} for three pair systems or Z_{m1} and Z_{m2} for two pair systems according to tables 18 and 19, using the pair identification number it was assigned.

Table 18: Pair identification bit assignment for the three pair system

Pair number [m]	Z_{m1}	Z_{m2}	Z_{m3}
1	$Z_{11} = 1$	$Z_{12} = 0$	$Z_{13} = 0$
2	$Z_{21} = 0$	$Z_{22} = 1$	$Z_{23} = 0$
3	$Z_{31} = 0$	$Z_{32} = 0$	$Z_{33} = 1$

Table 19: Pair identification bit assignment for the two pair system

Pair number [m]	Z_{m1}	Z_{m2}
1	$Z_{11} = 1$	$Z_{12} = 0$
2	$Z_{21} = 0$	$Z_{22} = 1$

6.2.2 Pair identification at the NTU

Prior to the completion of the evaluation process of the individual pair, the transmitted Z-bits are set to ONE. When the HDSL transceiver at the NTU enters the Active-Tx/Rx State the common circuitry starts to look at the Z-bits. If it detects a valid pattern according to tables 18 or 19 respectively in six consecutive HDSL frames and the same pattern has not been detected on another pair before, then the evaluation process is completed successfully for this pair and the outgoing pair identification Z-bits are set to equal the recognized Z-bits for the whole actual activation period. When the common circuitry detects a complete valid matrix according to tables 18 or 19 it can achieve the correct data assignment and becomes transparent for the core frame data.

6.2.3 Pair identification at the LTU

After starting the transmission of the Z-bits the common circuitry starts to look at the received Z-bits. Initially, it should detect that all the pair identification Z-bits are ONE. When the HDSL transceiver at the NTU reflects the received Z-bits the common circuitry at the LTU will detect the pair identification number. When it finds its own valid pattern in six consecutive HDSL frames, the NTU has acknowledged the pair identification for this individual pair. If the Z-bits for all installed pairs are acknowledged the common circuitry becomes transparent for the core frame data.

The identification procedure introduces a delay of at least 12 frames (72 ms) between transition to the Active-Tx/Rx State and transparent data transfer, because valid patterns are required for six consecutive frames at each side.

6.3 Laboratory performance measurements

6.3.1 General

The performance requirements have been specified so that the HDSL transceivers are tolerant to NEXT, impulsive noise and shaped noise, and not optimized for only one operating condition.

The laboratory performance measurement of a particular HDSL transmission system requires the following preparations:

- definition of a number of DLL models to represent physical and electrical characteristics encountered in local line distribution networks;
- simulation of the electrical environment caused by impulse noise and finite crosstalk coupling loss to other pairs in the same cable;
- specification of laboratory performance tests to verify that the performance limits referred to in clause 7 will be met.

Some representative models of DLLs (test loops) for evaluating the performance of transceivers for transmission systems are defined in figure 32, the basic test cable characteristics are given in annex A.

6.3.2 Test configuration

It is assumed that the various applications described in clause 7 shall operate over a number of pairs each connected to an individual 784 kbit/s, 1 168 kbit/s or 2 320 kbit/s 2B1Q duplex HDSL transmission system. The number of pairs required for each application and for each bit rate is described in clause 7. Performance requirements should relate to the integrity of the data at the application interface when individual transmission systems are subjected to synthesized impairments. In this way access is not required to the raw data transported by the individual transceivers. Data errors can therefore be measured at the application interface, avoiding the need for test access to the individual data channels.

A representative test arrangement is shown in figure 34.

The Bit Error Ratio Test Set (BERTS) applies a $2^{15}-1$ Pseudo-Random Bit Sequence (PRBS) test signal to the transmitter in the direction under test at the bit-rate required by the application interface. Impairments (when required by the test) are injected at the input of the appropriate HDSL transceivers at the receiver end of the path, and the reconstructed data is then returned to the BERTS. The transmitter in the opposing direction shall be fed with a similar PRBS signal, although the reconstructed signal in this path need not be monitored.

The test performance of the HDSL transceiver shall be such that the Bit Error Ratio (BER) on the disturbed system is less than (10^{-7} divided by the number of pairs) while transmitting a PRBS. The BER should be measured after at least 10^9 bits have been transmitted.

The tests are carried out with zero margin, that is, with no additional attenuation added to the test pairs. It is expected that network operators will calculate their own margins for planning purposes based on a knowledge of the relationship between this standard test set and their network characteristics.

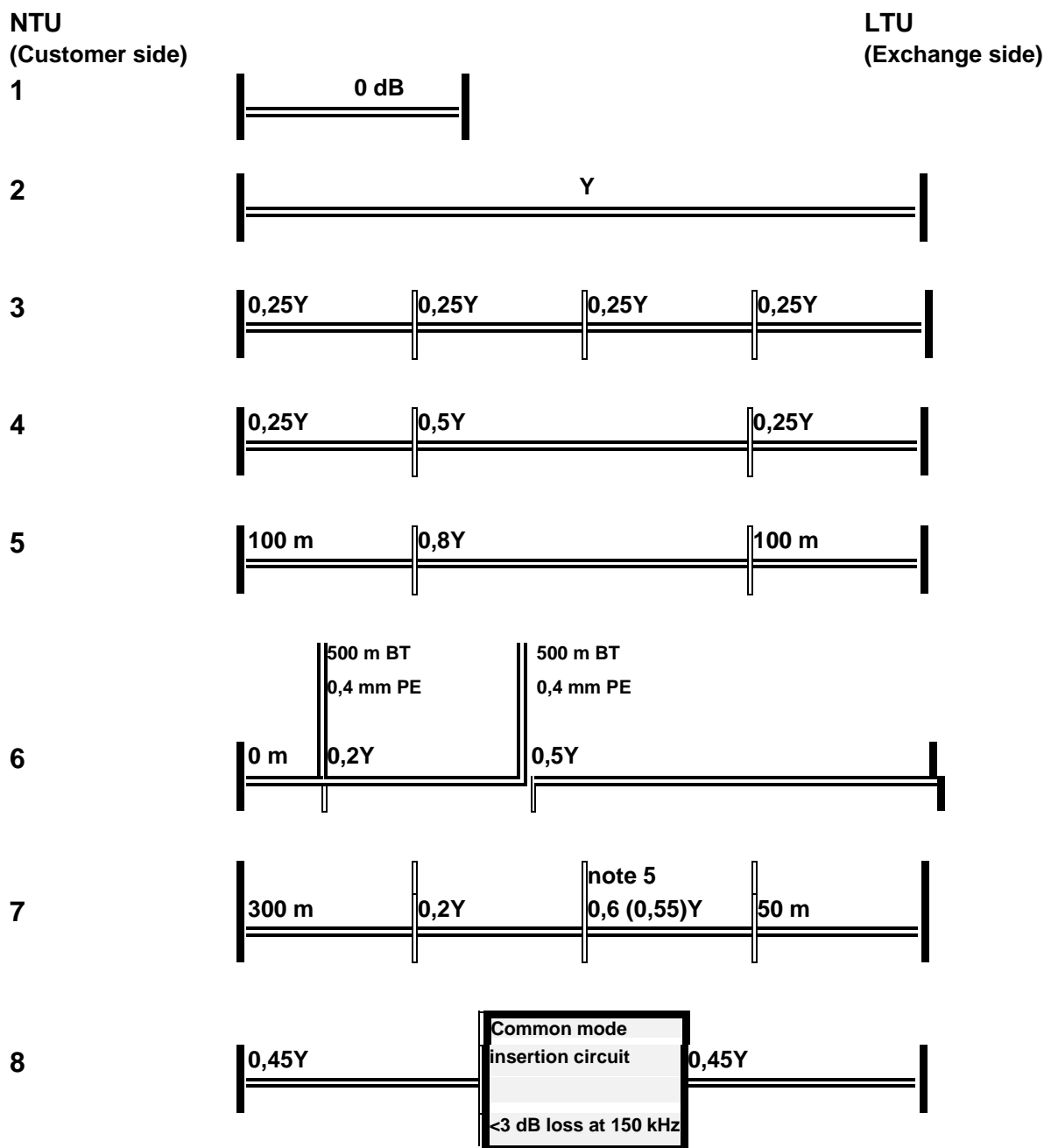
It is considered sufficient to use a representative combination of test pairs for performance testing. The test pairs should be adjusted to achieve the required sinewave insertion loss of the individual sections when measured at 150 kHz. (It is not considered reliable to measure the overall sinewave attenuation, as impedance discontinuities can result in non-linear effects in the frequency response of some pairs).

Two distinct classes of added disturbance are injected: Shaped test noise (specified in subclause 6.3.3) and Impulses (defined in subclause 6.3.4). A further test (specified in subclause 6.3.5) tests the common mode rejection capability of the system under test, and a test for determining the susceptibility to micro-interruptions is given in subclause 6.3.6.

Test sequences are shown in table 20.

Table 20: Test sequence for performance testing

N	Test Path	Direction	Comments
1	#1 (see note 1)	Forward	Y = 0 dB; Test noise of subclause 6.3.3 with N1=300 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=30 $\mu\text{V}/\sqrt{\text{Hz}}$
2	#2	Forward	Y = Y1 (see note 2); Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
3	#3	Forward	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$
4	#3	Reverse	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
5	#4	Forward	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
6	#4	Reverse	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
7	#5	Forward	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
8	#6	Forward	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
9	#6	Reverse	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
10	#7	Forward	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
11	#7	Reverse	Y = Y1; Test noise of subclause 6.3.3 with N1=100 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$;
12	#8	Forward	Y = Y1; Common mode rejection test of subclause 6.3.5
13	(see note 3)	Forward and Reverse	Y = Y2; Test noise of subclause 6.3.3 with N1=300 $\mu\text{V}/\sqrt{\text{Hz}}$ and N2=30 $\mu\text{V}/\sqrt{\text{Hz}}$; Worst path of tests 1 to 11
14	(see note 3)	(see note 3)	Y = Y3; No added impairment; Worst path of tests 1 to 11; BER < 10 ⁻⁸
15	#2	Forward	Y = Y1; Impulse test as described in subclause 6.3.4
16	As for subclause 6.3.6	Forward	Micro-interruption test as described in subclause 6.3.6
<p>NOTE 1: Test Path = #1 means that the path under test shall be connected with test loop #1 as defined in figure 32. The path(s) not under test shall be connected with a dummy loop, normally loop #1.</p> <p>NOTE 2: Y1 = 22 dB for the one pair system, 27 dB for the two pair system and 31 dB for the three pair system. Y2 = Y1 - 10 dB and Y3 = Y1 + 3 dB.</p> <p>NOTE 3: The tests are carried out on the worst path in the worst direction from tests 1 to 11, with dummy loop(s) for the remaining path(s). If there are no errors, then loop #2 forward for path A is taken as default.</p> <p>NOTE 4: The tests 1 to 15 shall be carried out on all pairs. In the case of fractionally installed HDSL system, the tests shall be carried out only on the installed pair(s).</p>			



NOTE 1: The value for Y (insertion loss in dB at 150 kHz) is to be found in table 20.

NOTE 2: Due to mismatches and bridged taps (BTs) the total DLL attenuation differs from the sum of the attenuation of the parts. Annex A provides theoretical values for the transmission parameters of the above loops.

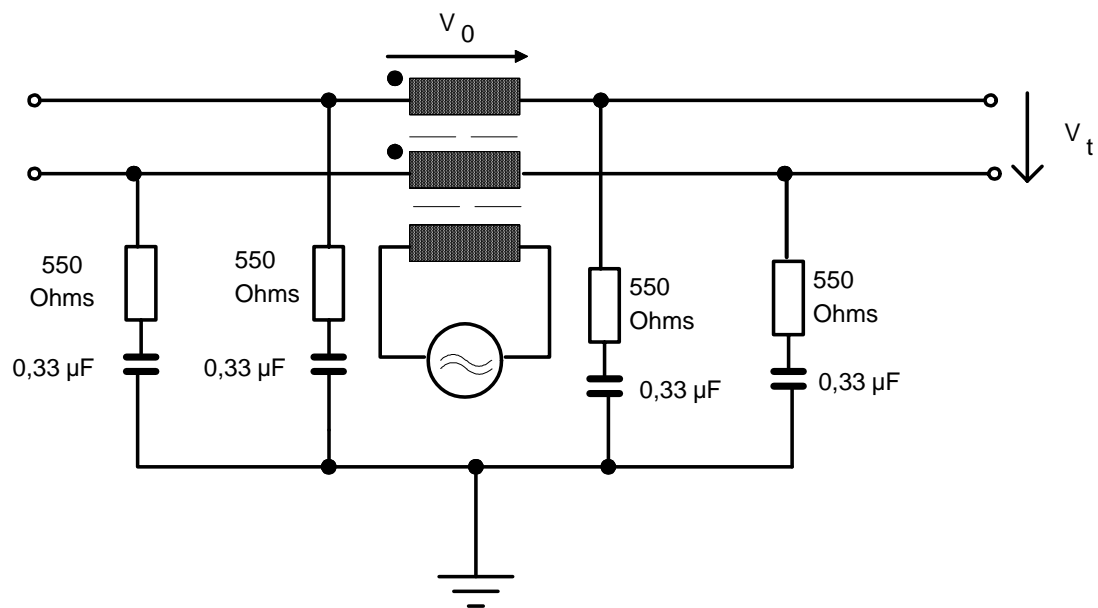
NOTE 3: Attenuation of separate sections is measured with a 135Ω termination.

NOTE 4: These test loops and artificial cable parameters include worst case examples as well as those more typical of a local network. They are chosen to provide the wide range of different echoes and distortions which may occur in European networks.

NOTE 5: The value in brackets is valid for one pair systems only. The reduction is necessary to compensate the higher attenuation of the fixed sections.

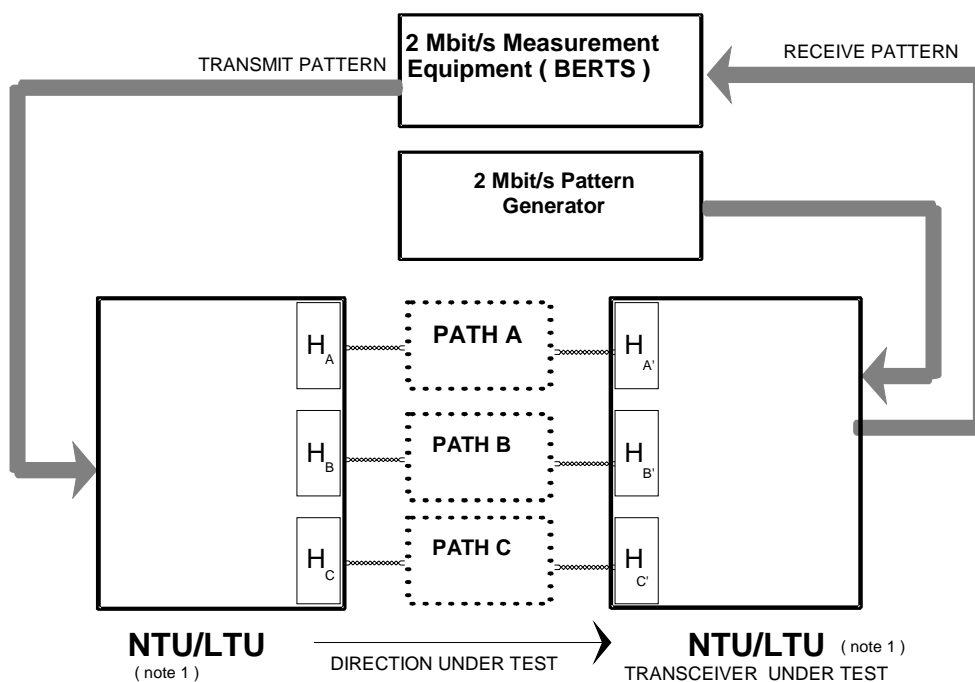
NOTE 6: See figure 33.

Figure 32: DLL physical models for laboratory testing

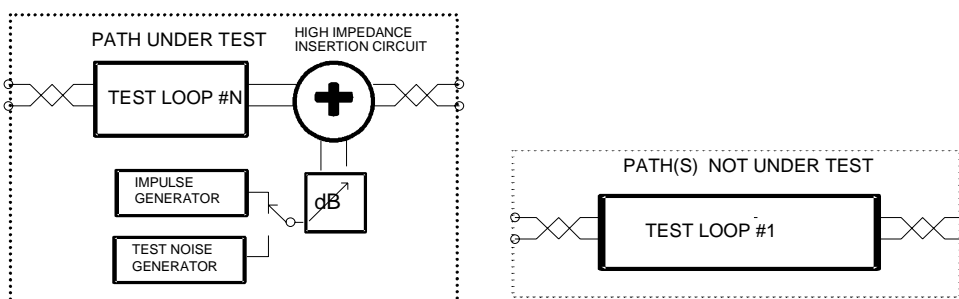


- NOTE 1: The minimum return loss of the terminated test insertion circuit shall be better than the minimum return loss of the system.
- NOTE 2: The minimum LCL (ETS 300 167 [20]) of the test insertion circuit shall be better than 80 dB at 50 Hz, decreasing with 20 dB/decade up to 1 kHz (above 1 kHz transversal voltage is negligible compared with the test noise).

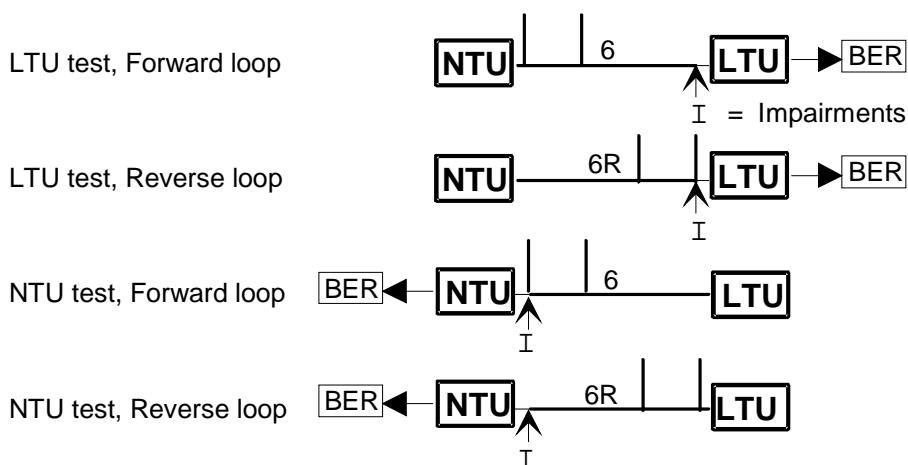
Figure 33: Common mode insertion test circuit



a) Test configuration



b) Details of paths A, B and C



c) Example illustrating test permutations

NOTE 1: Some tests are carried out in both the forward and reverse direction.

NOTE 2: Paths B and C are not used for all HDSL systems or applications.

Figure 34: Configuration for performance tests of an access digital section

6.3.3 Test procedure with shaped noise

6.3.3.1 General

The noise in the local network lines can be represented by an artificial noise source as described below. This artificial noise offers a worst case test condition for intersystem and intrasystem crosstalk for all presently known disturbers.

The characteristics of the noise are as follows:

a) the PSD of the noise is given by the formula below and shown in figure 35:

- N1 between 320 Hz and 1 kHz;
- N2 between 10 kHz and 1,5 MHz;

(The signal falls off between 1 kHz and 10 kHz at 20 dB/decade).

- Noise PSD;
- $\mu\text{V}/\sqrt{\text{Hz}}$.

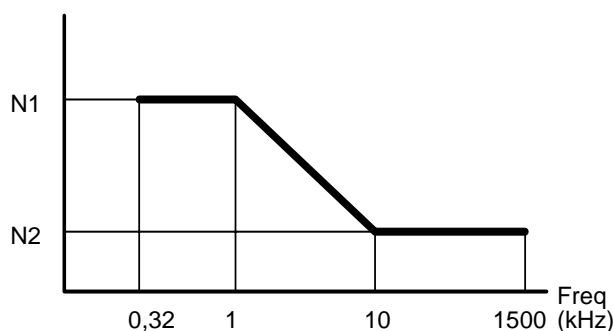


Figure 35: Test noise characteristics

b) the values N1 and N2 differ for "Standard Noise" and "Increased Noise":

- standard noise:
 - $N1 = 100 \mu\text{V}/\sqrt{\text{Hz}}$;
 - $N2 = 10 \mu\text{V}/\sqrt{\text{Hz}}$.
- these levels correspond to a 53 dB NEXT at 150 kHz:
 - increased noise:
 - $N1 = 300 \mu\text{V}/\sqrt{\text{Hz}}$;
 - $N2 = 30 \mu\text{V}/\sqrt{\text{Hz}}$.
 - these levels correspond to a 41 dB NEXT at 150 kHz.
- c) the "Standard Noise" has an rms voltage of 13 mV in the frequency band up to 1,5 MHz when measured with the injection circuitry described below.

6.3.3.2 Generation

The artificial noise shall be constructed using discrete sinewaves with frequencies of $f = n \times 320$ Hz in the range 320 Hz to 1,5 MHz. The level of the individual sinewaves is: $\sqrt{(320 \text{ Hz}) \times n}$ (where $n = N1$ or $N2$ as appropriate).

The phase relationships of the different sinewaves is given as the IEEE Transactions on Circuits and Systems Volume [26]. This will give a signal with a crest factor of about 2,8.

NOTE: Noise with a crest factor of 2,8 is not necessarily representative of crosstalk found in typical access networks where crosstalk has been measured to have a distribution which is close to Gaussian to a crest factor in excess of 4,5. Low crest factor noise does however provide for rapid and repeatable systems tests. This discrepancy is the subject of further study in ETSI TM6.

6.3.3.3 Injection

The injection circuit should have a Thevenin output impedance of at least 4 k Ω . The shaped noise voltage density should be measured at the output of the shunt injection circuit of figure 34, with the test loop replaced by a 67,5 Ω resistor and no terminal equipment connected.

6.3.3.4 Tolerances and calibration

The accuracy of performance margins will depend on the measurement accuracy, in particular the tolerance of the noise source and the loop simulator.

6.3.3.4.1 0 dB level calibration

The noise source may be calibrated so that the averaged summation of the noise PSD over the bandwidth of interest (usually the transmit spectrum of the system under test) conforms with the specification above. This averaged noise power shall be accurate to within ± 1 dB of that specified. If the setting of the noise source is changed by this calibration the new value shall be used as the 0 dB level.

Noise sources from different manufacturers may cause slightly different noise power despite correct calibration and lead to differing measurement results.

6.3.3.4.2 Test loop tolerances

The frequency response of the simulated test loops may deviate from the ideal given in annex A.

This fact may lead to differing measurement results, especially when simulators from different manufacturers are used, and no calibration procedure is known to compensate for this difference.

6.3.4 Test procedure for impulse noise

6.3.4.1 Impulse noise test waveform

The impulse noise waveform $V(t)$ (hereafter called the "test impulse" and also known as the "Cook pulse") is defined as:

- $V(t) = +K|t|^{-3/4}$ ($t > 0$);
- $V(t) = 0$ ($t = 0$);
- $V(t) = -K|t|^{-3/4}$ ($t < 0$).

where t is time given in units of seconds (s) and K is a constant defined numerically in table 21.

A sampled version of the test impulse should be used with samples at $t = (2n-1)T/2$. The sampling rate ($1/T$) should be at least twice the baud rate of the system under test. A minimum number of 8 ksamples (i.e. ± 4 ksamples) is required with an amplitude accuracy of at least 12 bits. It is important to note that there is no sample at $t = 0$. A window on the sampled test impulse is shown in figure 36.

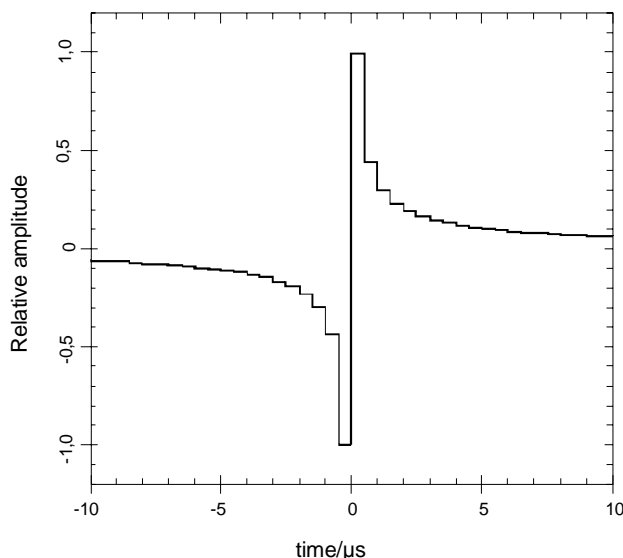


Figure 36: Time domain representation of the test impulse sampled at 2 Msamples/s with 12 bit accuracy

6.3.4.2 Impulse noise test measurement

The test impulse shall be applied to the system under test at a rate of 10 Hz. The test period shall be at least 10 seconds (i.e. > 100 impulses should be applied).

The test configuration shall be as described in subclause 6.3.2, with the BERTS configured to display BER.

The test impulse waveform shall be transformer coupled to the line via a well balanced shunt injection circuit. The injection circuit should have 4 k Ω Thevenin impedance to present minimal loading to the transmission line.

6.3.4.3 Impulse noise test performance requirements

The maximum bit error ratio for the three levels of impulse noise is given in table 21. The peak-to-peak amplitude of the test impulse noise is given in mV (and in dB relative to a reference level of 320 mV) measured at the output of the shunt injection circuit, loaded with a 67,5 Ω resistor.

The minimum value of Y (attenuation of the test pair in dB at 150 kHz) to be used for the impulse noise measurement for various applications is Y1 = 22 dB for the one pair system, Y1 = 27 dB for the two pair system and Y1 = 31 dB for the three pair system.

Table 21: Performance requirements for impulse noise test

Peak-to-peak amplitude (Vpp) of the test impulse when sampled at 2 Msamples/s (see note 1)	K	BER upper limit when measured at the application interface (see note 2)
320 mV (0 dB level)	$1,775 \times 10^{-6}$	$(9/N) \times 10^{-4}$
160 mV (-6 dB level)	$8,875 \times 10^{-7}$	$(12/N) \times 10^{-5}$
80 mV (-12 dB level)	$4,4375 \times 10^{-7}$	$(14/N) \times 10^{-6}$

NOTE 1: The peak-to-peak amplitude will vary with sampling rate and may be easily calculated from the following expression for sampling rates other than 2 Msamples/s. If the sampling rate is 1/T samples/s then $V_{pp} = 2K|T/2|^{-3/4}$.

NOTE 2: N = 1 for a 2 320 kbit/s one pair system, N = 2 for a 1 168 kbit/s two pair system; and N = 3 for a 784 kbit/s three pair system.

6.3.5 Common mode rejection test

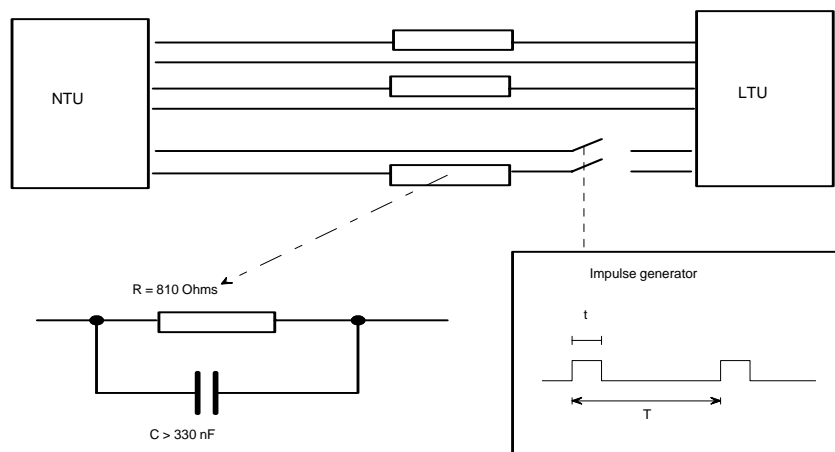
This procedure is intended to test the common mode rejection capability of an implementation. Test Loop 8 shall be used with a common mode triangle signal of 50 Hz with a voltage of 15 V rms for the first harmonic (25,5 V_p). The 21st harmonic (1 050 Hz) shall be 53 dB to 56 dB below the level of the first harmonic. The measured BER shall be less than $(1/N) \times 10^{-7}$, where N is the number of pairs used.

The circuit for common mode insertion is shown in figure 33.

6.3.6 Micro-interruption test

The configuration for micro-interruption susceptibility test is shown in figure 37.

In this arrangement a periodic trigger signal S stimulates a micro-relay device inducing periodic micro-interruptions on one of the pairs forming the transmission link. Using the test arrangement as described in figure 32, each HDSL transceiver shall not be reset by a micro-interruption of at least $t = 10$ ms when stimulated with a signal of period $T = 5$ s.



NOTE: The test shall be carried out for each transceiver pair constituting the transmission link.

Figure 37: Micro-interruption test circuit

7 Application specific requirements

7.1 Application specific requirements for ISDN PRA

7.1.1 Mapping of 2 048 kbit/s to HDSL

As described in subclause 5.4 (Frame structure) the 2 048 kbit/s application data has to be mapped into a core frame with 144 bytes and 500 μ s length. The data at the application interfaces T and V3 (see figures 1 and 2 and ETS 300 233 [1]) contain only 128 bytes per 500 μ s and the unused bytes have to be filled up with 16 stuffing bytes, called Y- and R-bytes and containing all binary ONES, as shown in figure 6b). The use of the stuffing bytes for other purposes e.g. forward error correction is for further study. To achieve total decoupling of the HDSL frame from the core frame and a minimum signal delay the location of time slot 0 within the core frame is arbitrary. This means that, with exception of the location occupied by the Y- and R-stuffing bytes, the first bit of time slot 0 may occur anywhere in the frame. In addition loss of frame alignment at the application interfaces T and V3 does not lead to a resynchronization of the HDSL transceivers, because the core frame is transmitted totally transparent through the HDSL transceiver systems. The bits Z_{m9} to Z_{m48} in the HDSL frame are unused and set to ONE.

7.1.2 Mapping of HDSL maintenance functions to the interface

The application dependant maintenance functions, the definition of the function elements (FE) for the signalling across the application interfaces and the coding of the FE, using the E-, A-, Sa5- and Sa6-bits of time slot 0 in the application frame, are defined in ETS 300 233 [1], clause 9 for the V3 reference point and in ETS 300 011 [7], table 1 for the T reference point. All these functions have to be performed in the interface blocks according to figure 1 by evaluating frame alignment, signal patterns and CRC-4 error detection.

For the detection of the states "Normal operation of the DS", "LOS/LFA at line side of the NT1" and "LOS at the line side of the LT" the maintenance functions "LOS/LFA at line side of the NTU" and "Active indication (INDR)", which are created by the common core at the NTU, respectively "LOS/LFA at LTU line side" and "Active indication (INDC)", which are created by the common core at the LTU, have to be taken into account.

The access digital section shall be considered operational when all the transceiver pairs have indicated completion of the activation procedure (see subclause 5.6) and correct pair identification has been achieved in the core frame, as described in subclause 6.2, and no further failure condition is detected. If one of the transceiver pairs is indicating non-operational condition or incorrect pair identification, the access digital section shall be considered non-operational.

The only maintenance function of this application which has to be achieved by the common core is "Loopback 1 command" as described in table 22.

Table 22: Loopback

Function	Localization	Controlled by	Requested via
Loopback 1	As near as possible to the line	O&M in block M in LTU (see note)	V3 interface
NOTE: When loopback 1 is requested via V3 interface a complete and transparent loopback shall be activated in all HDSL transceivers at the line side of the LTU. These loopbacks are managed by an O&M function inside the functional block M in the LTU.			

7.1.3 Performance

7.1.3.1 Performance specification

The overall performance shall be such that the performance limits given in ITU-T Recommendation G.826 [10] can be met. For the purpose of conformance, an HDSL transmission system is required to meet the specific laboratory performance tests that are defined in subclause 6.3.

7.1.3.2 Signal transfer delay

The one-way signal transfer delay, which is the mean value of the delay time in both directions of transmission between the T and V3 reference points as defined in ETS 300 233 [1], shall not exceed 1 250 μ s, the allocation for a 2B1Q HDSL system shall be as follows:

- LTU $\leq 450 \mu$ s;
- NTU $\leq 450 \mu$ s;
- REG $\leq 200 \mu$ s;
- line $\leq 150 \mu$ s.

7.1.3.3 Clock specification for external interfaces

7.1.3.3.1 NTU clock tolerance

The frequency of the free running NTU clock is 2 048 kHz with a maximum tolerance ± 50 ppm.

7.1.3.3.2 LTU clock tolerance

The frequency of the free running LTU clock is 2 048 kHz with a maximum tolerance ± 50 ppm.

7.1.3.3.3 Jitter specification

The tolerance to input jitter as well as the jitter transfer limitation are defined in terms of amplitude and frequency of sinusoidal input jitter which, when modulating a $2^{15} - 1$ pseudo-random bit sequence within time slots 1 to 31 of the bit stream, should not cause bit errors in the transmission system or jitter at the relevant output which is in excess of limits defined below. This test method is used for convenience of testing and is not, in itself, intended to be representative of the type of jitter to be found in practical applications.

The tolerable input jitter is given in figure 38 with the values of table 23. The output jitter limits given in table 24 shall be met when applying the tolerable jitter to the relevant input, where B1 is measured with a bandpass having a upper cut-off frequency of f_4 and a lower cut-off frequency of f_1 , whilst B2 is measured with the same high cut-off frequency but with a low cut-off frequency increased to f_3 .

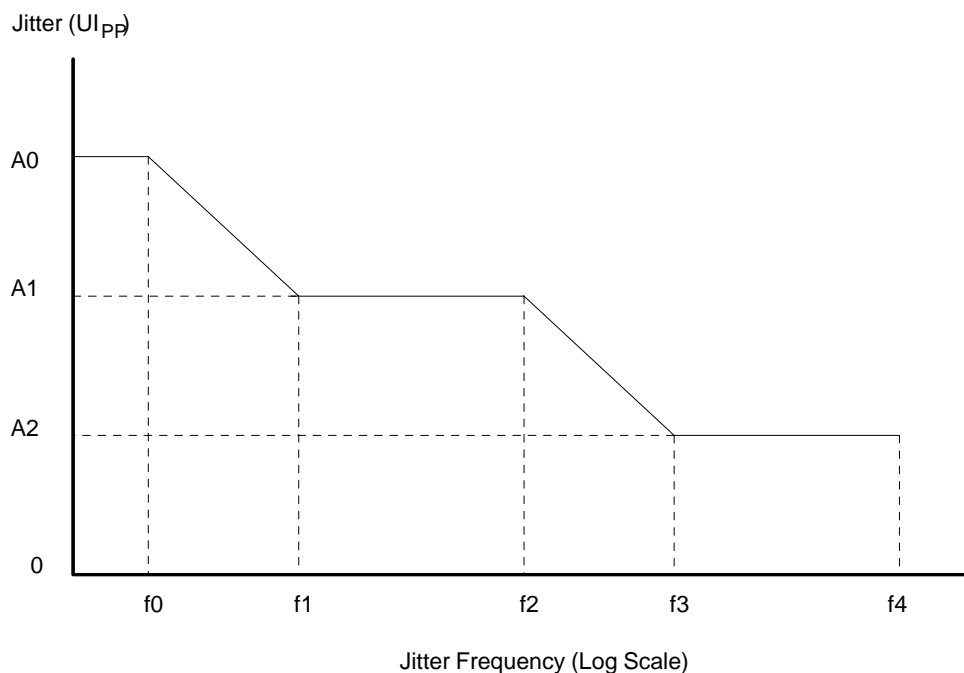


Figure 38: Lower limit of maximum tolerable input jitter

Table 23: Parameter values for input jitter tolerance at inputs

Interface	Parameter:	Peak-to-peak amplitude			Frequency				
		A0	A1	A2	f0	f1	f2	f3	f4
At T input	Value	-	1,1	0,11	-	-	40	0,4	100
At V3 input	Value	20,5	0,9	0,18	12	20	3 600	18	100
	Units	U _{lpp}	U _{lpp}	U _{lpp}	μ Hz	Hz	Hz	kHz	kHz
NOTE 1: U _{lpp} = Unit Interval peak-peak. 1 U _{lpp} = 1/2 048 kHz = 488 ns for the ISDN PRA application.									
NOTE 2: The values for the T-interface input are taken from ETS 300 011 [7] as required by ETS 300 233 [1].									
NOTE 3: The values for the V3-interface input are taken from ETS 300 011 [7], but reduced by 10 % margin for jitter accumulation in the HDSL transmission system.									

Table 24: Maximum permitted values of output jitter

Interface	Parameter	Maximum permissible jitter		Measurement bandpass parameters (high pass part has first order slope)		
		B1; (f1-f4)	B2; (f3-f4)	f1	f3	f4
At T output	Value	1,0	0,2	20	18 000	100
At V3 output	Value	1,2	0,2	20	700	100
	Units	UIpp	UIpp	Hz	Hz	kHz

NOTE 1: The values for the output at T-interface are taken from ETS 300 011 [7].
NOTE 2: The values for the output at V3-interface are taken from ETS 300 011 [7], but increased by 10 % for jitter accumulation in the HDSL transmission system in lower frequency area and based on high Q transmission network following.

7.1.3.3.4 Wander specification

The maximum wander that may be experienced at the output of an HDSL system, expressed in MTIE, shall not exceed the values given in table 25. The resultant overall specification is illustrated in figure 39.

The timing reference for the MTIE measurement shall be the same as used as a reference for the 2,048 Mbit/s pseudo random test sequence generator. The pseudo random test sequence shall be $2^{15}-1$ according to ITU-T Recommendation O.151 [12].

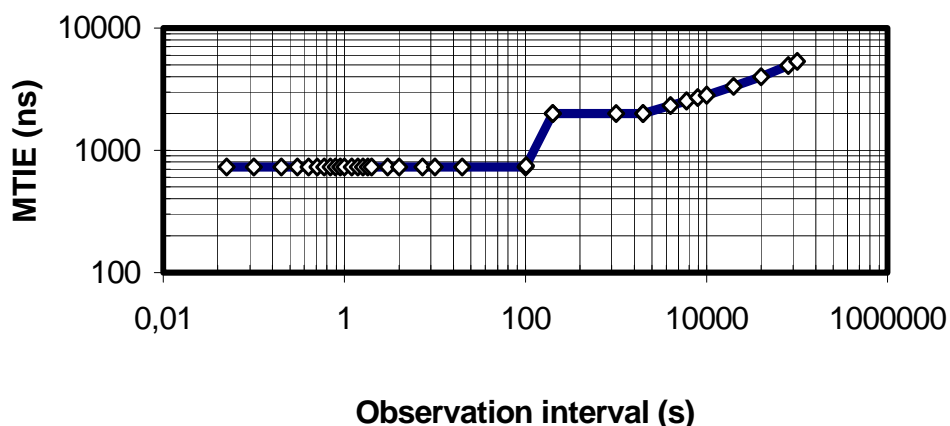
NOTE 1: Transmission systems designed according to editions 1 to 3 of ETR 152 may cause higher values for wander and will therefore not be suited for applications that are sensitive to wander.

NOTE 2: In order to determine the maximum wander amplitude produced by a HDSL system, it is required to vary the network clock frequency at the input of the system in the range of ± 50 ppm. It is recommended to use a clock offset resolution of ≤ 1 ppm to measure the wander accurately.

This requirement shall also be met in the presence of a regenerator.

Table 25: maximum permitted values of output wander

MTIE	Observation interval
732 ns	$0,05 < \tau \leq 100$ s
$13 \tau - 568$ ns	$100 < \tau \leq 200$ s
2 000 ns	$200 < \tau \leq 2\ 000$ s
$433 \tau ^{0,2} + 0,01 \tau $ ns	$\tau > 2\ 000$ s

**Figure 39: Maximum permitted values of output wander expressed in MTIE**

7.1.3.4 Laboratory performance measurement

It is assumed that the performance can be evaluated at the application interface. The test arrangement and procedures of subclause 6.3 shall be used.

7.2 Application specific requirements for the 2 048 kbit/s digital unstructured leased line (D2048U)

7.2.1 Application interfaces

7.2.1.1 Application interface at the customer side

The application interface at the customer side shall be according to ETS 300 246 [2] and ETS 300 247 [3], subclause 7.1.7.2. ETS 300 246 [2] may be replaced by ETS 300 418 [4] in future.

7.2.1.2 Application interface at the network side

The application interface at the network side is a 2 048 kbit/s interface according to ETS 300 166 [19].

7.2.2 Mapping of the D2048U signal to HDSL

As described in subclause 5.4 the application data having a nominal bit rate of 2 048 kbit/s with maximum tolerance of ± 50 ppm shall be mapped bit sequence independently into a core frame with 144 bytes and 500 μ s length. The data at the application interface at the customer side contain only 128 bytes per 500 μ s. The unused bytes shall be filled up with 16 stuffing bytes called Y- and R-bytes and containing all binary ONEs, as shown in figure 6b). The use of the stuffing bytes for other purposes e.g. forward error correction is for further study.

The bits Z_{m9} to Z_{m48} in the HDSL frame are unused and shall be set to ONE.

7.2.3 Mapping of HDSL maintenance functions to the interface

The access digital section shall be considered operational when all of the transceiver pairs have indicated completion of the activation procedure (see subclause 5.6), correct pair identification has been achieved in the core frame, as described in subclause 6.2, and no further failure condition is detected. If one of the transceiver pairs is indicating non-operational condition or incorrect pair identification, the access digital section shall be considered non-operational.

The fact that the D2048U signal is unstructured makes it impossible for the HDSL core to map any operation and maintenance information into or out of the payload because the HDSL system does not have any information about the contents or the internal structure of the transmitted data.

The only information the core can get is "LOS at the application interface of LTU" and "LOS at the application interface of NTU". When LOS at the application interface of NTU or LTU is detected, an "All ONEs" signal shall be transmitted to the far end of the HDSL system. At the same time bit 15 of the HDSL frame ("losd") shall be set to ZERO as shown in table 26.

Table 26: LOS at the application interface of LTU and NTU

Leased line input condition	Action
LOS at the application interface of LTU	losd = 0 in HOH (LTU/NTU)
LOS at the application interface of NTU	losd = 0 in HOH (NTU/LTU)

The mapping of LOS/LFA at the line side of LTU, NTU, and both sides of REG to the application interface is shown in table 27.

Table 27: Mapping of maintenance functions to the application interfaces

Condition on one (or more) pair(s)	Message towards the application interface of	
	NTU	LTU
LOS/LFA at LTU line side	(see note)	AIS
LOS/LFA at NTU line side	(see note)	AIS
LOS/LFA at REG-R	(see note)	AIS
LOS/LFA at REG-C	(see note)	AIS
NOTE: As long as the HDSL system is not in the full operating state, i.e. not all of the HDSL transceivers are in the Active-Rx/Tx state, the signal towards the application interface of the NTU is not defined.		

7.2.4 Performance

7.2.4.1 Performance specification

The overall performance shall be such that the performance limits defined in ITU-T Recommendation G.826 [10] can be met.

7.2.4.2 Signal transfer delay

The one-way signal transfer delay between the application interfaces shall not exceed 1 250 μ s. This shall be calculated as the mean delay for both directions. The allocation for a 2B1Q HDSL system shall be as follows:

- LTU $\leq 450 \mu$ s;
- NTU $\leq 450 \mu$ s;
- REG $\leq 200 \mu$ s;
- line $\leq 150 \mu$ s.

7.2.4.3 Clock specification for external interfaces

7.2.4.3.1 NTU clock tolerance

The frequency of the free running NTU clock shall be 2 048 kHz with a maximum tolerance of ± 50 ppm.

7.2.4.3.2 LTU clock tolerance

The frequency of the free running LTU clock shall be 2 048 kHz with a maximum tolerance of ± 50 ppm.

7.2.4.3.3 Jitter specification

The tolerance to input jitter as well as the jitter transfer limitation are defined in terms of the amplitude and frequency of sinusoidal input jitter which, when modulating a $2^{15} - 1$ pseudo random test sequence of the 2 048 kbit/s bit stream at the nominal rate and with tolerances of +50 ppm and -50 ppm, shall not cause bit errors in the transmission system or jitter at the relevant output in excess of the limits defined below. This test method is used for convenience of testing and is not, in itself, intended to be representative of the type of jitter to be found in practice.

The tolerable input jitter is given in figure 38 (subclause 7.1.3.3.3) with the values of table 28. The output jitter limits given in table 29 shall be met when applying the tolerable jitter to the relevant input.

Table 28: Parameter values for input jitter tolerance at inputs

Application interface	Parameter:	Peak-to-peak amplitude			Frequency				
		A0	A1	A2	f0	f1	f2	f3	f4
at NTU (input)	Value	-	1,1	0,11	-	-	4	0,04	100
at LTU (input)	Value	-	1,35	0,18	-	20	2 400	18	100
	Units	-	U _{Ipp}	U _{Ipp}	-	Hz	Hz	kHz	kHz
NOTE 1: U _{Ipp} = Unit Interval peak-peak. 1 U _{Ipp} = 1/2 048 kHz = 488 ns for the D2048U application.									
NOTE 2: The values for the NTU input are taken from ETS 300 247 [3].									
NOTE 3: The values for the LTU input are taken from ITU-T Recommendation G.823 [9] but reduced by 10 % margin for jitter accumulation in the HDSL transmission system.									

Table 29: Maximum permitted values of output jitter

Application Interface	Parameter	Maximum permissible jitter		Measurement bandpass parameters (high pass part has first order slope)		
		B1; (f1-f4)	B2; (f3-f4)	f1	f3	f4
at NTU output	Value	1,5	0,2	20	18 000	100
at LTU output	Value	0,3	0,15	20	700	100
	Units	U _{Ipp}	U _{Ipp}	Hz	Hz	kHz
NOTE 1: The values for the NTU output are taken from ETS 300 247 [3].						
NOTE 2: The values for the LTU output are based on the input at NTU, but increased for jitter accumulation in the HDSL transmission system in the lower frequency area and based on high Q transmission network following.						

7.2.4.4 Laboratory performance measurements

It is assumed that the performance can be evaluated at the application interface. The test arrangement and procedures of subclause 6.3 shall be used.

7.3 Application specific requirements for the 2 048 kbit/s digital structured leased line (D2048S)

7.3.1 Application interfaces

7.3.1.1 Application interface at the customer side

The application interface at the customer side shall be according to ETS 300 418 [4] and ETS 300 419 [5], subclause 5.1.7.2.

7.3.1.2 Application interface at the network side

The application interface at the network side is a 2 048 kbit/s interface according to ETS 300 166 [19]. If the structure information according ETS 300 419 [5] is handled in the NTU and/or LTU then the relevant function shall be implemented as defined in ETS 300 419 [5] and ETS 300 167 [20].

7.3.2 Mapping of the D2048S signal to HDSL

As described in subclause 5.4 the application data having a nominal bit rate of 2 048 kbit/s with maximum tolerance of ± 50 ppm shall be mapped bit sequence independently into a core frame with 144 bytes and 500 μ s length. The data at the application interface at the customer side contain only 128 bytes per 500 μ s. The unused bytes shall be filled up with 16 stuffing bytes called Y- and R-bytes and containing all binary ONES, as shown in figure 6b). The use of the stuffing bytes for other purposes e.g. forward error correction is for further study. The bits Z_{m9} to Z_{m48} in the HDSL frame are unused and shall be set to ONE.

7.3.3 Mapping of HDSL maintenance functions to the interface

The access digital section shall be considered operational when all of the transceiver pairs have indicated completion of the activation procedure (see subclause 5.6), correct pair identification has been achieved in the core frame, as described in subclause 6.2, and no further failure condition is detected. If one of the transceiver pairs is indicating non-operational condition or incorrect pair identification, the access digital section shall be considered non-operational.

The mapping of LOS/LFA at the line side of LTU, NTU, and both sides of the REG to the application interface is shown in table 30.

Table 30: Mapping of maintenance functions to the application interfaces

Condition on one (or more) pair(s)	Message towards the application interface of	
	NTU	LTU
LOS/LFA at LTU line side	(see note 1)	(see note 2)
LOS/LFA at NTU line side	(see note 1)	(see note 2)
LOS/LFA at REG-R	(see note 1)	(see note 2)
LOS/LFA at REG-C	(see note 1)	(see note 2)

NOTE 1: As long as the HDSL system is not in the full operating state, i.e. not all of the HDSL transceivers are in the Active-Rx/Tx state, the signal towards the application interface of the NTU is not defined.
NOTE 2: The message sent towards the application interface of the LTU shall either be AIS or AUXP dependent on the requirement of the network operator.

Table 31 shows how to achieve a complete and transparent loopback in the LTU.

Table 31: Loopback in the LTU

Function	Localization	Controlled by	Requested via
Loopback 1	as close as possible to the line	O&M in block M in LTU	the application interface of LTU

NOTE 1: The use of this loopback is network dependent.
NOTE 2: When the loopback 1 is requested via the application interface of the LTU a complete and transparent loopback shall be activated in all HDSL transceivers on the line side of the LTU. These loopbacks are managed by an O&M function inside the functional block M in the LTU.

7.3.4 Performance

7.3.4.1 Performance specification

The overall performance shall be such that the performance limits defined in ITU-T Recommendation G.826 [10] can be met.

7.3.4.2 Signal transfer delay

The one-way signal transfer delay between the application interfaces shall not exceed 1 250 μ s. This shall be calculated as the mean delay for both directions. The allocation for a 2B1Q HDSL system shall be as follows:

- LTU \leq 450 μ s;
- NTU \leq 450 μ s;
- REG \leq 200 μ s;
- line \leq 150 μ s.

7.3.4.3 Clock specification for external interfaces

7.3.4.3.1 NTU clock tolerance

The frequency of the free running NTU clock shall be 2 048 kHz with a maximum tolerance of \pm 50 ppm.

7.3.4.3.2 LTU clock tolerance

The frequency of the free running LTU clock shall be 2 048 kHz with a maximum tolerance of ± 50 ppm.

7.3.4.3.3 Jitter specification

The tolerance to input jitter as well as the jitter transfer limitation are defined in terms of the amplitude and frequency of sinusoidal input jitter which, when modulating a $2^{15} - 1$ pseudo random test sequence within time slots 1 to 31 of the 2 048 kbit/s bit stream at the nominal bit rate and with tolerances of +50 ppm and -50 ppm, shall not cause bit errors in the transmission system or jitter at the relevant output in excess of the limits defined below. This test method is used for convenience of testing and is not, in itself, intended to be representative of the type of jitter to be found in practice.

The tolerable input jitter is given in figure 38 (see subclause 7.1.3.3.3) with the values of table 32. The output jitter limits given in table 33 shall be met when applying the tolerable jitter to the relevant input.

Table 32: Parameter values for input jitter tolerance at inputs

Application interface	Parameter:	Peak-to-peak amplitude			Frequency				
		A0	A1	A2	f0	f1	f2	f3	f4
at NTU (input)	Value	-	1,1	0,11	-	-	4	0,04	100
at LTU (input)	Value	-	1,35	0,18	-	20	2 400	18	100
	Units	-	Ulpp	Ulpp	-	Hz	Hz	kHz	kHz

NOTE 1: Ulpp = Unit Interval peak-peak. 1 Ulpp = 1/2 048 kHz = 488 ns for the D2048S application.
 NOTE 2: The values for the NTU input are taken from ETS 300 419 [5].
 NOTE 3: The values for the LTU input are taken from ITU-T Recommendation G.823 [9] but reduced by 10 % margin for jitter accumulation in the HDSL transmission system.

Table 33: Maximum permitted values of output jitter

Application Interface	Parameter	Maximum permissible jitter		Measurement bandpass parameters (high pass part has first order slope)		
		B1; (f1-f4)	B2; (f3-f4)	f1	f3	f4
at NTU output	Value	1,5	0,2	20	18 000	100
at LTU output	Value	0,3	0,15	20	700	100
	Units	Ulpp	Ulpp	Hz	Hz	kHz

NOTE 1: The values for the NTU output are taken from ETS 300 419 [5].
 NOTE 2: The values for the LTU output are based on the input at NTU, but increased for jitter accumulation in the HDSL transmission system in the lower frequency area and based on high Q transmission network following.

7.3.4.4 Laboratory performance measurements

It is assumed that the performance can be evaluated at the application interface, avoiding the need for test access to the individual data channels. The test arrangement and procedures of subclause 6.3 shall be used.

7.4 Application specific requirements for fractional installation

7.4.1 Mapping of fractional services to HDSL

7.4.1.1 Overview of mapping procedure

The fractional installation application interface is based on ETS 300 167 [20].

The fractional installation application of HDSL provides reduced access capability for the case where not all HDSL transceivers are equipped. The core frame of 144 bytes and 500 μ s length, described in subclause 5.4 (frame structure) is mapped onto one, two or three parallel HDSL frames, depending on the bit rate (784 kbit/s or 1 168 kbit/s) and number of the equipped HDSL transceivers. If mapping option according to figure 6c) is implemented, in which the HDSL core frame is synchronized to the application frame, with TS 0 being inserted in the first payload position in the HDSL frame, then the possibility exists for transparent transmission of a fractionally filled application frame, and also for partial operation of the system in the case of failure of transmission on one or more of the pairs.

An external data interface (e.g. ISO 2110 [21]) and pre-processing functions may accept data at an aggregate bit rate of $(n \times 64)$ kbit/s and map it into the 2 048 kbit/s application interface frame. An optional time slot interchange block allows the implementation of complex applications such as point-to-multipoint operation or the transmission of contiguous blocks of channels on each HDSL pair. (These functions are outside the scope of the present document).

The mapping of the core frame into the HDSL frame follows in the normal fashion, with the exception that not all the pairs need be equipped. This mapping process is illustrated in figures 40 and 41.

With this mapping partial operation of a fractionally installed three pair system is possible.

7.4.1.2 Details of mapping of the application interface from the HDSL core frame

The mapping process for 784 kbit/s transceiver is shown in figures 42 and 43, and for 1 168 kbit/s transceivers in figure 44. The application interface frame described in ETS 300 167 [20] is synchronously mapped byte-wise into the core frame, with the application frame occupying a defined position within the HDSL frame. Unused bytes have an AIS signal (all-ONES) inserted.

7.4.1.3 Details of HDSL core frame mapping into HDSL frame

The mapping from core frame to HDSL transmission frame takes place in exactly the same way as for the other applications, as can be seen from figures 42, 43 and 44. The pre-processing involved in mapping the application into the core frame is responsible for defining the final mapping onto the HDSL pairs. No additional processing is required in the core-to-HDSL mapping. The pairs carrying only AIS signal do not need to be equipped, the AIS being reinserted at the receiver. The CRC-4 checking in the application frame thus appears transparent through the system, that is, from the point of view of the CRC-4 checking the system behaves as if there were error free transmission on those channels (containing AIS) which were terminated at the transmitter and reintroduced at the receiver.

7.4.1.4 Optional external mappings into the application frame

Additional mappings from external data interfaces into the application frame may be implemented externally in order to facilitate applications such as point-to-multipoint operation, multiple $(n \times 64)$ kbit/s data streams, creation of high and low priority data streams (in the case of partial operation) and the mapping of contiguous blocks of time slots onto a specific HDSL pair. The definition of such mappings is, however, outside the scope of the present document.

7.4.2 Mapping of HDSL maintenance functions to the interface

A fractionally installed system shall be considered fully operational when all the installed transceiver pairs have indicated completion of the activation procedure as described in subclause 5.6, correct pair identification has been achieved in the core frame, as described in subclause 6.2, and no further failure condition is detected. If one of the installed transceiver pairs is indicating non-operational condition or incorrect pair identification, the fractionally installed system shall be considered non-operational.

Table 34: Mapping of maintenance functions to the application interface

Condition on one (or more) pair(s)	Message towards the application interface of	
	NTU	LTU
LOS/LFA at LTU line side	(see note 1)	(see note 2)
LOS/LFA at NTU line side	(see note 1)	(see note 2)
LOS/LFA at REG-R	(see note 1)	(see note 2)
LOS/LFA at REG-C	(see note 1)	(see note 2)
NOTE 1: As long as the selected transceiver(s) is not in the full operating state, the signal towards the application interface of the NTU is not defined.		
NOTE 2: The message sent towards the application interface of the LTU shall either be AIS or AUXP dependent on the requirements of the network operator.		

The mapping of LOS/LFA at the line side of LTU, NTU and both sides of the REG to the application interface is shown in table 34, and table 35 shows how a complete and transparent loopback is achieved.

Table 35: Loopback in LTU

Function	Localization	Controlled by	Requested via
Loopback 1	as close as possible to the line	O&M in block M in LTU (see note)	the application interface of LTU
NOTE: When the loopback 1 is requested via the application interface of the LTU a complete and transparent loopback shall be activated in all HDSL transceivers on the line side of the LTU. These loopbacks are managed by an O&M function inside the functional block M in LTU.			

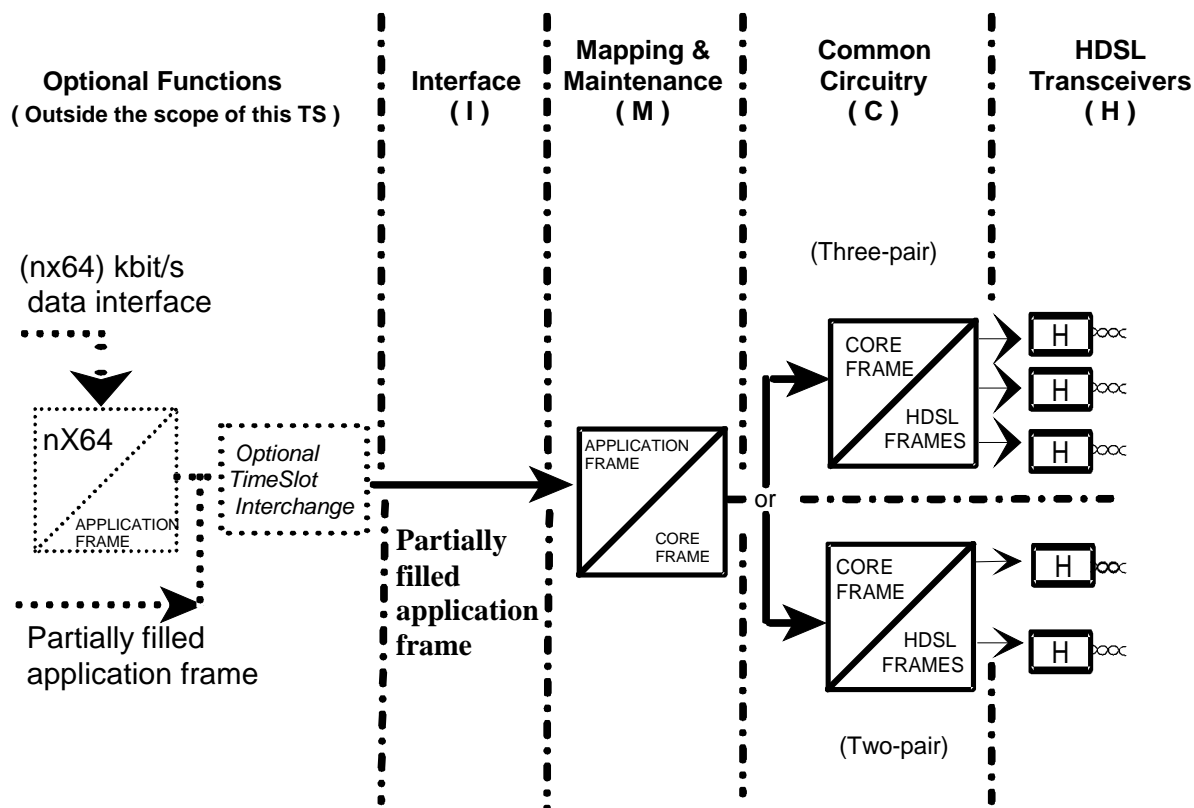
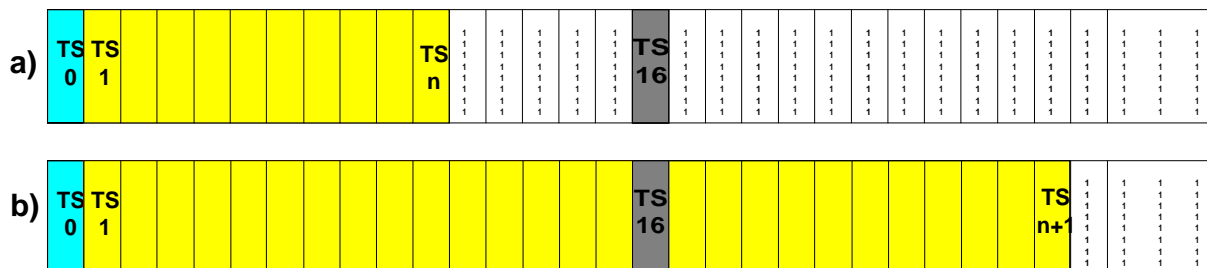


Figure 40: Mapping process for fractional installation



Time slots of the 2 048 kbit/s application frame are filled as follows:

- TS0 is filled according to ETS 300 167 [20];
- TS16 is reserved for the accommodation, if required, of a 64 kbit/s signalling channel:
 - if $2 \leq n \leq 15$, TS1 to TSn are filled with $n \times 64$ kbit/s data (a);
 - if $15 < n \leq 30$, TS1 to TS15 and TS17 to TS(n+1) are filled with $n \times 64$ kbit/s data (b).
- Remaining time slots are filled with all-ONEs (AIS) data.

Figure 41: Illustration of the fractional installation mapping into 2 048 kbit/s application frame

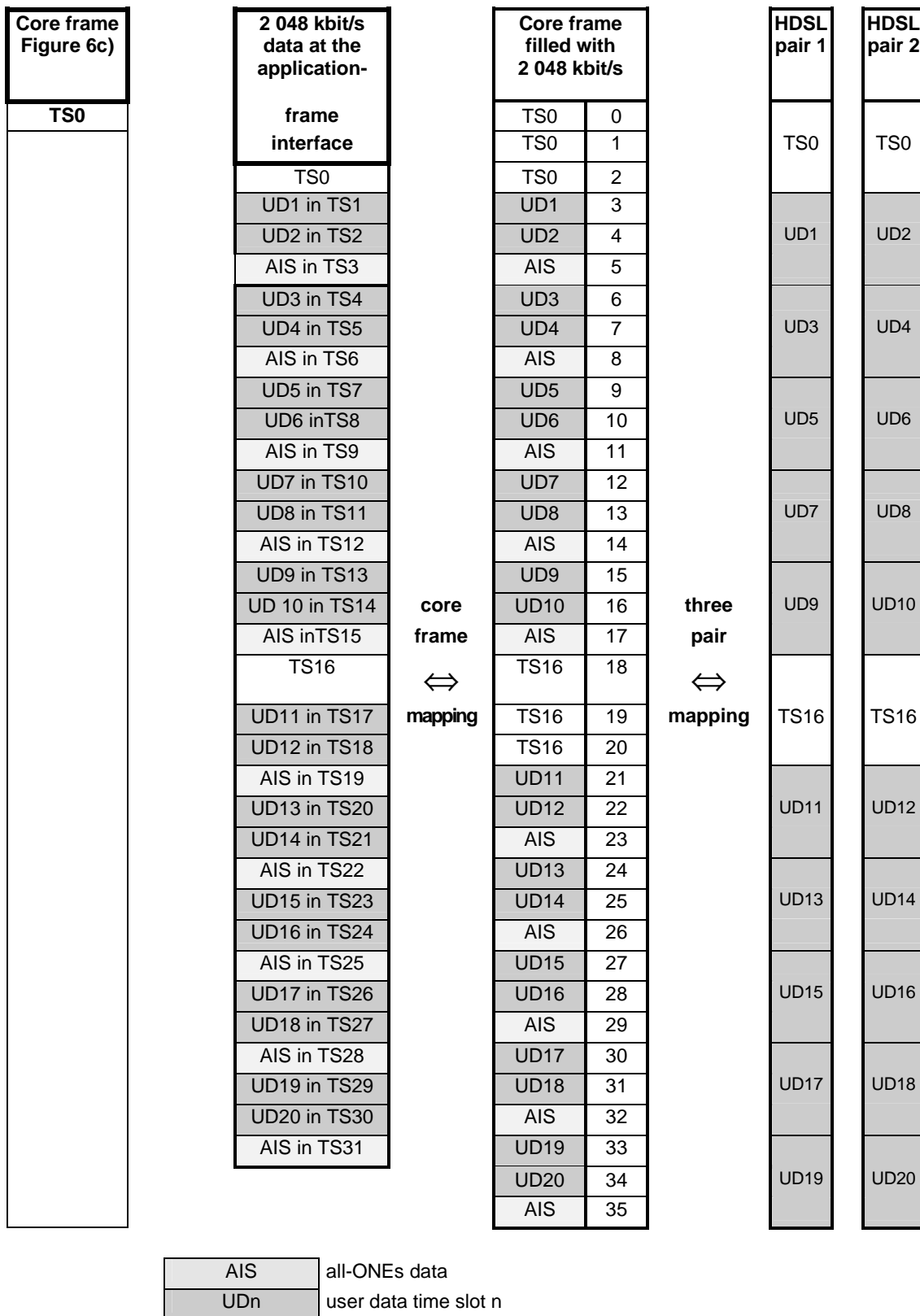


Figure 42: Mapping procedure for fractional installation of two out of three pairs of a three pair 784 kbit/s HDSL system

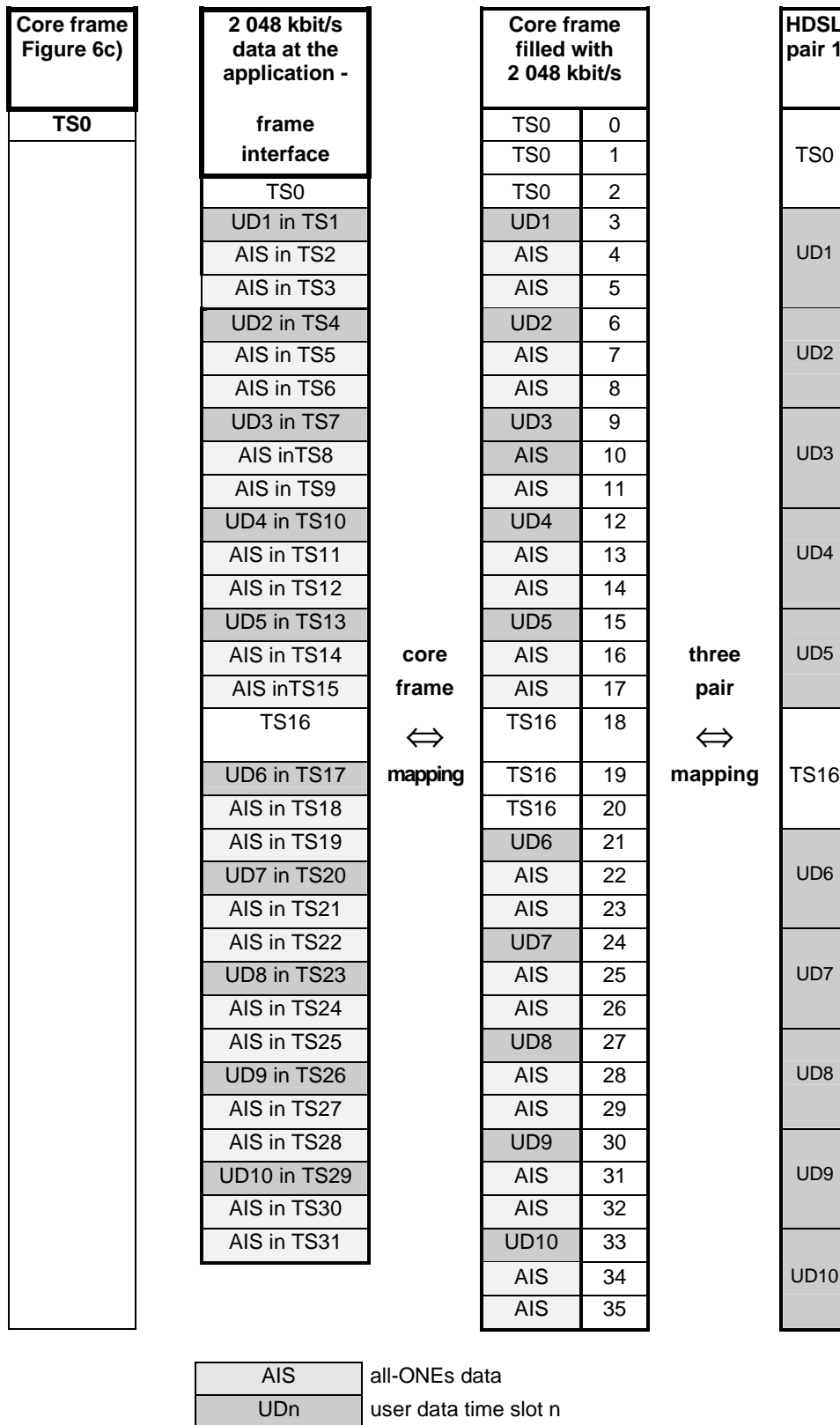


Figure 43: Mapping procedure for fractional installation of one out of three pairs of a three pair 784 kbit/s HDSL system

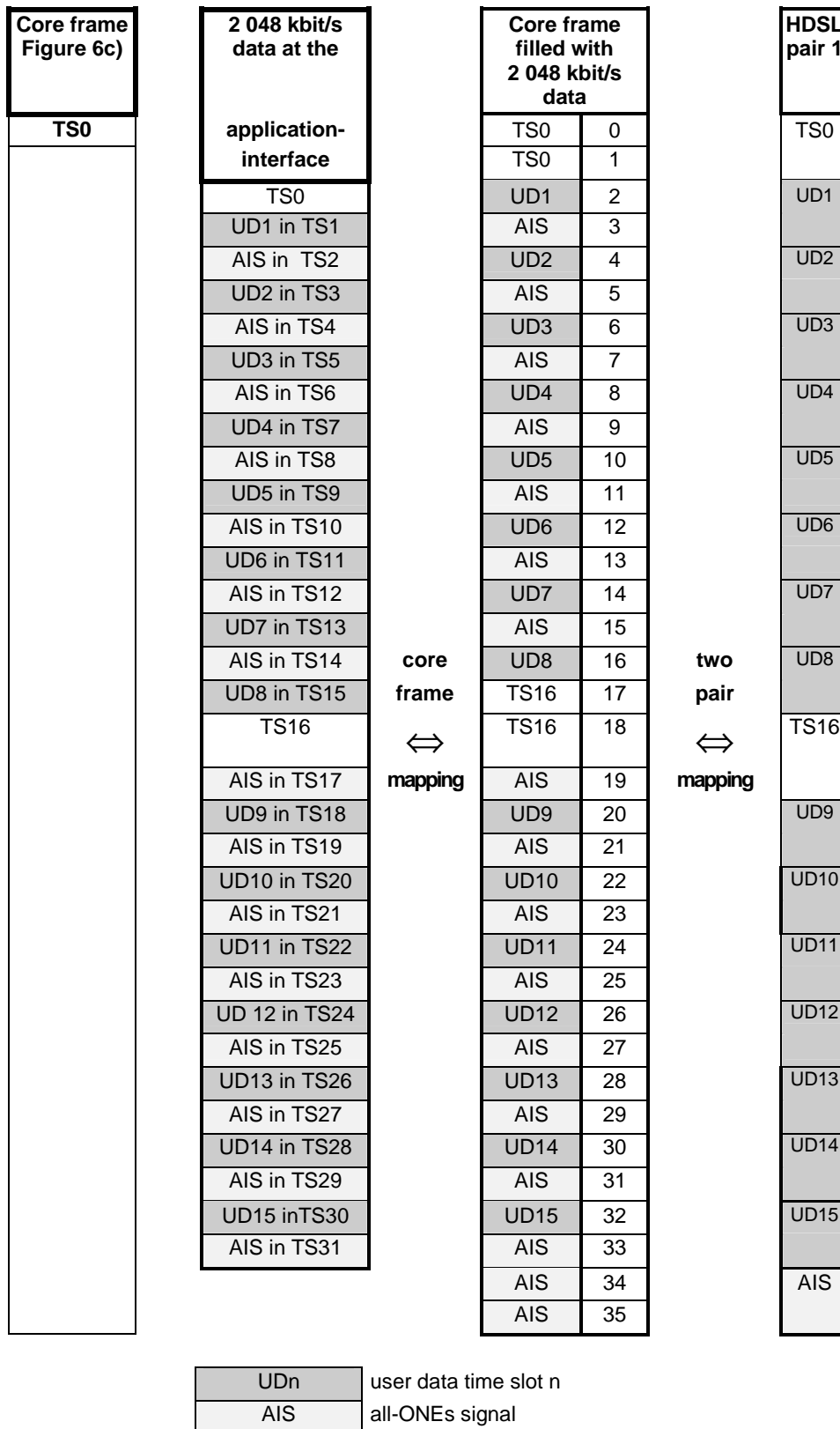


Figure 44: Fractional installation mapping onto one pair of a two pair system

7.4.3 Performance

7.4.3.1 Performance specification

The overall performance shall be such that the performance limits given in ITU-T Recommendation G.826 [10] can be met. For the purpose of conformance, an HDSL transmission system is required to meet the specific laboratory performance tests that are defined in the following subclauses.

The performance requirements have been specified so that the HDSL transceivers are tolerant to near-end crosstalk (NEXT), impulsive noise and shaped noise, and not optimized for only one operating condition.

The one way signal transfer delay shall be as defined in subclause 7.1.3.2.

7.4.3.2 Clock specification for external interfaces

7.4.3.2.1 Clock tolerance

The clock tolerance shall be as defined in subclauses 7.1.3.3.1 and 7.1.3.3.2.

7.4.3.2.2 Jitter and wander specifications

The jitter specifications of subclause 7.1.3.3.3 shall be applied to the application interface. The specification of jitter at the output of the external data interface is outside the scope of the present document.

7.4.3.3 Laboratory performance measurements

It is assumed that performance can be evaluated at the application interface, avoiding the need for test access to the individual data channels. The test arrangement and procedures of subclause 6.3 shall be used.

7.5 Application specific requirements for partial operation

7.5.1 Mapping of the application frame for partial operation application

As described in subclause 5.4 (frame structure) the 2 048 kbit/s application data is mapped into a core frame with 144 bytes and 500 μ s length. If the mapping option figure 6c) is implemented, then the possibility exists for partial operation of the system in the case of failure of transmission on one or more of the pairs. This mapping is shown in more detail for the case of partial operation in figure 45 (three pair system) and figure 46 (two pair system). These mappings allow ISDN PRA or ETS 300 167 [20] framed operation in normal operation, but permit reduced capacity operation if one or two pairs fail. It is also possible to have partial operation in the case of partial failure of a fractionally installed three pair system.

In the case of partial operation, the output mapping for the non-corrupted channels shall be unchanged, and missing channel time slots shall be filled with all-ONES data (AIS). In addition, the necessary modification of the embedded maintenance functions (TS0 and TS16) shall be carried out in accordance with subclause 7.5.2.

7.5.2 Mapping of HDSL maintenance functions to the interface

The HDSL embedded operations channel (eoc) is transmitted in parallel over all the HDSL pairs (subclause 5.5.2). Thus, in the event of a failure of one of the HDSL pairs, all the functions of the eoc will still be available on the remaining pairs. In the event of a pair failure, there will be some means of communicating the failure to the HDSL mapping function so that the mapping function may take the appropriate actions, such as time slot reallocation (if required) and insertion of AIS into the non-supportable time slots. The mapping and maintenance block shall continually monitor the status of all pairs and in particular, that of any failed pair(s). When a failure condition has been cleared, the M block may then reallocate the previously unsupportable time slots to the reactivated pair.

The access digital section shall be considered operational, when all of the transceiver pairs have indicated completion of the activation procedure, correct pair identification has been achieved in the core frame, as described in subclause 5.6, and no further failure condition is detected. If one of the transceiver pairs is indicating non-operational condition, or incorrect pair identification, the access digital section shall be considered non-operational. When during operation a transceiver becomes inoperable, the transport in the other loops is still operating. The mapping of LOS/LFA at the line side of LTU, NTU and both sides of the REG to the application interface is shown in table 36, and table 37 shows how a complete transparent loopback is achieved.

Table 36: Mapping of maintenance functions to the application interface

Condition on one (or more) pair(s)	Message towards the application interface of	
	NTU	LTU
LOS/LFA at LTU line side	(see note)	(see note)
LOS/LFA at NTU line side	(see note)	(see note)
LOS/LFA at REG-R	(see note)	(see note)
LOS/LFA at REG-C	(see note)	(see note)

NOTE: AIS in the time slots of the inoperable loop(s).

Table 37: Loopback in the LTU

Function	Localization	Controlled by	Requested via
Loopback 1	as close as possible to the line	O&M in block M in LTU (see note)	the application interface of LTU

NOTE: When the loopback 1 is requested via the application interface of the LTU a complete and transparent loopback shall be activated in all HDSL transceivers on the line side of the LTU. These loopbacks are managed by an O&M function inside the functional block M in LTU.

7.5.3 Performance

The overall performance shall be such that the performance limits given in ITU-T Recommendation G.826 [10] can be met, for either the complete transmission system, or the individual data channels supported during partial operation.

The performance specification for the ISDN PRA application as described in subclause 7.1.3 shall be applied. It is not necessary to test the performance for partial operation separately.

The partial operation functionality shall be tested by interrupting each loop in turn, and confirming that the system continues to operate correctly in the partial operation mode, and that the performance of the remaining channels is acceptable.

7.5.4 Remote power feeding

In HDSL systems which rely solely on remote power feeding the NTU may not work in the event of a pair failure due to the fact that the NTU may consume more power than can be supplied over a single pair, especially where loops with high DC resistances are involved. For such systems, locally powered NTUs may be appropriate.

7.5.5 Partial failure criteria

The criteria for detection of partial failure should not be based solely on LOSW (loss of sync word) because this could be generated by a trivial event (e.g. noise event) and should not be interpreted as a line failure.

Activation flags should be used to indicate pair(s) failure (e.g. LOS, LOST) to the mapping and maintenance functional block.

7.5.6 Action following partial failure

The transceiver which has flagged a failure to the mapping and maintenance functional block shall automatically initiate start-up procedures independently of the other transceivers in the system and continue to do so until it is able to reactivate the link. Once this has been achieved, the pair failure flag should be cleared. The mapping and maintenance function may then reallocate this additional capacity to the transmission of application data.

7.5.7 Time slot prioritization/reallocation

In some applications, there may be a need to assign priorities to time slots so that, if any of the pairs fail, the time slots with the highest priority only are transmitted on the remaining pair(s). This implies that, in the event of a pair failure, dynamic reallocation of the high priority time slots to the remaining pairs is required, along with a means of agreeing the reallocation details between the LTU and the NTU. Since the LTU is the master as far as O&M functions are concerned, the time slot reallocation strategy is to be determined at the LTU end of the system. The reallocation may be performed at various points in the transmission path, for example:

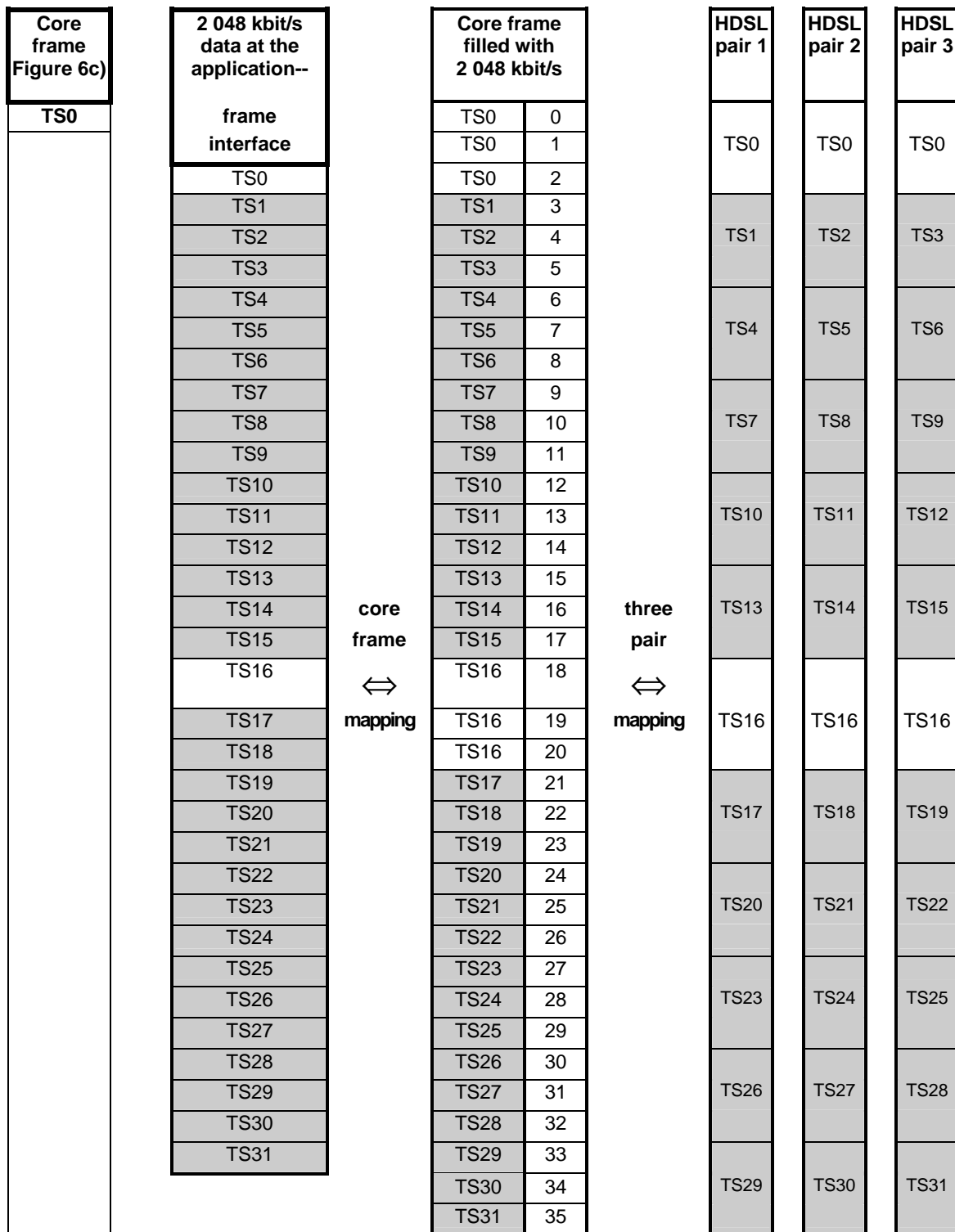
- a) time slot interchanger at the application interface;
- b) core frame mapping;
- c) pair mapping.

Option a) assumes that the application interfaces at both the LTU and the NTU contain the functionality required to interchange time slots and to deal appropriately with signalling and error correction bits in the application frame, so that the application frame can be reconstructed at both application interfaces. This option allows the core and frame mapping at the LTU and the NTU to stay the same following a pair failure.

NOTE: High Priority TSs will be in the new application frames, and Low Priority TSs will not and contain instead AIS. UNI and NNI non-HDSL equipment would need to know status of pairs, because they could not otherwise distinguish between pair failure and no call info which both are indicated by AIS.

Option b) requires a mechanism for informing the NTU core frame mapping function of the changes to the LTU core frame mapping, so that the NTU can replicate the changes.

Option c) requires a mechanism for informing the NTU HDSL frame mapping function of the changes to the LTU HDSL frame mapping, so that the NTU can replicate the changes.



user data (30 X 64 kbit/s channels)

Figure 45: Core frame mapping - Synchronous mapping onto three pairs

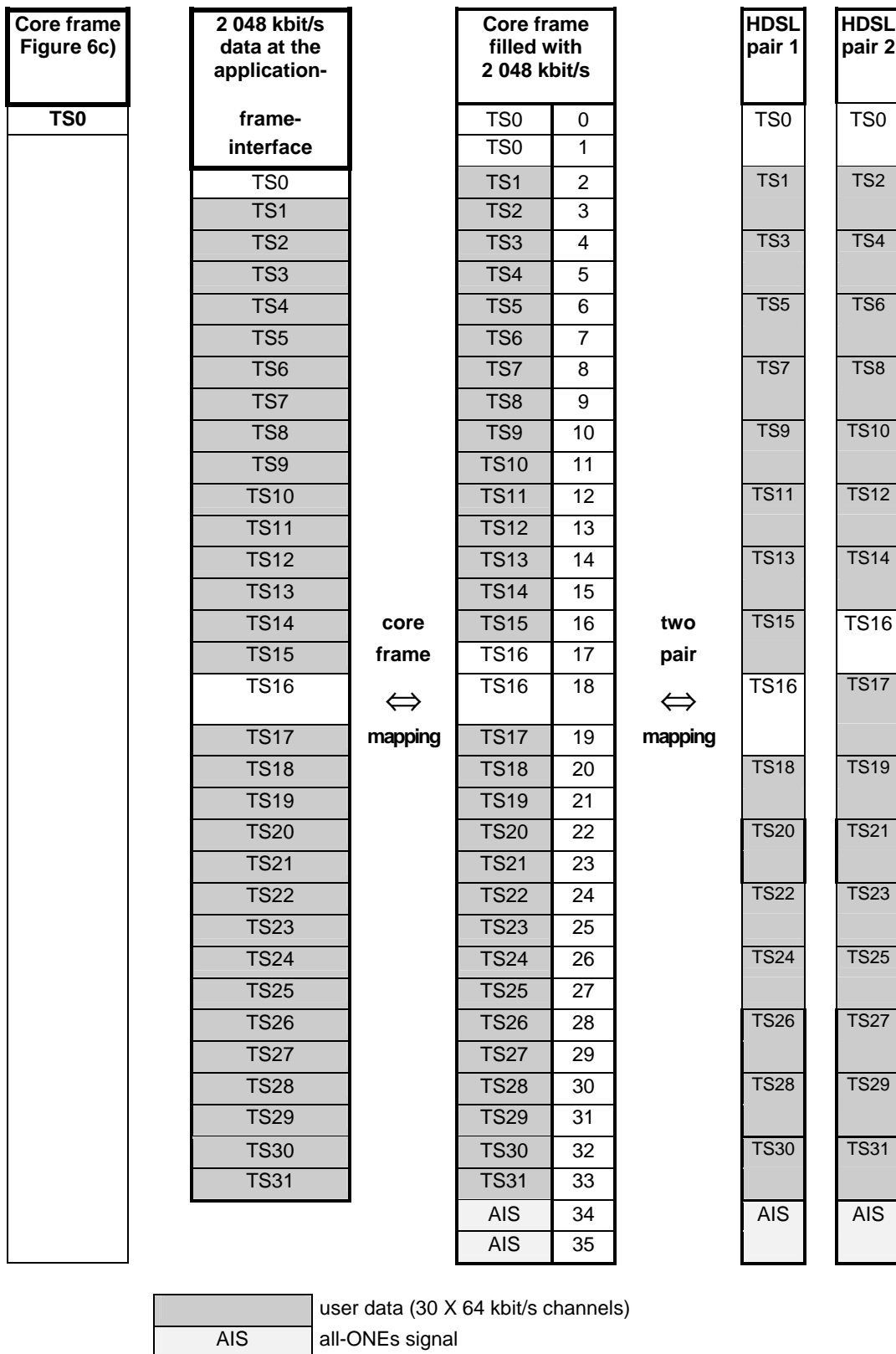
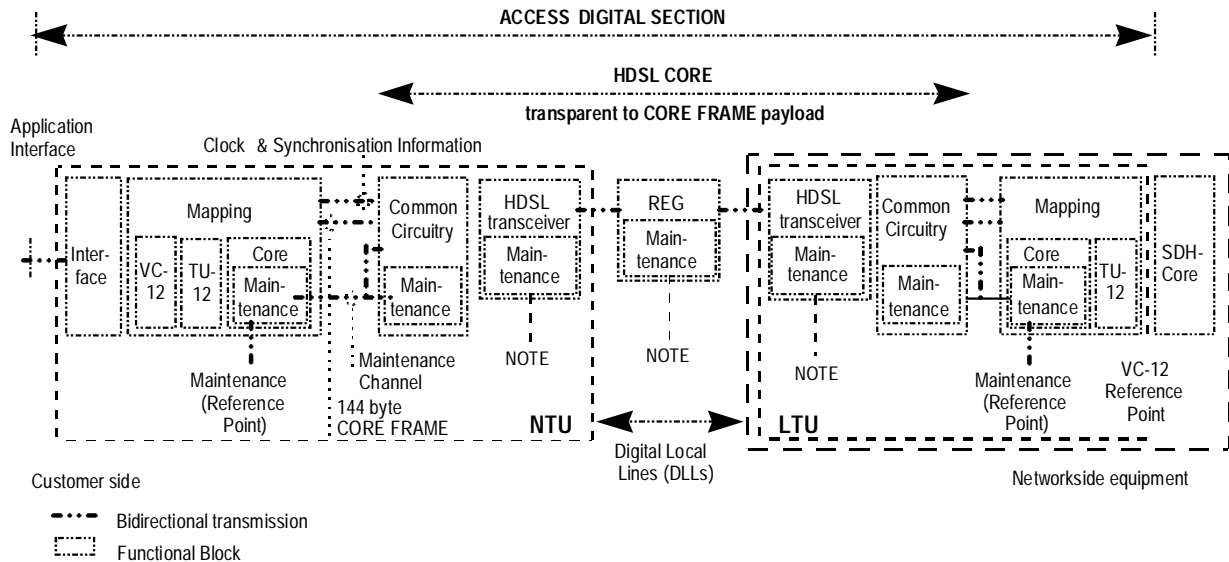


Figure 46: Core frame mapping - Synchronous mapping onto two pairs

7.6 Application specific requirements for the 2 048 kbit/s mapped into TU-12 structure

7.6.1 Reference configuration

The amended access section for the HDSL transmission system with TU-12 structured signals is shown in figure 47. At the NTU mapping part additional VC-12 and TU-12 functions are inserted. The LTU is part of a SDH equipment.



NOTE: A fully equipped HDSL CORE consists of one, two or three H, REG, DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 47: Access Section for TU-12 transport employing HDSL technology

7.6.2 Application Interfaces

7.6.2.1 Application interface at the customer side

The application interface at the customer side shall be a 2 048 kbit/s digital unstructured leased line interface according to ETS 300 246 [2] and ETS 300 247 [3], subclause 7.1.7.2. ETS 300 246 [2] may be replaced by ETS 300 418 [4] in future.

7.6.2.2 Application interface at the network side

No application interface exists at the network side, only a VC-12 reference point internal to the network side equipment between the LTU and the SDH core is defined.

7.6.3 Mapping of application frame into HDSL using TU-12 structure

The data at the application frame are mapped to HDSL in three steps.

7.6.3.1 Mapping of application frame into VC-12 structure

The data at the application interface are mapped into VC-12 structure according to ITU-T Recommendation G.707 [22], subclause 10.1.4. All mapping modes as described in this recommendation shall be supported.

7.6.3.2 Mapping of VC-12 into TU-12

The VC-12 are mapped into the TU-12 structure according to ITU-T Recommendation G.707 [22], subclause 8.3.

7.6.3.3 Mapping of TU-12 into HDSL

As described in subclause 5.4 the TU-12 structured data having a bit rate of 2 304 kbit/s shall be mapped into a core frame with 144 bytes and 500 μ s length. Pointer byte V1 shall be located in byte 144 of the core frame. The bits Z_{m9} to Z_{m48} are unused and shall be set to ONE.

The mapping process into three and two pairs is shown in figures 48 and 49.

7.6.4 Mapping of HDSL maintenance functions to the interface

The access digital section shall be considered operational when all of the transceiver pairs have indicated completion of the activation procedure (see subclause 5.6), correct pair identification has been achieved in the core frame, as described in subclause 6.2, and no further failure condition is detected. If one of the transceiver pairs is indicating non-operational condition or incorrect pair identification, the access digital section shall be considered non-operational.

The fact that the D2048U signal is unstructured makes it impossible for the HDSL core to map any operation and maintenance information into or out of the payload because the HDSL system does not have any information about the contents or the internal structure of the transmitted data.

The only information the core can get is "LOS at the application interface of LTU" and "LOS at the application interface of NTU". When LOS at the application interface of NTU or LTU is detected, an "All ONES" signal shall be transmitted to the far end of the HDSL system. At the same time bit 15 of the HDSL frame ("losd") shall be set to ZERO as shown in table 38.

Table 38: LOS at the application interface of LTU and NTU

Leased line input condition	Action
LOS at the application interface of LTU	losd=0 in HOH (LTU/NTU)
LOS at the application interface of NTU	losd=0 in HOH (NTU/LTU)

The mapping of LOS/LFA at the line side of LTU, NTU, and both sides of REG to the application interface is shown in table 39.

Table 39: Mapping of maintenance functions to the application interfaces

Condition on one (or more) pair(s)	Message towards the application interface of	
	NTU	LTU
LOS/LFA at LTU line side	(see note)	AIS
LOS/LFA at NTU line side	(see note)	AIS
LOS/LFA at REG-R	(see note)	AIS
LOS/LFA at REG-C	(see note)	AIS
NOTE:	As long as the HDSL system is not in the full operating state, i.e. not all of the HDSL transceivers are in the Active-Rx/Tx state, the signal towards the application interface of the NTU is not defined.	

7.6.5 Performance

7.6.5.1 Performance specification

The overall performance shall be such that the performance limits defined in ITU-T Recommendation G.826 [10] can be met.

7.6.5.2 Signal transfer delay

The one-way signal transfer delay between the application interface at the NTU and the TU-12 reference point at the LTU shall not exceed 1 250 μ s. This shall be calculated as the mean delay for both directions. The allocation for a 2B1Q HDSL system shall be as follows:

- LTU \leq 450 μ s;
- NTU \leq 450 μ s;
- REG \leq 200 μ s;
- line \leq 150 μ s.

7.6.5.3 Clock specification

7.6.5.3.1 Clock synchronization at the NTU

The TU-12 signal towards the network shall use the TU-12 timing of the incoming direction from the network side as timing reference.

The NTU timing towards the application interface may be derived from:

- the received VC-12 signal;
- the received TU-12 signal, with an additional frame buffer inserted in the receive direction.

7.6.5.3.2 Jitter specification

The tolerance to input jitter as well as the jitter transfer limitation are defined in terms of the amplitude and frequency of sinusoidal input jitter which, when modulating a $2^{15} - 1$ pseudo random test sequence of the 2 048 kbit/s bit stream at the nominal rate and with tolerances of +50 ppm and -50 ppm, shall not cause bit errors in the transmission system or jitter at the relevant output in excess of the limits defined below. This test method is used for convenience of testing and is not, in itself, intended to be representative of the type of jitter to be found in practice.

The tolerable input jitter is given in figure 38 (subclause 7.1) with the values of table 40. The output jitter limits given in table 41 shall be met when applying the tolerable jitter to the relevant input.

Table 40: Parameter values for input jitter tolerance at inputs

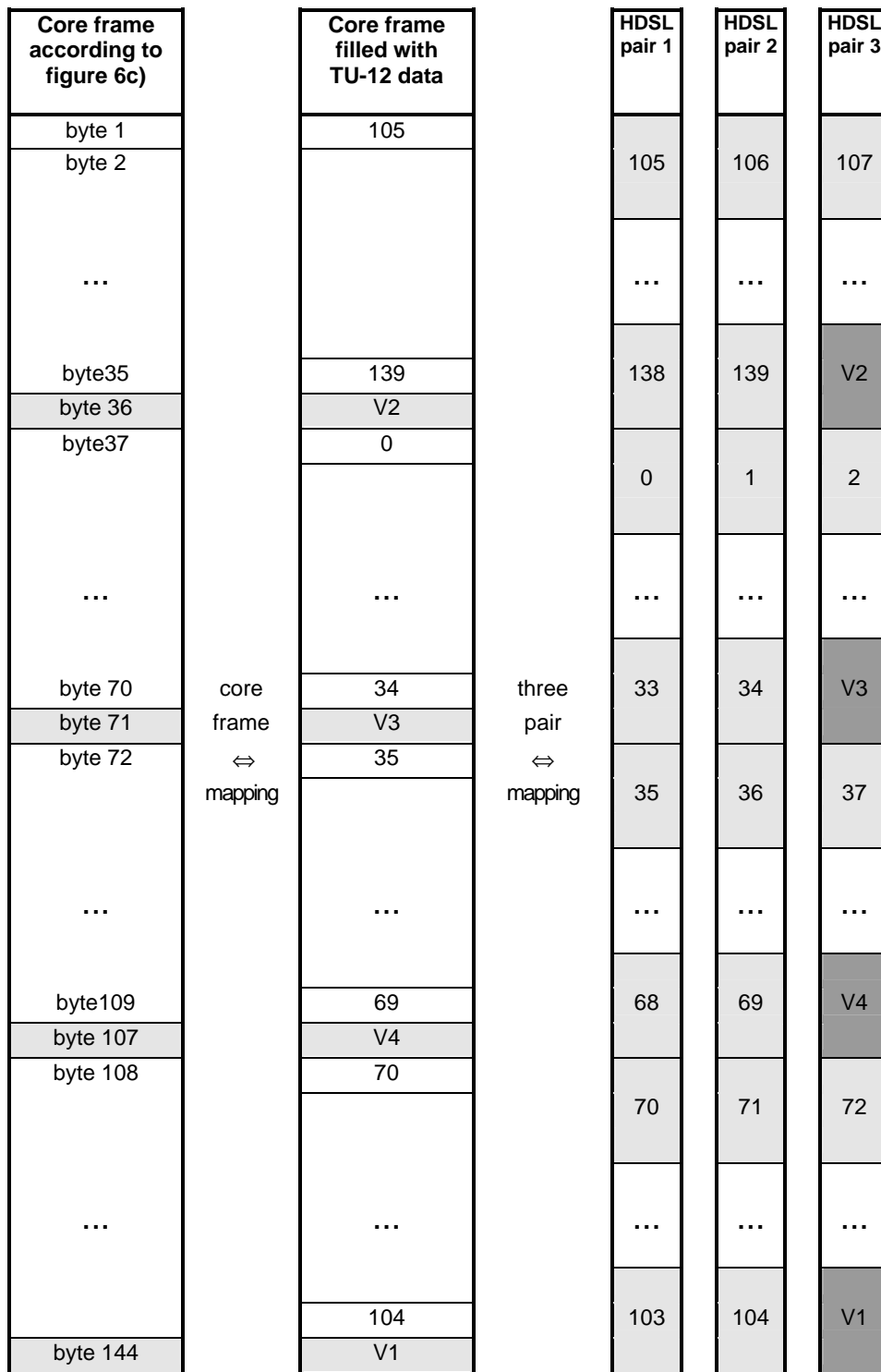
Application interface	Parameter:	Peak-to-peak amplitude			Frequency				
		A0	A1	A2	f0	f1	f2	f3	f4
at NTU (input)	Value	-	1,1	0,11	-	-	4	0,04	100
at LTU (input)	Value	-	1,35	0,18	-	20	2 400	18	100
	Units	-	U _{Ipp}	U _{Ipp}	-	Hz	Hz	kHz	kHz
NOTE 1: U _{Ipp} = Unit Interval peak-peak. 1 U _{Ipp} = 1/2 048 kHz = 488 ns for the D2048U application.									
NOTE 2: The values for the NTU input are taken from ETS 300 247 [3].									
NOTE 3: The values for the LTU input are taken from ITU-T Recommendation G.823 [9] but reduced by 10 % margin for jitter accumulation in the HDSL transmission system.									

Table 41: Maximum permitted values of output jitter

Application interface	Parameter	Maximum permissible jitter		Measurement bandpass parameters (high pass part has first order slope)		
		B1; (f1-f4)	B2; (f3-f4)	f1	f3	f4
at NTU output	Value	1,5	0,2	20	18 000	100
at LTU output	Value	0,3	0,15	20	700	100
	Units	U _{Ipp}	U _{Ipp}	Hz	Hz	kHz
NOTE 1: The values for the NTU output are taken from ETS 300 247 [3].						
NOTE 2: The values for the LTU output are based on the input at NTU, but increased for jitter accumulation in the HDSL transmission system in the lower frequency area and based on high Q transmission network following.						

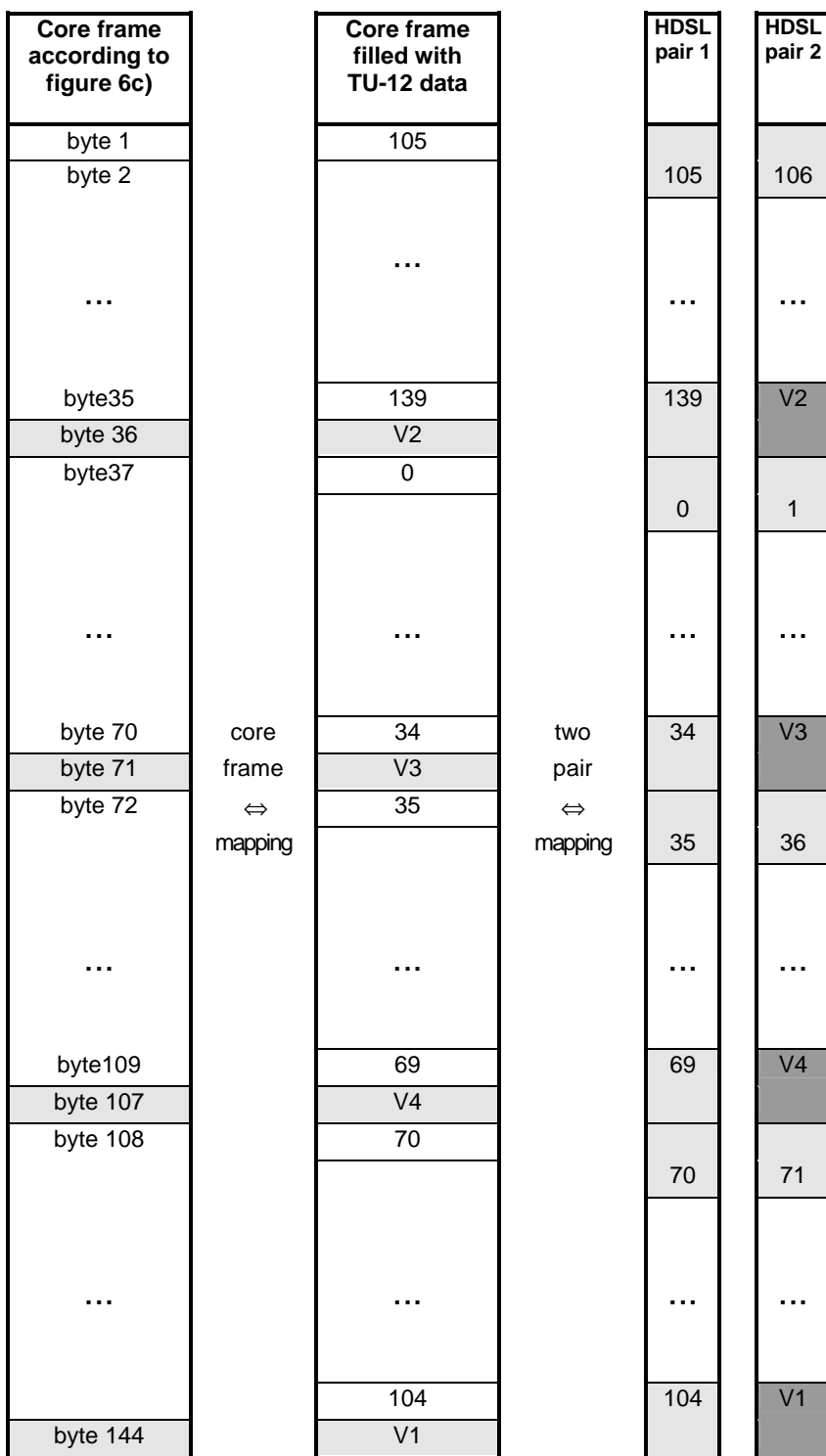
7.6.5.4 Laboratory performance measurement

The test arrangement and procedures of subclause 6.3 shall be used. The performance shall be evaluated between the application interface at the NTU and the VC-12 reference point in the LTU between the mapping functionality and the SDH core. A special adaptor will be used for the connection of the measuring equipment to the internal VC-12 reference point.



NOTE: V1, V2 and V3 are TU -12 pointers 1, 2 and 3; V4 is set to ONE. These bytes are part of the TU-12 and terminated at a pointer processor.

Figure 48: Core frame mapping of TU-12 option - Synchronous mapping into three pairs



NOTE: V1, V2 and V3 are TU-12 pointers 1, 2 and 3; V4 is set to ONE. These bytes are part of the TU-12 and terminated at a pointer processor.

Figure 49: Core frame mapping of TU-12 option - Synchronous mapping into two pairs

7.7 Application specific requirements for the simultaneous connection of 2 048 kbit/s digital signals and ISDN-BA inside the HDSL core frame

7.7.1 Reference Configuration

This application allows the simultaneous transport of an ISDN-BA inside the HDSL core frame. The reference configuration is shown in figure 49A. It contains in addition to the 2 048 kbit/s interface function another for the ISDN-BA, which converts the ISDN-BA into a digital 192 kbit/s signal, and an adaptation and a multiplexing function for the mapping of the ISDN-BA into the core frame.

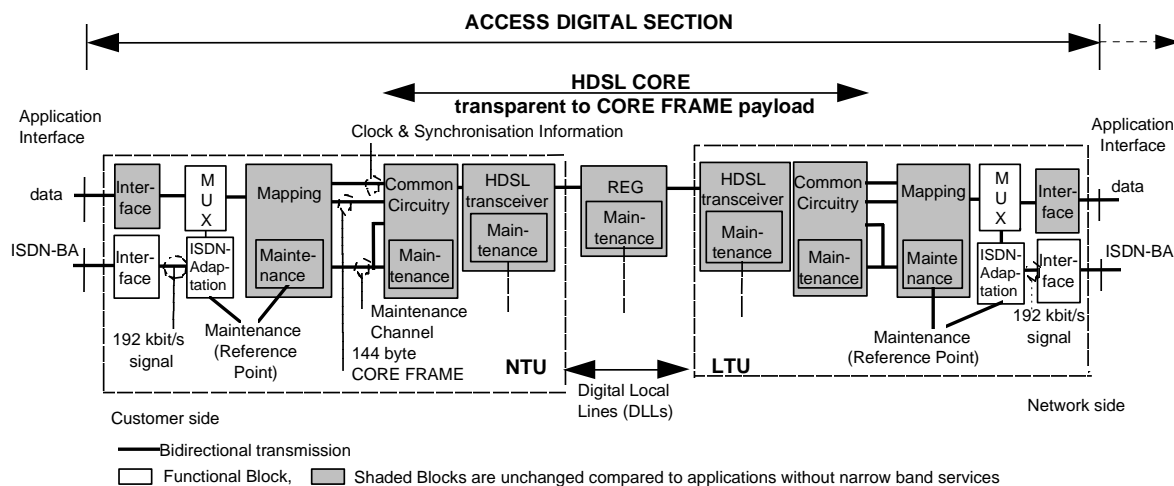


Figure 49A: Access section for simultaneous transport of narrowband and 2 048 kbit/s signals

7.7.2 Application interfaces

7.7.2.1 Application interfaces at the customer side

7.7.2.1.1 2 048 kbit/s interfaces

The application interface at the customer side shall be as described in subclause 7.1 for ISDN-PRA, subclause 7.2 for unstructured leased line and subclause 7.3 for structured leased line.

7.7.2.1.2 ISDN interfaces

The application interface for ISDN-BA at the T-reference point of the customer side shall be according to ETS 300 012 [27].

7.7.2.2 Application interfaces at the network side

7.7.2.2.1 2 048 kbit/s interfaces

The application interface at the network side shall be as described in subclauses 7.1 for ISDN-PRA, 7.2 for unstructured leased line and 7.3 for structured leased line.

7.7.2.2.2 ISDN interfaces

The application interface at the network side shall provide for an interface representing a V1-reference point or for an U-reference point, which has to be converted by a LT-function to a V1-reference point. The requirements for the access digital section between the V1- and the T-reference points are defined in ETS 300 297 [28].

7.7.3 Mapping procedures

7.7.3.1 Conversion of the ISDN-BA signals

The ISDN-BA signals at the application interface shall be converted into a structured digital 192 kbit/s signal with a frame length of three bytes, where the first two bytes shall contain the B-channels of the ISDN-BA. The third byte, which is shown in figure 49B as D+byte, shall contain the D-channel in the first and second bit position and bits S1 to S4 for interface activation/deactivation and loopback 2 activation/deactivation for 4B3T-based applications according to ETR 80 [6], annex B, in the fifth to eighth bit position. X1 and X2 in the third and fourth bit position can be used for the transport of special information in 4B3T applications or the CL-channel for 2B1Q-based applications according to ETR 80 [6], annex A, where X2 is used for the CL-channel and X1 for its multiframe indication.

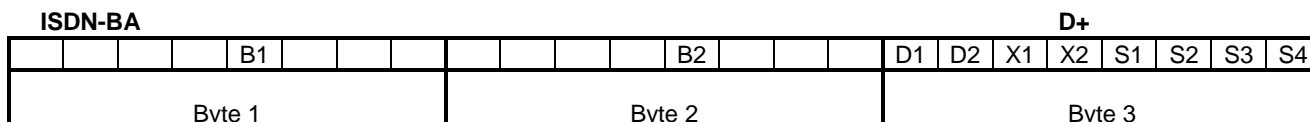


Figure 49B: Structure of the 192 kbit/s of an ISDN-BA-frame

7.7.3.2 Mapping of the ISDN-BA to the core frame

As described in subclause 5.4 the application data shall be mapped bit sequence independently into a core frame with 144 bytes and 500 μs length. Only 128 bytes are occupied by the 2 048 kbit/s data signal. Into the remaining 16 bytes - indicated R and Y in figure 6b)- a 127 bit ISDN-sequence, containing the 12 bytes of 4 ISDN-BA-frames, a 7 bit Synch Word and 3 spare bytes Z, shall be transported. Figure 49C shows such an ISDN-sequence of 127 bit in one core frame. Dependent upon different tolerances of the ISDN-BA- and the data-clock this ISDN-sequence is floating inside the core frame, Figures 49D shows examples for possible positions.

The correct position of the ISDN-sequence is indicated by the synchronization word with a 7 bit long Barker Code 1110010, which has to be detected at the receiver.

To prevent simulation of the synchronization word the ISDN-sequence shall -with the exception of the synchronization word and the justification bits- be scrambled with the simple polynomial $1 + x^{-6} + x^{-7}$.

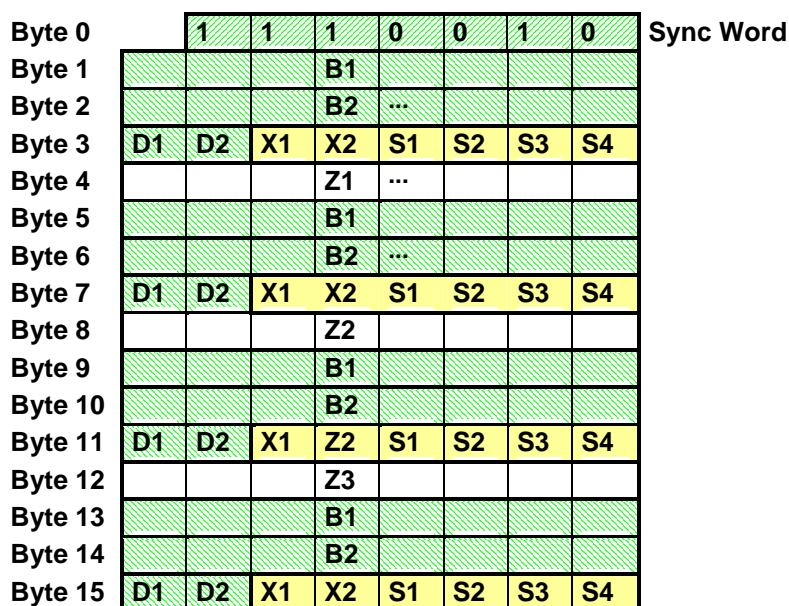
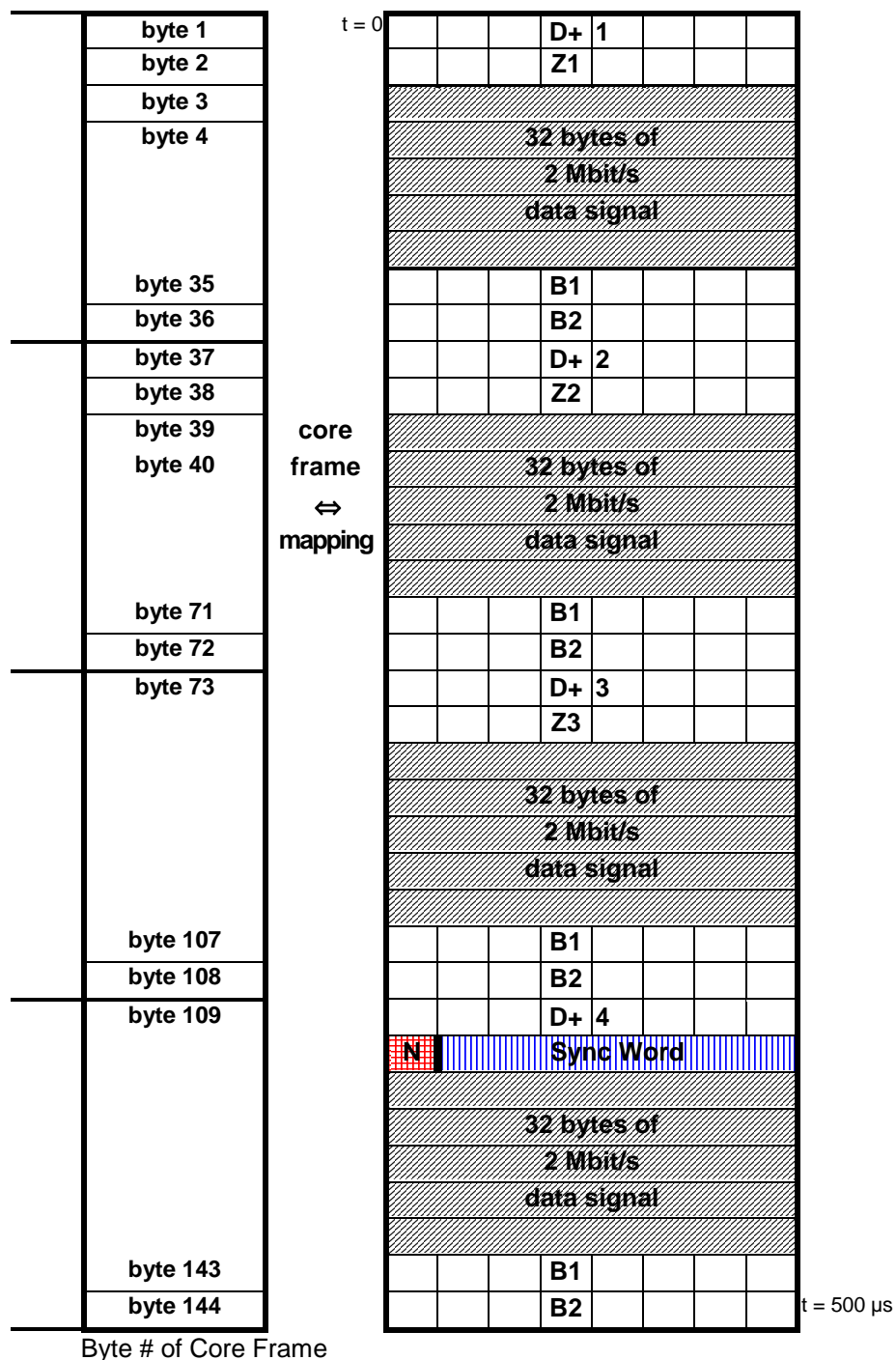


Figure 49C: Structure of a ISDN-sequence with 127 bit

7.7.3.3 Core frame mapping into HDSL frame

The mapping from core frame to HDSL transmission frame takes place in exactly the same way as for the other applications, as can be seen from figure 9.



unshaded bit positions: (B1 & B2 & D+ & spare Z) of ISDN-sequence.
 N: negative justification possibility containing stuffing.

Figure 49D (1/3): Core frame for simultaneous transport of 2 048 kbit/s data and ISDN-BA; ZERO justification state

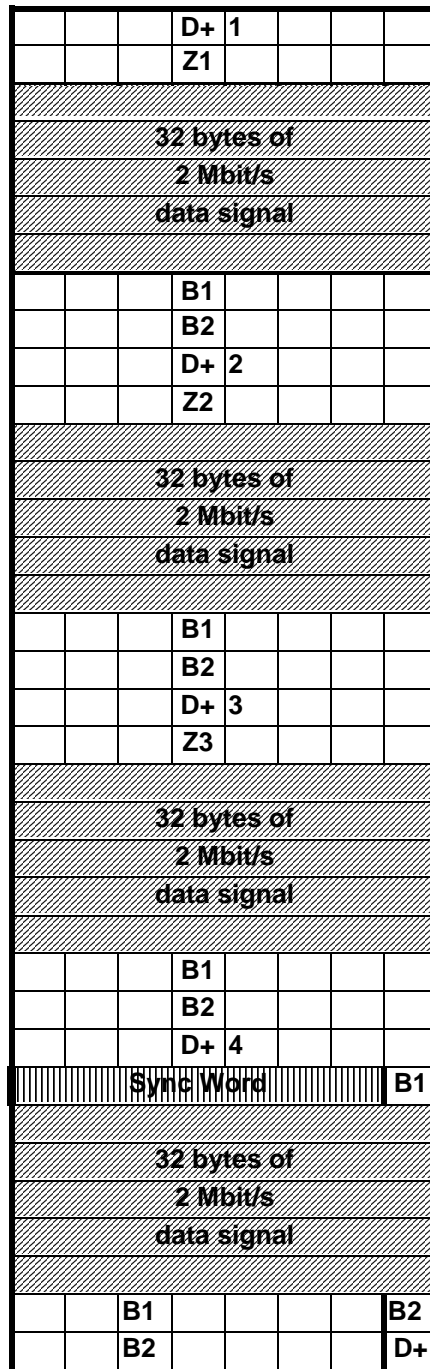


Figure 49D (2/3): Negative Justification

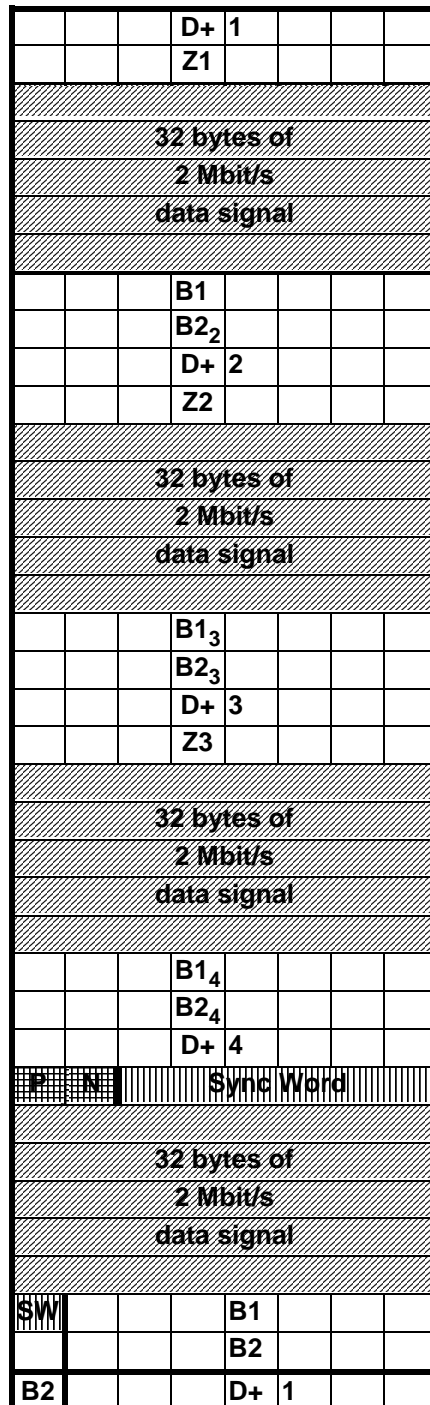


Figure 49D (3/3): Positive justification

7.7.4 Mapping of HDSL maintenance functions to the interface

The maintenance functions and the mapping procedures shall be as given in the relevant applications in subclauses 7.1, 7.2 and 7.3.

The mapping function of the ISDN-BA shall be informed by the HDSL maintenance function and insert suitable failure messages as defined in ETR 80 [6] into the signal at the interface.

An additional maintenance reference point is foreseen at the ISDN-adaptation function for the access to the Z-bytes.

7.7.5 Performance

7.7.5.1 Performance specification

The overall performance shall be such that the performance limits defined in ITU-T Recommendation G.826 [10] for data and ITU-T Recommendation G.821 [31] for ISDN-BA can be met.

NOTE: Due to the complex synchronization mechanisms used for the ISDN subsystem micro interruptions on the HDSL-line may lead to interruptions up to 21 ms of the ISDN-BA access digital section.

7.7.5.2 Signal transfer delay

The one-way signal transfer delay between the application interfaces for data and ISDN-BA shall not exceed 1 250 μ s. This shall be calculated as the mean delay for both directions. The allocation for the data signal shall be as given in the relevant data applications.

7.7.5.3 Clock specification

7.7.5.3.1 NTU clock tolerance

The tolerance of the free running NTU clock shall be ± 50 ppm.

7.7.5.3.2 LTU clock tolerance

The tolerance of the free running LTU clock shall be ± 50 ppm.

7.7.5.3.3 ISDN clock tolerance

The tolerance of the ISDN clock is ± 32 ppm.

7.7.5.3.4 Clock synchronization for ISDN-BA

The ISDN-terminal has to be synchronized to the clock of the ISDN and for this purpose the ISDN-clock at the LTU application interface has to be transported transparently through the HDSL transmission system. The ISDN- clock has therefore to be mapped to the clock of the application data by means of a zero/positive/negative justification procedure.

When both clocks have their nominal values (zero-justification) in bit N dummy information is inserted permanently. The relevant frame is shown in figure 49D (1/3).

When the clock of the ISDN-BA is higher than the data clock, a negative justification is necessary. In this case bit N is used occasionally for the transport of information, which is the first bit of the ISDN-sequence synchronization word. The start position of the ISDN-sequence with the synchronization word is decremented one unit interval as shown in figure 49D (2/3).

When the clock of the ISDN-BA is lower than the data clock, a positive justification is necessary. In this case a stuffing bit P occurs in the bit position prior to N, to compensate the lack of information in the ISDN-sequence. The start position of the ISDN-sequence with the synchronization word is incremented one unit interval as shown in figure 49D (3/3).

Both justification bits keep their position relative to the synchronization word and are therefore floating together with the synchronization word inside the core frame.

Justification indication is derived by comparing the position of the clocks of the core frame and the frame of the ISDN sequence. No extra justification control bits are necessary.

7.7.5.3.5 Jitter and wander specification

For the 2 048 kbit/s interface the jitter specifications of subclauses 7.1.3.3.3, 7.2.4.3.3 and 7.3.4.3.3 respectively and the wander specification of subclause 7.1.3.3.4 shall be applied.

The jitter for the ISDN-BA application interface is specified in ETS 300 012 [27], subclause 9.3, and shown in figure 49E.

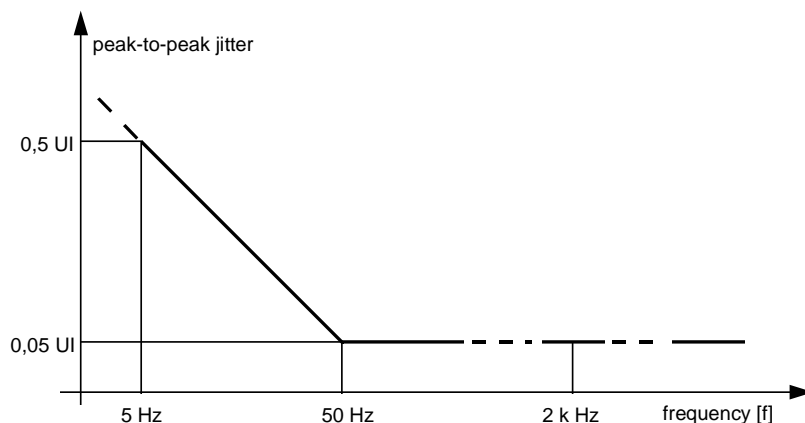


Figure 49E: Output jitter at ISDN-BA interface

7.7.5.4 Laboratory performance measurements

It is assumed that the performance can be evaluated at the application interface. The test arrangement and procedures of subclause 6.3 shall be used.

7.7.6 Power feeding

The operation of the ISDN-BA has to be maintained under all conditions of operation. Therefore remote power feeding of the NTU is preferred.

Where this is not possible a means shall be provided, which allows to bypass the data modem in case of local power failure and to keep only the ISDN-BA operational and to feed them remotely. A loss of power at NTU is indicated to the LTU according to subclause 5.4.2.2 by the HDSL overhead bits ps1 and ps2, which shall be used as control message for the bypass.

7.8 Application specific requirements for the simultaneous connection of 2 048 kbit/s digital signals and analogue telephone lines inside the HDSL core frame

7.8.1 Reference Configuration

This application allows the simultaneous transport of up to three A/D-converted analogue telephone signals inside the HDSL core frame. The reference configuration is shown in figure 49F. It contains in addition to the 2 048 kbit/s interface function other interface functions for analogue telephone signals, which converts these signals including their belonging signalling information into a digital 72 kbit/s signal and an adaptation and a multiplexing function for the mapping of the telephone signals into the core frame.

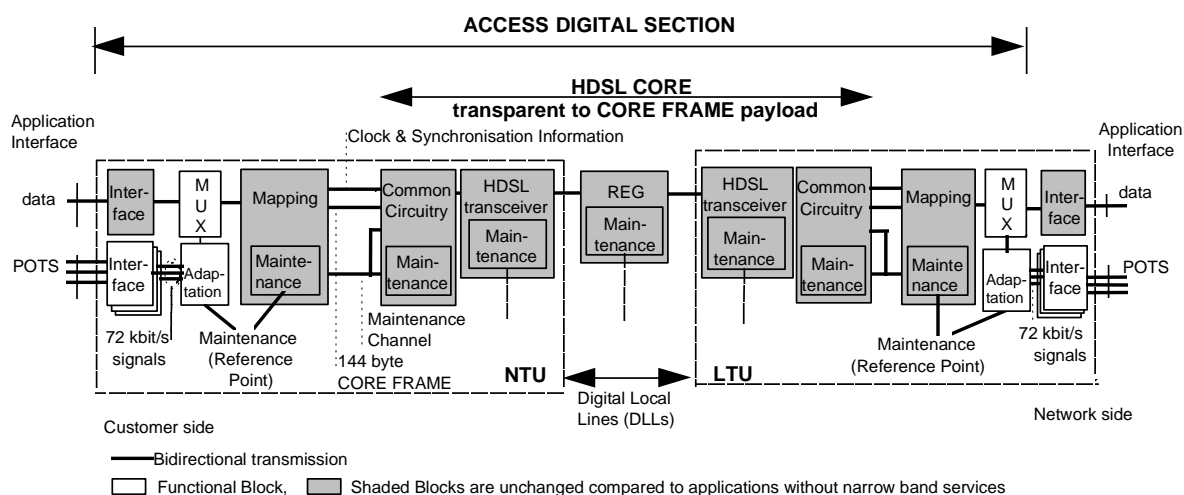


Figure 49F: Access section for simultaneous transport of analogue telephone connections and 2 048 kbit/s data signals

7.8.2 Application interfaces

7.8.2.1 Application interface at the customer side

7.8.2.1.1 2 048 kbit/s interfaces

The application interface at the customer side shall be as described in subclauses 7.1 for ISDN-PRA, 7.2 for unstructured leased line and 7.3 for structured leased line.

7.8.2.1.2 Analogue telephone interfaces

The application interfaces at the customer side for analogue telephones shall be according to ITU-T Recommendation Q.552 [29]. The signalling may be country specific.

7.8.2.2 Application interface at the network side

7.8.2.2.1 2 048 kbit/s interfaces

The application interface at the network side shall be as described in subclauses 7.1 for ISDN-PRA, 7.2 for unstructured leased line and 7.3 for structured leased line.

7.8.2.2.2 Analogue telephone interfaces

The application interfaces at the network side for analogue telephones, including the signalling, are country specific.

7.8.3 Mapping procedures

7.8.3.1 Conversion of the analogue telephone signals

The analogue telephone signals at the application interface shall be converted into a digital 64 kbit/s signal according to CCITT Recommendation G.711 [30]. The signalling information is converted into a 4 bit blocks with a bit rate of 8 kbit/s. The signalling information and the coding will be country specific.

7.8.3.2 Mapping of the combined signals to the core frame

As described in subclause 5.4 the application data shall be mapped bit sequence independently into a core frame with 144 bytes and 500 μ s length. Only 128 bytes are occupied by the 2 048 kbit/s data signal. The remaining 16 bytes - indicated R and Y in figure 6b) - shall be used for the transport of a 7 bit synchronization word, the bytes of the three digital telephone signals and the belonging signalling information and three 4 bit blocks of spare capacity Z with 24 kbit/s. The resulting core frame structure is shown in figure 49G. The bytes of the telephone channels as well as signalling and spare capacity blocks have fixed positions in the core frame.

NOTE: The 7 bit Barker Code synchronization word (1110010) is not necessary in this application, it is used to keep the frame structure of the ISDN-BA application.

7.8.3.3 Core frame mapping into HDSL frame

The mapping from core frame to HDSL transmission frame takes place in exactly the same way as for the other applications, as can be seen from figure 9.

7.8.4 Mapping of HDSL maintenance functions to the interface

The maintenance functions and the mapping procedures shall be as given in the relevant applications in subclauses 7.1, 7.2 and 7.3.

An additional maintenance reference point is foreseen at the adaptation function for the access to the Z-bytes.

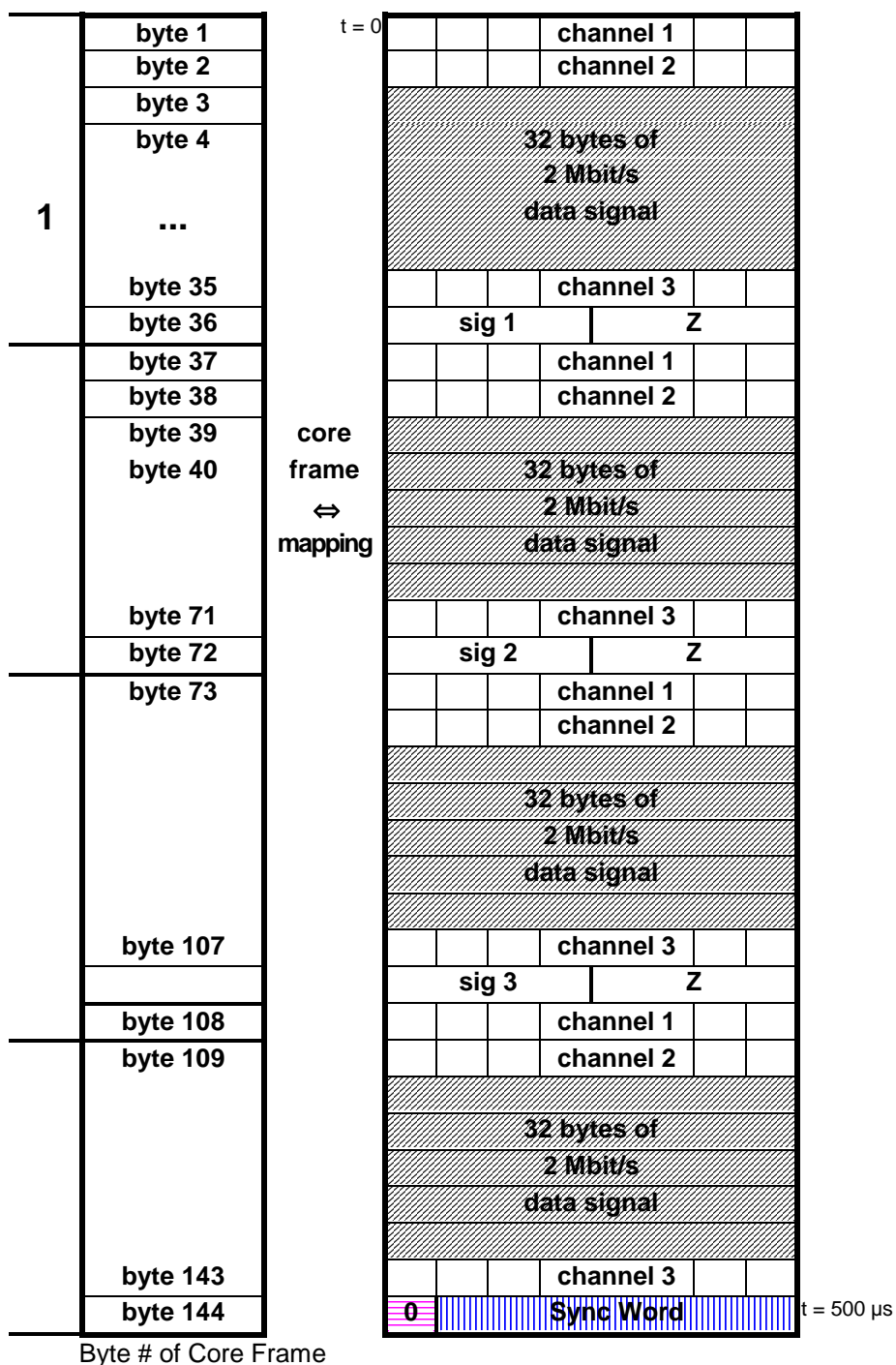
7.8.5 Performance

7.8.5.1 Performance specification

The overall performance shall be such that the performance limits defined in ITU-T Recommendation G.826 [10] can be met.

7.8.5.2 Signal transfer delay

The one-way signal transfer delay between the application interfaces for data and analogue telephone applications shall not exceed 1 250 μ s. This shall be calculated as the mean delay for both directions. The allocation shall be as given in the relevant data applications.



sig x = 4 bit blocks for signalling of channel x
 Z = spare capacity 24 kbit/s
 Bit 144/1 = fixed stuffing bit = ZERO
 Bit 144/2 to 144/8 = Synchronization Word 1110010

Figure 49G: Core frame for simultaneous transport of 2 048 kbit/s data and narrowband services

7.8.5.3 Clock specification

7.8.5.3.1 NTU clock tolerance

The tolerance of the free running NTU clock shall be ± 50 ppm.

7.8.5.3.2 LTU clock tolerance

The tolerance of the free running LTU clock shall be ± 50 ppm.

7.8.5.3.3 Clock synchronization for analogue telephony interfaces

No particular requirement exists for the clock at the analogue telephony application interface. The A/D-converter is synchronized to the clock of the core frame which is synchronized to the clock of the data application interface.

7.8.5.3.4 Void

7.8.5.3.5 Jitter and wander specification

For the 2 048 kbit/s interface the jitter specifications of subclauses 7.1.3.3.3, 7.2.4.3.3 and 7.3.4.3.3 respectively and the wander specification of subclause 7.1.3.3.4 shall be applied.

7.8.5.4 Laboratory performance measurements

It is assumed that the performance can be evaluated at the application interface. The test arrangement and procedures of subclause 6.3 shall be used.

7.8.6 Power feeding

The operation of the telephone access has to be maintained under all conditions of operation. Therefore remote power feeding of the NTU is preferred.

Where this is not possible a means shall be provided, which allows to bypass the data modem in case of local power failure and to keep only the telephone connections operational and to feed them remotely. A loss of power at NTU is indicated to the LTU according to subclause 5.4.2.2 by the HDSL overhead bits ps1 and ps2, which shall be used as control message for the bypass.

8 Power feeding

8.1 General

This clause deals with remote power feeding of regenerator or NTU and wetting current requirements.

Remote power feeding of the NTU is only required in some applications. Remote power feeding of optional regenerators is a requirement. However a detailed specification of a regenerator is outside the scope of the present document.

The case where regenerator and NTU are both remotely powered is excluded since it is considered not feasible within the limited power budget available.

Due to the:

- different national safety requirements;
- different DLL planning rules;
- the optional use of regenerators; and
- the application dependant requirement to power the NTU;

no detailed power feeding requirement is provided. Instead general guidelines are provided for the situations where remote powering is required.

8.2 Wetting current

Wetting current may be used to prevent corrosion of contacts. In the case of remote power feeding the feeding current is enough to fulfil the wetting current requirements.

Figure 50 gives the basic concept for the provision of wetting current.

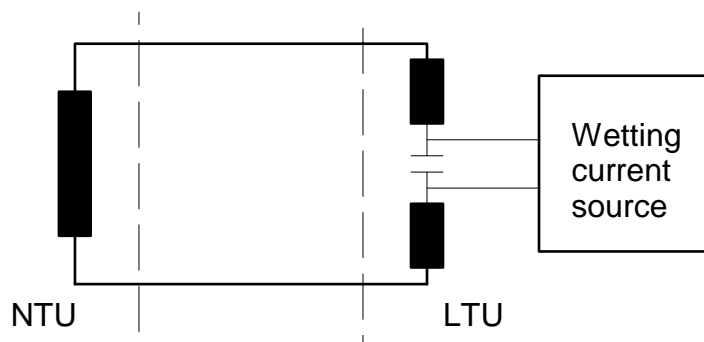


Figure 50: Basic method for provision of wetting current

The wetting current shall be less than 20 mA.

8.3 Remote power feeding aspects

Parallel power feeding is recommended as basic method of power feeding for all HDSL applications and configurations (e.g. 1, 2 or 3 pairs, partial operation).

The NTU/REG shall be able to deal with polarity reversal.

Figure 51 shows the basic circuit for parallel power feeding.

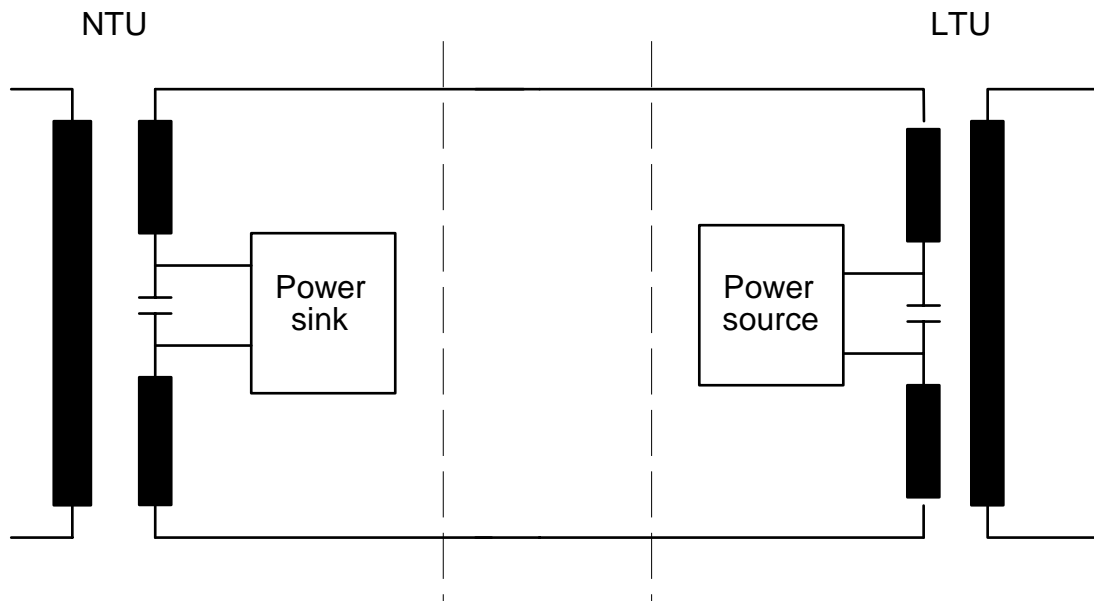


Figure 51: Parallel power feeding

8.3.1 Remote power feeding aspects at the LTU

If the LTU provides remote power this power is shared over all the available pairs. This should prevent that the majority of the power is transported over the pair with the lowest resistance.

The provision of power in partial operation is for further study.

8.3.2 Remote power feeding aspects at the NTU

Power will be delivered to the NTU via each HDSL pair. The total power (derived from all available pairs) can be used to operate the NTU. HDSL transceivers which are not active may be placed in a low power consumption mode or switched off.

8.3.3 Remote power feeding aspects at the regenerator

Remote power feeding of a regenerator shall be done on a per pair basis.

The regenerator shall, if required, also provide wetting current towards the NTU. The amount of wetting current which can be provided may be dependant on the available power budget.

Figure 52 shows the basic circuit for remote power feeding of a regenerator and provision of wetting current.

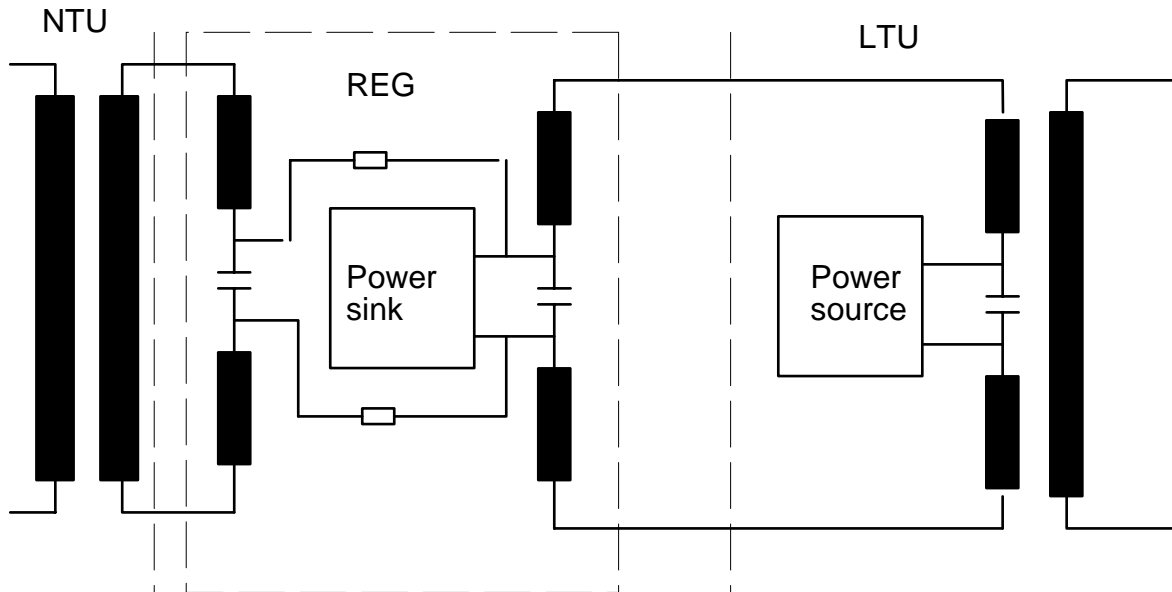


Figure 52: Basic concept to power a regenerator and to provide wetting current

9 Environmental requirements

9.1 Climatic conditions

Climatograms applicable to the operation of HDSL equipment can be found in ETS 300 019 [11]. The choice of classes is under national responsibility.

9.2 Safety

No safety requirements are specified under the present document.

NOTE 1: Safety requirements are imposed under the Low Voltage Directive (73/23/EEC).

NOTE 2: EN 60950 [13] is normally applicable.

9.3 Overvoltage protection

No overvoltage protection requirements are specified under the present document.

NOTE: Dependent on the equipment NTU, LTU or REG the ITU-T Recommendations K.21 [16], K.20 [15] or CCITT Recommendation K.17 [14] should be applied.

9.4 Electromagnetic compatibility (EMC)

The EMC requirements are defined according to the equipment type and as described in ETS 300 386-2 [17] or ETS 300 386-1 [18] as applicable.

NOTE: Additional EMC requirements may be imposed under EMC Directive (89/336/EEC).

Annex A (informative): Detailed definition of cable characteristics and test loops

A.1 Typical characteristics of cables

Annex A contains tables of typical parameters of cables, together with calculated values of the expected test loop behaviour. Practical measurements on cables or test loops will not necessarily be identical to the values in these tables. Additional information on cables and test loops (including graphical representations) can be found in ETR 080 [6], annex C.

Table A.1: Parameters of 0,4mm PE cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	268	268	269	271	282	295	312	390	425
L' (μ H/km)	680	678	675	669	650	642	635	619	608
C' (nF/km)	45,5	45,5	45,5	45,5	45,5	45,5	45,5	45,5	45,5

Table A.2: Parameters of 0,5mm PE cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	172	172	173	175	190	207	227	302	334
L' (μ H/km)	680	678	675	667	646	637	629	603	592
C' (nF/km)	25	25	25	25	25	25	25	25	25

Table A.3: Parameters of 0,6mm PE cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	119	120	121	125	146	167	189	260	288
L' (μ H/km)	700	695	693	680	655	641	633	601	590
C' (nF/km)	56	56	56	56	56	56	56	56	56

Table A.4: Parameters of 0,8mm PE cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	67	70	72,5	75,0	91,7	105	117	159	177,5
L' (μ H/km)	700	700	687	665	628	609	595	568	543
C' (nF/km)	37,8	37,8	37,8	37,8	37,8	37,8	37,8	37,8	37,8

Table A.5: Parameters of 0,32mm PVC cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	419	419	419	419	427	453	493	679	750
L' (μ H/km)	650	650	650	650	647	635	621	577	560
C' (nF/km)	120	120	120	120	120	120	120	120	120

Table A.6: Parameters of 0,4mm PVC cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	268	268	268	268	281	295	311	391	426
L' (μ H/km)	650	650	650	650	635	627	619	592	579
C' (nF/km)	120	120	120	120	120	120	120	120	120

Table A.7: Parameters of 0,63 mm PVC cables

Frequency	0 Hz	10 kHz	20 kHz	40 kHz	100 kHz	150 kHz	200 kHz	400 kHz	500 kHz
R' (Ω /km)	108	108	108	111	141	173	207	319	361
L' (μ H/km)	635	635	635	630	604	584	560	492	469
C' (nF/km)	120	120	120	120	120	120	120	120	120

A.2 Theoretical characteristics of test loops for $Y = 31$ dB at 150 kHz

Table A.8: Loop 2

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		15,2	19,0	23,4	28,6	31,0	33,3	42,5	46,8
Phase (deg)		-97	-165	-280	-611	-889	-1 168	-2 277	-2 823
Group Delay (μ s)		21,7	17,0	15,4	15,4	15,5	15,6	15,3	15,1
Impedance (Ω) at NTU	Re.	228	179	146	126	122	120	117	117
	Im.	-209	-129	-82	-39	-28	-23	-14	-13
Impedance (Ω) at LTU	Re.	228	179	146	126	122	120	117	117
	Im.	-209	-129	-82	-39	-28	-23	-14	-13

Table A.9: Loop 3

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		16,4	20,0	23,2	28,3	31,3	34,5	45,9	50,3
Phase (deg)		-114	-191	-336	-770	-1 129	-1 489	-2 896	-3 588
Group Delay (μ s)		23,8	20,2	20,1	20,0	20,0	19,9	19,4	19,1
Impedance (Ω) at NTU	Re.	219	199	166	120	123	120	117	116
	Im.	-152	-98	-91	-41	-27	-26	-13	-13
Impedance (Ω) at LTU	Re.	257	190	134	128	121	116	118	120
	Im.	-201	-151	-84	-33	-34	-19	-17	-12

Table A.10: Loop 4

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		15,3	19,3	23,3	28,2	31,2	34,3	45,6	50,0
Phase (deg)		-113	-195	-339	-768	-1 126	-1 484	-2 887	-3 578
Group Delay (μ s)		25,5	20,9	19,6	19,9	20,0	19,9	19,3	19,1
Impedance (Ω) at NTU	Re.	128	110	114	105	109	108	103	103
	Im.	-143	-68	-26	-18	-18	-11	-9	-7
Impedance (Ω) at LTU	Re.	263	210	192	159	165	159	157	157
	Im.	-205	-122	-75	-30	-34	-16	-13	-12

Table A.11: Loop 5

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		13,9	16,7	18,6	24,4	28,9	33,0	46,1	51,1
Phase (deg)		-160	-290	-545	-1 300	-1 912	-2 512	-4 838	-5 963
Group Delay (μ s)		36,5	35,5	35,4	34,4	33,6	33,5	31,3	30,7
Impedance (Ω) at NTU	Re.	164	144	126	87	67	57	60	79
	Im.	-95	-71	-60	-55	-44	-31	+8	+11
Impedance (Ω) at LTU	Re.	164	144	126	87	67	57	60	79
	Im.	-95	-71	-60	-55	-44	-31	+8	+11

Table A.12: Loop 6

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		12,4	16,1	21,9	31,2	27,0	28,1	35,7	41,4
Phase (deg)		-81	-138	-232	-413	-612	-833	-1 613	-1 977
Group Delay (μ s)		18,5	14,1	12,1	8,3	12,1	12,3	11,6	10,1
Impedance (Ω) at NTU	Re.	124	88	65	49	68	75	68	52
	Im.	-167	-97	-64	-9	0	-19	-18	3
Impedance (Ω) at LTU	Re.	253	188	144	125	124	120	117	117
	Im.	-200	-133	-88	-43	-29	-21	-14	-13

Table A.13: Loop 7

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		14,1	17,7	22,1	28,0	30,6	33,1	45,2	50,9
Phase (deg)		-98	-171	-296	-645	-941	-1 237	-2 391	-2 801
Group Delay (μ s)		22,9	18,4	16,6	16,3	16,3	16,7	15,8	15,5
Impedance (Ω) at NTU	Re.	124	86	57	48	70	96	73	61
	Im.	-182	-109	-65	-4	+16	-14	+2	-17
Impedance (Ω) at LTU	Re.	218	161	133	103	91	81	57	53
	Im.	-218	-135	-90	-59	-53	-49	-31	-21

Annex B (normative): High bit-rate Digital Subscriber Line (HDSL) CAP based system

B.1 Scope and general information

B.1.1 Scope

Annex B describes HDSL systems using CAP (Carrierless Amplitude Phase modulation) for metallic local lines that provide transport for the same applications discussed in the body of the present document. Individual systems transport net bit rates of 1 168 kbit/s or 2 320 kbit/s. Two 1 168 kbit/s systems are used for the support of bit rates at the 2 048 kbit/s hierarchical level for different types of applications associated with this bit rate. Common circuitry for combining and controlling two 1 168 kbit/s HDSL systems is described. One 2 320 kbit/s system supports bit rates at the 2 048 kbit/s hierarchical level.

The requirements for the individual HDSL transmission system, the transmission medium, the transmission performance and the HDSL maintenance and procedures and the mapping for the dedicated applications are defined in annex B. The common circuitry and the HDSL transceivers that form the common core, are defined in the present document. The core is generally independent of applications defined in the present document.

The scope of annex B is in general the same as the scope, clause 1, of the body of the present document. Many provisions in the present document are line-code independent. Such provisions are not repeated in annex B, only a reference to the corresponding provisions in the body of the present document is included.

B.2 References

See clause 2 for references.

B.3 Abbreviations

See clause 3 for abbreviations.

B.4 Reference configuration and functional description

See clause 4 for the reference configuration and functional description. However, annex B focuses on HDSL transmission systems that use only one or two pairs.

The provisions in annex B are aimed at interoperability of equipment from different vendors.

B.5 HDSL core specification

B.5.1 Functions

See subclause 5.1 for functions necessary for the correct operation of the HDSL core.

B.5.2 Transmission medium

See subclause 5.2 for descriptions of the transmission medium, including noise and micro-interruptions. However, for testing CAP-based HDSL systems, additional artificial noise that simulates NEXT is defined in clause B.6 as are requirements, for CAP-based HDSL systems, concerning performance in the presence of, or concerning the susceptibility to, the various impairments associated with the transmission medium.

B.5.3 Transmission method

B.5.3.1 General

See subclause 5.3.1 for general description of the transmission method.

B.5.3.2 Transmission on one pair

Transmission on one DLL is provided by HDSL transceivers operating at 2 320 kbit/s and using the CAP line code in accordance with figure 4 and figures B.2 through B.4 and associated description.

B.5.3.3 Transmission on two pairs

Transmission on two DLLs is provided by two parallel HDSL transceivers, each operating at 1 168 kbit/s and using the CAP line code in accordance with figure 4 and figures B.2 through B.4 and associated description.

B.5.3.4 Transmission on three or four pairs

The transmission of the complete core frame on three or four pairs is not excluded, but is not treated in annex B.

B.5.3.5 Line code

The line code shall be trellis-coded CAP with Tomlinson precoding IEEE Journal on Selected Areas in Communication [24]. Trellis-coded 64-CAP and 128-CAP shall be used for 1 168 kbit/s and 2 320 kbit/s transceivers, respectively. An uncoded 64-CAP signal constellation (signal space diagram) is shown in figure B.1 (the lsb is received first). The uncoded mode is used during "start up" as described in subclause B.5.6. The 2D (2 dimensional) 8-state trellis code IEEE Transactions on Information Theory [23] (without the differential feature) shall be used. Of the 6 bit/symbol of 64-CAP and the 7 bit/symbol of 128-CAP, all bits except one are information bits. One bit of redundancy is added by the 2D 8-state code. Coded 64-CAP and 128-CAP signal constellations (signal space diagrams) are shown in figure B.3 (A) & (B), respectively. For each system, the scrambled data stream to be transmitted is divided into groups, the lsb of which is the first to be received.

The bit stream entering each "H" (HDSL transceiver) block of figures 1 or 2, shall be scrambled as defined in subclause B.5.3.5.2.

B.5.3.5.1 Trellis encoding/decoding

B.5.3.5.1.1 64 point constellation - two pair system

The scrambled data stream to be transmitted is divided into groups of 5 consecutive bits (lsb received first) each to be transmitted in a symbol. As shown in figure B.2, the first two bits of a group, $I1_n$ and $I2_n$, where n designates the sequence number of the group and $I1_n$ is the lsb are input to a systematic convolutional encoder. It generates redundant bit $Y0_n$. This redundant bit, $Y0_n$, and the bits $I1_n$, through $I5_n$ become bits designated $Z0_n$ through $Z5_n$. These bits are fed into the 64-state, bit-to-symbol-mapping function. Each group of bits maps to a point in the signal constellation shown in figure B.3 (A). The trellis is shown in figure B.4.

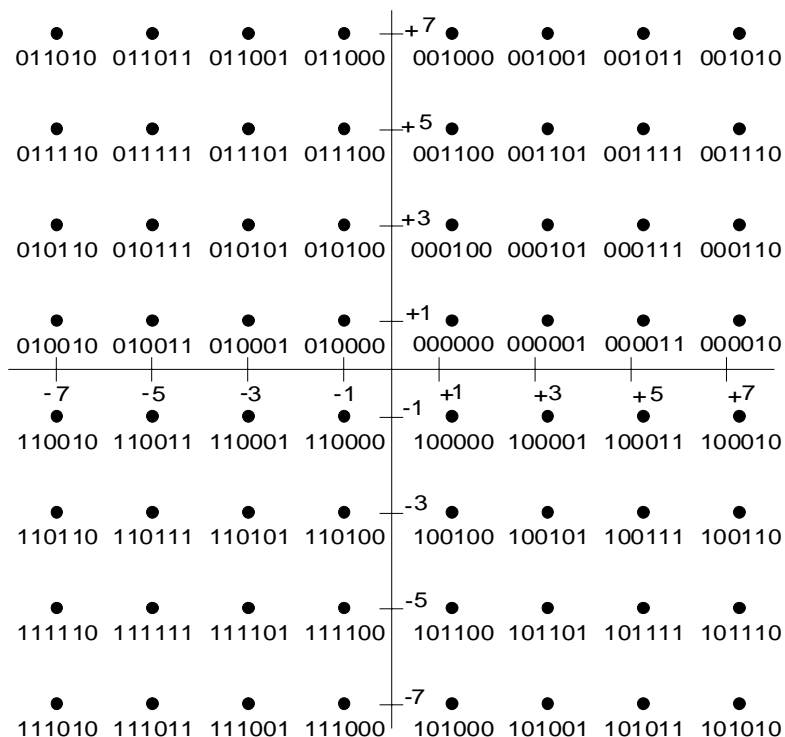


Figure B.1: Uncoded 64-CAP signal constellation (code point designations are Z0 to Z5)

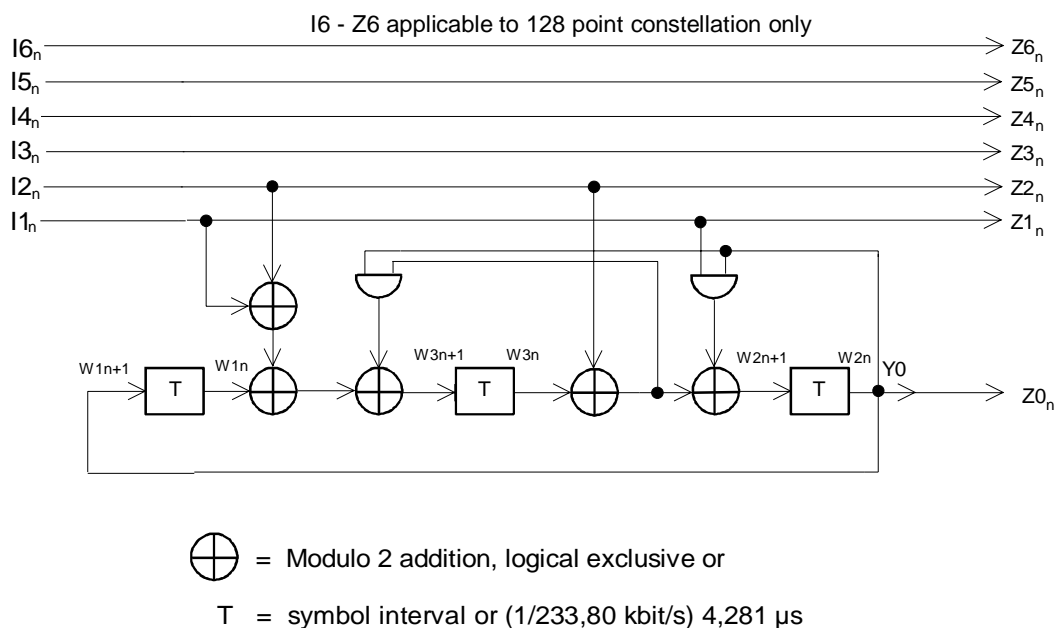
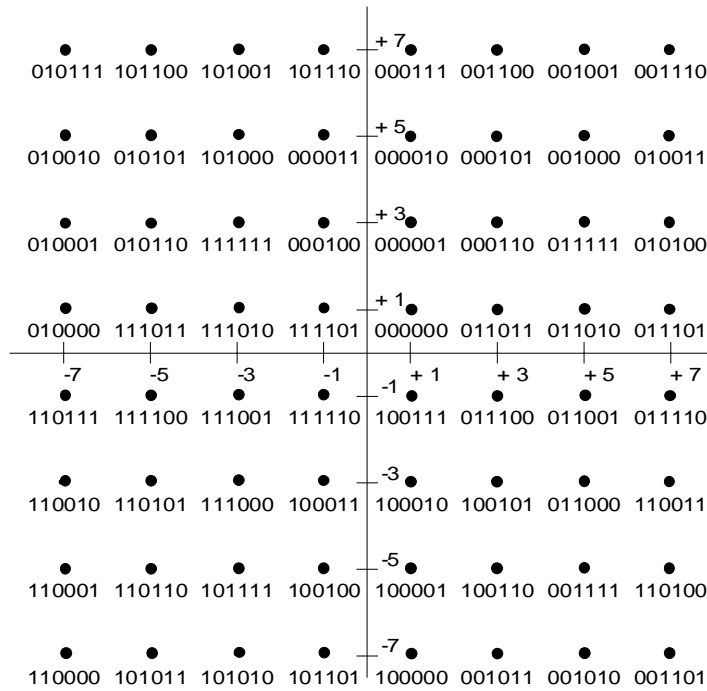


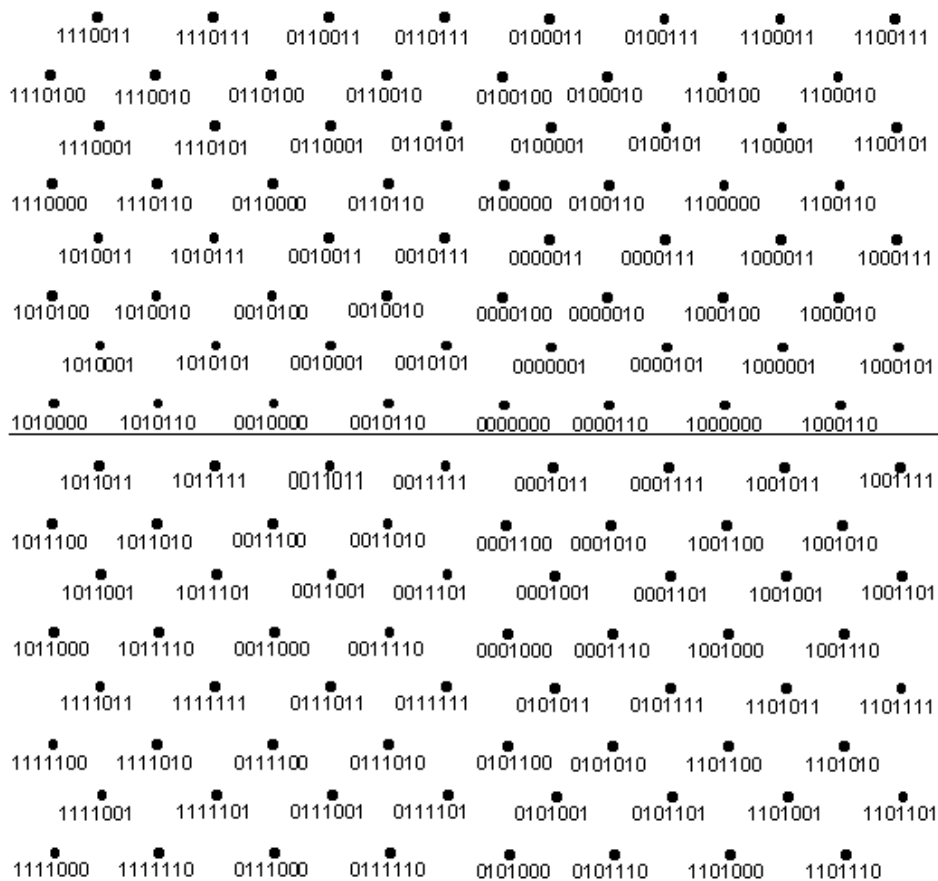
Figure B.2: 2D 8-state trellis encoder

B.5.3.5.1.2 128 point constellation - one pair system

The scrambled data stream to be transmitted is divided into groups of 6 consecutive bits (lsb received first) each to be transmitted in a symbol. As shown in figure B.2, the first two bits of a group, $I1_n$ and $I2_n$, where n designates the sequence number of the group and $I1_n$ is the lsb are input to a systematic convolutional encoder. It generates redundant bit $Y0_n$. This redundant bit, $Y0_n$, and the bits $I1_n$, through $I6_n$ become bits designated $Z0_n$ through $Z6_n$. These bits are fed into the 128-state, bit-to-symbol-mapping function. Each group of bits map to a point in the signal constellation shown in figure B.3 (B). The trellis is shown in figure B.4.



(A) Coded 64-CAP constellation (code point designations are Z5 to Z0).



(B) Coded 128-CAP constellation (code point designations are Z6 to Z0).

Figure B.3: Signal constellations with Trellis coding

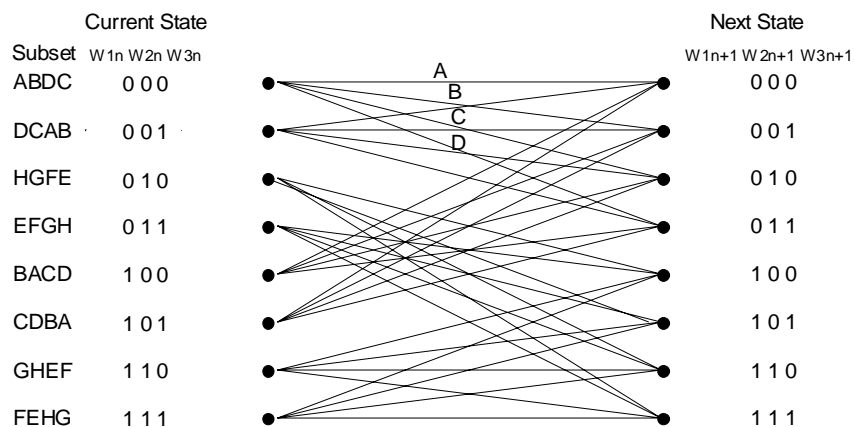


Figure B.4: Trellis diagram of 2D 8-state code

B.5.3.5.2 Scrambling method

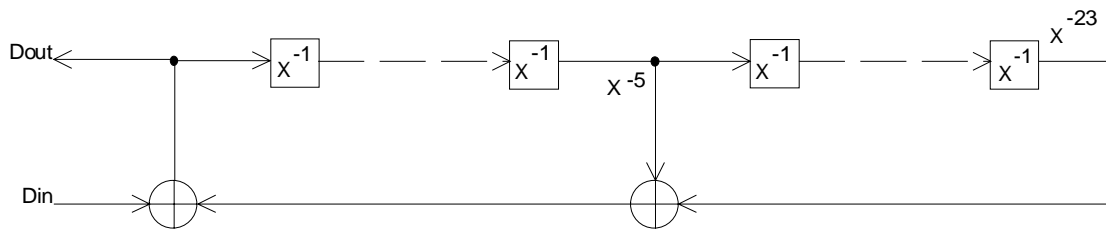
The scrambler/descrambler, included in each transceiver, shall be different in the two directions of transmission. The generating polynomials shall be as follows:

- customer premises transceiver (NTU) = $1 \oplus x^{-18} \oplus x^{-23}$;
- exchange transceiver (LTU) = $1 \oplus x^{-5} \oplus x^{-23}$.

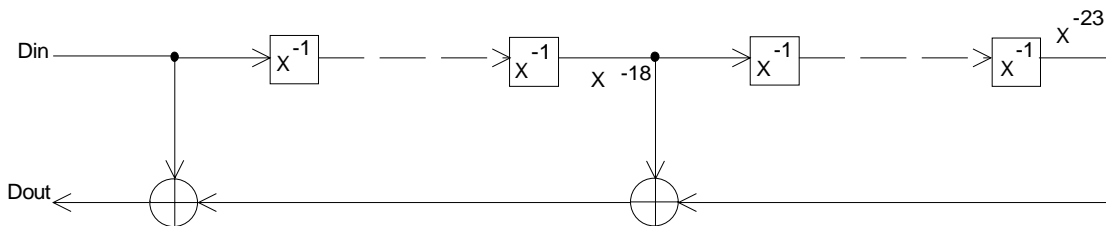
The scramblers and descramblers are shown in figure B.5 as they operate during start up: the self-synchronizing mode. At the transmitter, the scrambler shall effectively divide (modulo 2) the bits sequence by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence that appears at the output of the data scrambler. At the receiver, the received bit sequence shall be multiplied (modulo 2) by the polynomial to recover the original bit stream.

During data transfer the scramblers are locked and the scrambled sequence is added (modulo 2) at the transmitter and subtracted (modulo 2) at the receiver as indicated in figure B.6. As explained in subclause B.5.6.5.4, the transfer from the self synchronizing mode to the locked mode occurs with the transmit data being all ONES and the transfer to locked mode does not require synchronization of the transfer at the two ends.

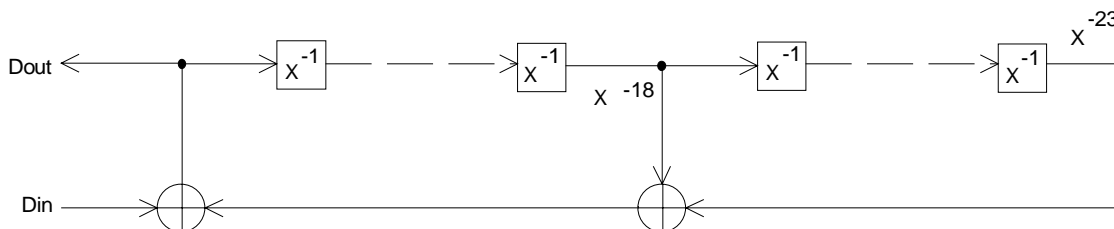
All bits in the HDSL frame, including overhead, sync word and stuffing bits, are scrambled.



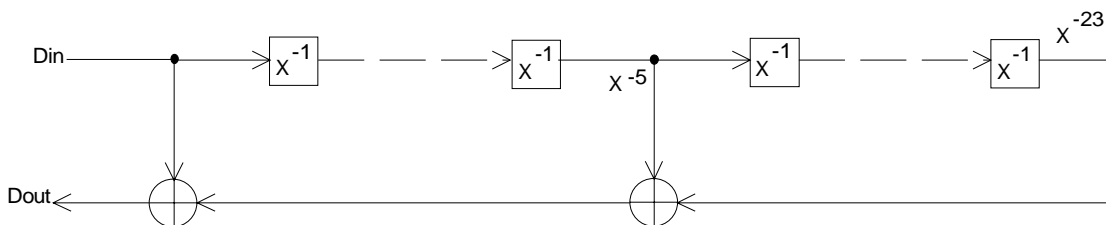
(a) *LTU transmit scrambler*



(b) *LTU receive descrambler*



(c) *NTU transmit scrambler*



(d) *NTU receive descrambler*

Figure B.5: CAP HDSL scrambler/descrambler start-up mode

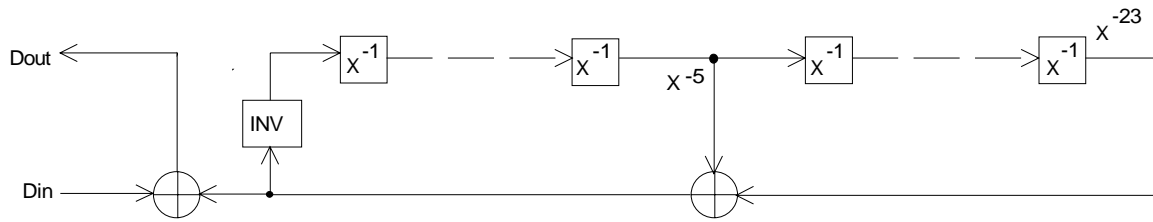
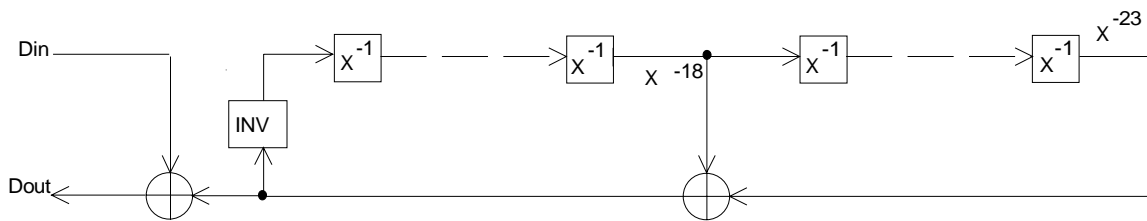
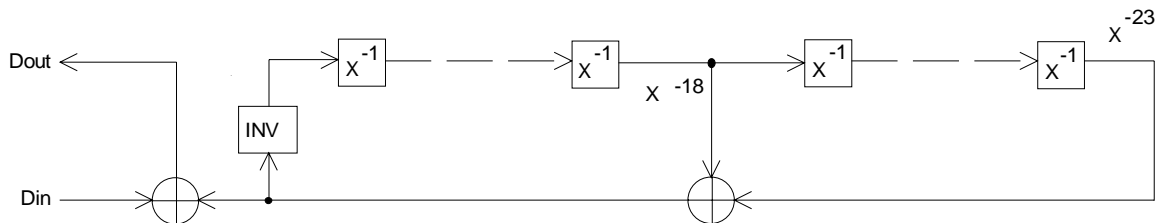
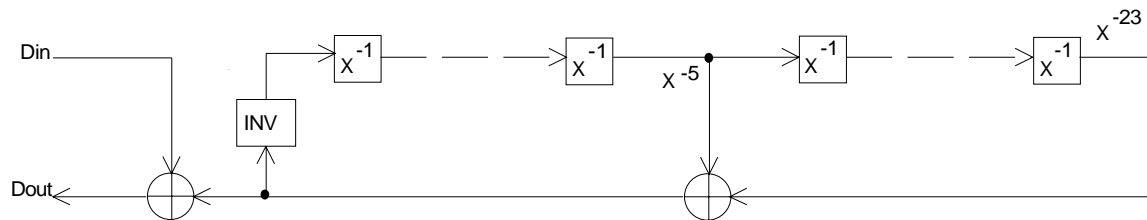
(a) *LTU transmit scrambler*(b) *LTU receive descrambler*(c) *NTU transmit scrambler*(d) *NTU receive descrambler*

Figure B.6: CAP HDSL scrambler/descrambler - data mode

B.5.3.6 Line symbol rate

The symbol rate shall be in the range of:

- 1 168 kbit/s transceiver: 233,60 kbaud \pm 110 ppm;
- 2 320 kbit/s transceiver: 386,667 kbaud \pm 90 ppm.

B.5.4 Frame structure

B.5.4.1 Core frame

See subclause 5.4.1 for a description of the core frame.

B.5.4.2 HDSL frame

This subclause describes the proposed HDSL frame structure in the binary format before scrambling and encoding. This structure is valid during normal operation after symbol timing synchronization, frame alignment and after all internal transceiver coefficients have stabilized sufficiently to permit a reliable transport of the signals through the HDSL transceiver systems. Except for the provision of stuffing 'bits' and the 14 'bit' sync word, the frame is the same as described in subclause 5.4.2.

- The nominal HDSL frame length is 6 ms.
- The mean length of the HDSL frame for the two pair system is 7 008 bits in 6 ms. But each individual frame contains either 0, 1 or 2 stuffing bit pairs, which gives a real length of 7 006 bits in $6 - 1/584$ ms, 7 008 bits in 6 ms, or 7 010 bits in $6 + 1/584$ ms.
- The mean length of the HDSL frame for the one pair system is 13 920 bits in 6 ms. But each individual frame contains either 0, 1, or 2 stuffing bit pairs, which gives a real length of 13 918 bits in $6 - 2/2\ 320$ ms or 13 922 bits in $6 + 2/2\ 320$ ms.
- The bit assignment in each HDSL frame in each direction of transmission for all pairs is shown in table B.1 and table 4.
- The HDSL transceiver systems shall each independently accommodate differences in the bit timing of the two directions of transmission or of the application data and the HDSL transceiver system by including none, one or two stuffing bit pairs at the end of the HDSL frame.
- In the LTU, the clock rate of the two different HDSL frames shall be derived from the same source. The location of the sync word, i.e. the start of the HDSL frames in the different pairs shall be synchronized to each other. The maximum differential delay between the start of the frames shall be less than one symbol period, measured at the line interface of each HDSL transceiver.
- The inclusion of stuffing bit pairs, if necessary, for a two pair system, shall be identical for both pairs.

B.5.4.2.1 HDSL frame structure

B.5.4.2.1.1 Frame structure for two pair system

Figure B.7 illustrates the HDSL frame structure for two pair systems, which is composed of framing bits and bytes and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the 14 bits long synchronization word followed by two HDSL overhead bits and 12 blocks of HDSL payload, each consisting of 145 bits, containing one overhead-bit Z_{mn} and eighteen bytes of the core frame. The Z_{mn} -bits ($m = 1,2$ indicates bits on one of the two pairs; $n = 1$ to 48 is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which 48 bits per frame of each HDSL transceiver system at a capacity of 8 kbit/s are available.

The first eight Z-bits (Z_{m1} to Z_{m8}) are reserved for core applications and presently set to ONE.

The Z-bits 9 to 48 (Z_{m9} to Z_{m48}) are application dependent and are transparently transported through the core. The use of these bits is described in clause 7 for the application specific requirements. Unused bits shall be set to ONE.

The three groups following the first group have an equal structure. Each consists of ten HDSL overhead bits and 12 HDSL payload blocks as described above. So one frame contains a synchronization word, 32 HDSL overhead bits, 48 Z-bits and 864 bytes of the core frame.

Provision is included at the end of the frame for the possibility of 4 stuffing bits. One stuffing bit pair is normally included. This bit pair may be deleted or one additional stuffing bit pair may be inserted, depending on the relation of the timing. The algorithm for determining whether to add or delete stuffing bit pairs shall provide a window of at least 2 unit intervals (at the 2 048 kbit/s rate), in the relative phase of the HDSL and 2 048 kbit/s sequences, within which the stuffing bits will neither be added nor deleted. The length of the HDSL frame is nominally 7 008 bits or 6 ms (for the nominal HDSL clock frequency), or either 7 010 bits, which equals $6 + 2/168$ ms or 7 006 bits corresponding to $6 - 2/168$ ms. The receiver is able to evaluate the length of an incoming frame by detection of the sync word in the following frame and to adjust the demultiplexing of the data stream.

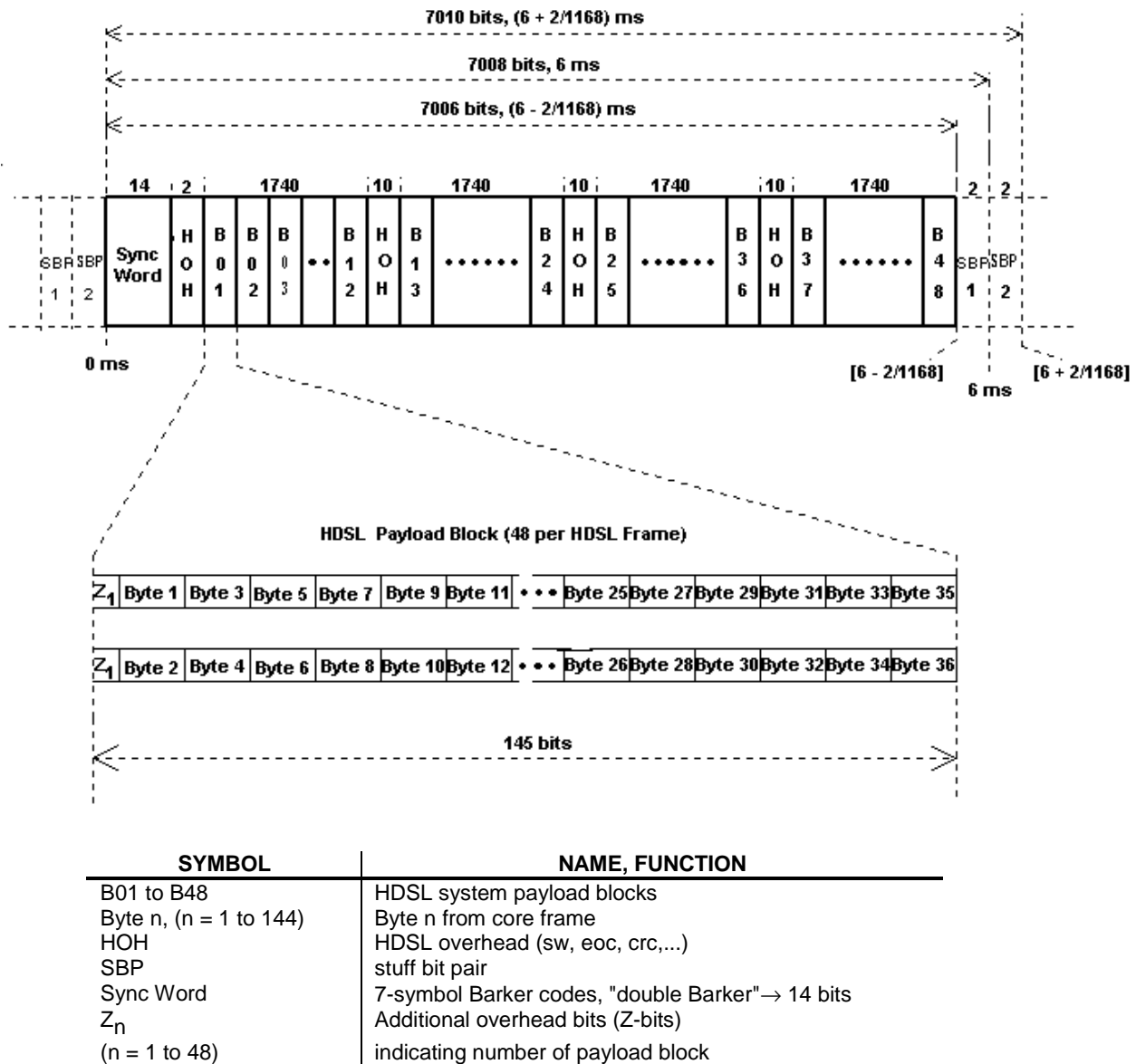


Figure B.7: HDSL two pair system frame structure

B.5.4.2.1.2 Frame structure for one pair system

Figure B.8 illustrates the HDSL frame structure and shows the mapping of the core frame bytes to it. As for the two pair structure, the frame is subdivided into four groups. The first group of the frame starts with the 14 bits long synchronization word followed by two HDSL overhead bits and 12 blocks of HDSL payload, each consisting of 289 bits, containing one overhead bit Z_n and 36 bytes of the core frame. The Z_n-bits (n = 1 to 48 is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which 48 bits of each HDSL frame, a capacity of 8 kbit/s, are available.

The first eight Z-bits (Z₁ to Z₈) are reserved for core applications and presently set to ONE.

The Z-bits 9 to 48 (Z_9 to Z_{48}) are application dependent and are transparently transported through the core. The use of these bits is described in clause 7 for the application specific requirements. Unused bits shall be set to ONE.

The three groups, following the first group, have an equal structure. Each consists of ten HDSL overhead bits and 12 HDSL payload blocks as described above. So one frame contains a synchronization word, 32 HDSL overhead bits, 48 Z-bits and 1 728 bytes of the core frame.

Provision is included at the end of the frame for the possibility of 4 stuffing bits. One stuffing bit pair is normally included. This bit pair may be deleted or one additional stuffing bit pair may be inserted, depending on the relation of the phase of the input bit stream and the transceiver clock. The algorithm for determining whether to add or delete stuffing bit pairs shall provide a window of at least 2 unit intervals (at the 2 048 kbit/s rate), in the relative phase of the HDSL and 2 048 kbit/s sequences, within which the stuffing bits will neither be added nor deleted. The length of the HDSL frame is nominally 13 920 bits or 6 ms (for the nominal HDSL clock frequency), or either 13 922 bits, which equals $6 + 2/2\,320$ ms or 13 918 bits corresponding to $6 - 2/2\,320$ ms. The receiver is able to evaluate the length of an incoming frame by detection of the sync word in the following frame and to adjust the demultiplexing of the data stream.

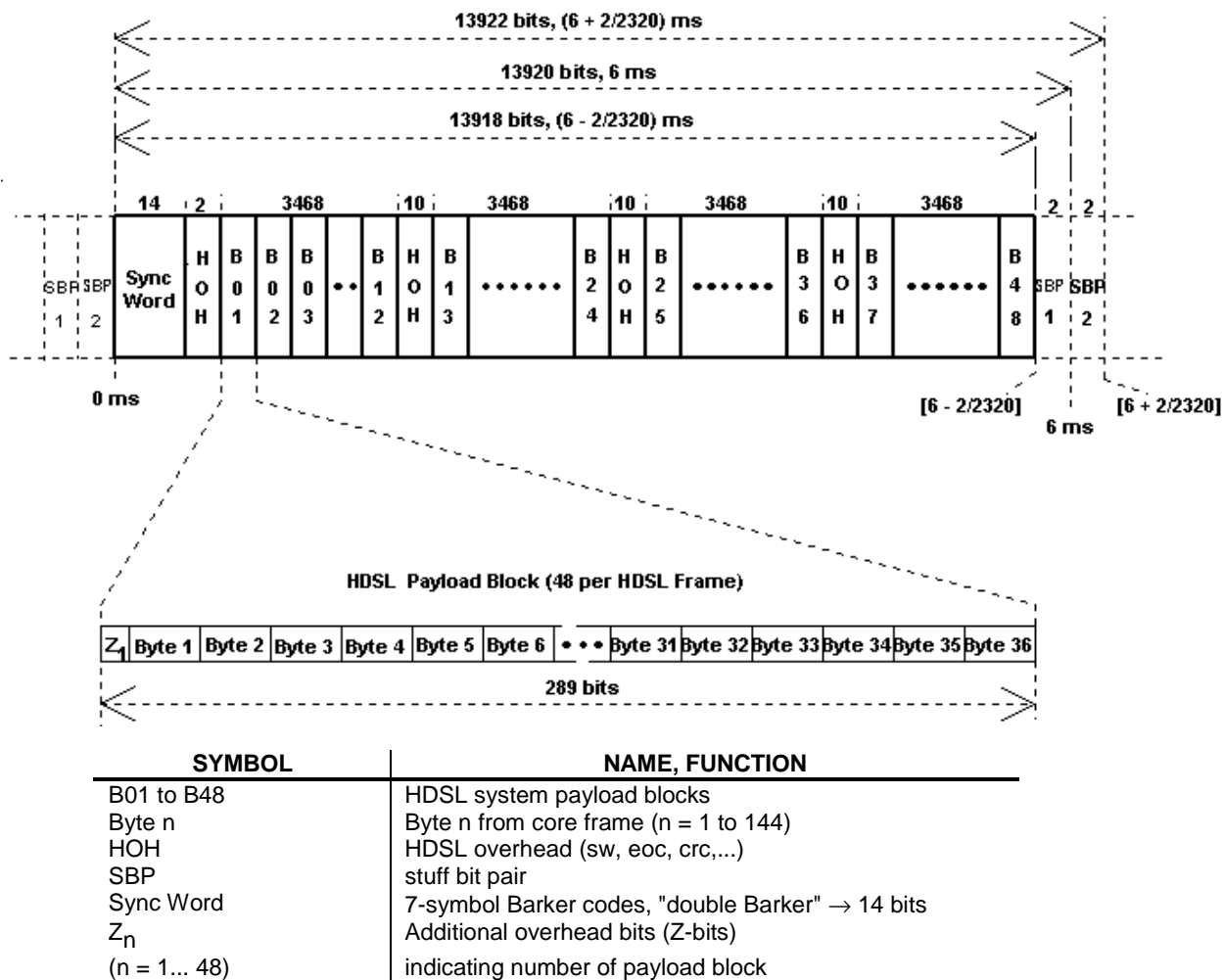


Figure B.8: HDSL one pair system frame structure

B.5.4.2.2 HDSL frame bit assignments

Table B.1 and table 2 (in the main body of the present document) present the bit sequences of the HDSL frames prior to scrambling at the transmit and after descrambling at the receive side. While the frame structures are identical in both directions of transmission, the functional assignments of individual bits in the direction LTU to NTU or NTU to LTU are different. Unused bits in either direction are set to ONE. For example the proposed NTU power status bits are defined only in the frame transmitted towards the LTU and the corresponding bit positions in the reverse direction have no assignment. The bit assignments are identical for each of the pairs. The bit assignments in table B.1 are nearly the same as in table 4 and most of the bit descriptions given in subclause 5.4.2.2 are applicable.

The following are brief descriptions of the currently defined overhead bits that are different from those defined in subclause 5.4.2.2:

- stb (stuffing bit pairs; stb_{1a}, stb_{1b} and stb_{2a}, stb_{2b}).

These bits are always used in pairs. This means either none, two (stb_{1a&b}) or four (stb_{1a&b} and stb_{2a&b}) stuffing bits are inserted, depending on the relation of the phase of the input bit stream and the bit clock synchronized to the transceiver(s). There should be a relative phase range of ± 2 bit intervals during which two stuffing bits (stb_{1a&b}) are transmitted.

Table B.1: HDSL two pair system frame structure

Time	Frame bit #	HOH bit #	Abbreviated name	Full name	Notes
0 ms	1 to 14	1 to 14	SW 1 to 14	Sync Word	Double Barker Code
	15	15	losd	loss of input signal at the far end applications interface	
	16	16	febe	far end block error	
	17 to 1 756	-----	B01 to B12	Payload Block 1 to 12	HDSL payload including Zm ₁ to Zm ₁₂
	1 757	17	eoc01	eoc address	
	1 758	18	eoc02	eoc address	
	1 759	19	eoc03	eoc data/opcode	
	1 760	20	eoc04	eoc odd/even byte	
	1 761	21	crc 1	cyclic redundancy check	CRC-6
	1 762	22	crc 2	cyclic redundancy check	CRC-6
	1 763	23	ps1	NTU power status bit 1	NTU → LTU only
	1 764	24	ps2	NTU power status bit 2	NTU → LTU only
	1 765	25	bpv	bipolar violation	
	1 766	26	eoc05	eoc unspecified	
	1 767 to 3 506	-----	B13 to B24	Payload Blocks 13 to 24	HDSL Payload including Zm ₁₃ to Zm ₂₄
	3 507	27	eoc06	eoc message bit 1	
	3 508	28	eoc07	eoc message bit 2	
	3 509	29	eoc08	eoc message bit 3	
	3 510	30	eoc09	eoc message bit 4	
	3 511	31	crc3	cyclic redundancy check	CRC-6
	3 512	32	crc4	cyclic redundancy check	CRC-6
	3 513	33	hrp	regenerator present	LTU ← REG → NTU
	3 514	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	3 515	35	rcbe	regenerator central block error	LTU ← REG → NTU
	3 516	36	repa	regenerator alarm	
	3 517 to 5 256	-----	B25 to B36	Payload Blocks 25 to 36	HDSL Payload including Zm ₂₅ to Zm ₃₆
	5 257	37	eoc10	eoc message bit 5	
	5 258	38	eoc11	eoc message bit 6	
	5 259	39	eoc12	eoc message bit 7	

Time	Frame bit #	HOH bit #	Abbreviated name	Full name	Notes
	5 260	40	eoc13	eoc message bit 8	
	5 261	41	crc5	cyclic redundancy check	CRC-6
	5 262	42	crc6	cyclic redundancy check	CRC-6
	5 263	43	rta	remote terminal alarm	NTU → LTU only
	5 264	44	indc/indr	ready to receive	indc=LTU → NTU indr=NTU → LTU
	5 265	45	uib	unspecified indicator bit	
	5 266	46	uib	unspecified indicator bit	
6 - 2/1 168 ms	5 267 to 7 006	-----	B37 to B48	Payload Blocks 37 to 48	HDSL Payload including Zm ₃₇ to Zm ₄₈
	7 007	47	stb1a	stuff bit 1a	Frame Stuffing
6 ms nominal	7 008	48	stb1b	stuff bit 1b	Frame Stuffing
	7 009	49	stb2a	stuff bit 2a	Frame Stuffing
6 + 2/1 168 ms	7 010	50	stb2b	stuff bit 2b	Frame Stuffing

Table B.2: HDSL one pair system frame structure

Time	Frame bit #	HOH bit #	Abbreviated name	Full name	Notes
0 ms	1 to 14	1 to 14	SW 1 to 14	Sync Word	Double Barker Code
	15	15	losd	loss of input signal at the far end applications interface	
	16	16	febe	far end block error	
	17 to 3 484	-----	B01 to B12	Payload Block 1 to 12	HDSL payload including Zm ₁ to Zm ₁₂
	3 485	17	eoc01	eoc address	
	3 486	18	eoc02	eoc address	
	3 487	19	eoc03	eoc data/opcode	
	3 488	20	eoc04	eoc odd/even byte	
	3 489	21	crc 1	cyclic redundancy check	CRC-6
	3 490	22	crc 2	cyclic redundancy check	CRC-6
	3 3491	23	ps1	NTU power status bit 1	NTU → LTU only
	3 492	24	ps2	NTU power status bit 2	NTU → LTU only
	3 493	25	bpv	bipolar violation	
	3 494	26	eoc05	eoc unspecified	
	3 495 to 6 962	-----	B13 to B24	Payload Blocks 13 to 24	HDSL Payload including Zm ₁₃ to Zm ₂₄
	6 963	27	eoc06	eoc message bit 1	
	6 964	28	eoc07	eoc message bit 2	
	6 965	29	eoc08	eoc message bit 3	
	6 966	30	eoc09	eoc message bit 4	
	6 967	31	crc3	cyclic redundancy check	CRC-6
	6 968	32	crc4	cyclic redundancy check	CRC-6
	6 969	33	hrp	regenerator present	LTU ← REG → NTU
	6 970-	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	6 971	35	rcbe	regenerator central block error	LTU ← REG → NTU
	6 972	36	repa	regenerator alarm	
	6 973 to 10 440	-----	B25 to B36	Payload Blocks 25 to 36	HDSL Payload including Zm ₂₅ to Zm ₃₆
	10 441	37	eoc10	eoc message bit 5	
	10 442	38	eoc11	eoc message bit 6	
	10 443	39	eoc12	eoc message bit 7	
	10 444	40	eoc13	eoc message bit 8	

Time	Frame bit #	HOH bit #	Abbreviated name	Full name	Notes
	10 445	41	crc5	cyclic redundancy check	CRC-6
	10 446	42	crc6	cyclic redundancy check	CRC-6
	10 447	43	rta	remote terminal alarm	NTU → LTU only
	10 448	44	indc/indr	ready to receive	indc=LTU → NTU indr=NTU → LTU
	10 449	45	uib	unspecified indicator bit	
	10 450	46	uib	unspecified indicator bit	
6 - 2/2 320 ms	10 451 to 13 918	-----	B37 to B48	Payload Blocks 37 to 48	HDSL Payload including Zm ₃₇ to Zm ₄₈
	13 919	47	stb1a	stuff bit 1a	Frame Stuffing
6 ms nominal	13 920	48	stb1b	stuff bit 1b	Frame Stuffing
	13 921	49	stb2a	stuff bit 2a	Frame Stuffing
6 + 2/2 320 ms	13 922	50	stb2b	stuff bit 2b	Frame Stuffing

B.5.5 HDSL embedded operations channel (eoc)

See subclause 5.5 for requirements for the embedded operations channel. The only departure from the description in subclause 5.5 is the use of the term Signal Quality (SQ) in annex B instead of "noise margin", (see subclause 5.5.7). SQ more accurately describes the measurement involved.

B.5.5.1 Signal Quality (SQ)

The requirements in this subclause are the same as in subclause 5.5.7 except that the measurement referred to here is SQ. The purpose of SQ is the same as that for noise margin in subclause 5.5.7.

B.5.6 Start-up procedure

B.5.6.1 General

B.5.6.1.1 Start-up

See subclause 5.6.1.1 for a description of start-up.

B.5.6.1.2 Activation of HDSL transceiver pairs

See subclause 5.6.1.2 for activation of HDSL transceiver pairs.

B.5.6.1.3 Transparency

Prior to the completion of activation, transmission is not transparent, the signals that are present at the line interfaces of the HDSL transceivers are special start-up patterns generated by the HDSL transceivers. Each HDSL transceiver shall provide transparent transmission of data to the core function after the termination of the individual activation procedure. The output signal of receivers that have not yet entered the Active-Rx State, as defined in subclauses B.5.6.7.1 and B.5.6.7.2, shall be set to all ONES.

The operational status is determined by the application.

NOTE: Transceivers in a REG are at no time fully transparent in so far as some HOH-bits will be overwritten.

B.5.6.1.4 Signal quality (SQ)

The SQ is estimated at the receivers of LTU, NTU and REG (if provided). This value is used to estimate the bit error ratio (BER) of the received data. It takes into account the signal to interference ratio (SIR), where interference includes noise and residual echo and distortion.

SQ has the same significance as "noise margin" defined in subclause 5.6.1.4.

B.5.6.2 Control and status signals

See subclause 5.6.2 for definitions of virtual control and status signals involved in the loop activation procedure. Departures from these definitions are as follows:

- for LOSW refer to figure B.20;
- for INDC and INDR, the term noise margin should be replaced by signal quality.

B.5.6.3 Transmitted signals

The following is the description of the transmitted signals during loop activation.

B.5.6.3.1 Silent

No signal is transmitted to the line during this state.

B.5.6.3.2 S0 signal

The S0 signal is used by the LTU for transceiver alerting ("wake up") and a time stamp sequence. It is used by the NTU transceivers for indicating that the NTU transceiver has detected S0 and is ready to proceed with start up. S0 transmitted from the LTU is referred to as CS0 and as RS0 from the NTU. Both CS0 and RS0 are 3 150 symbols in length. S0 is a 2-point, in-phase, pseudo-noise sequence. The sequence uses the generating polynomial $1 \oplus x^{-5} \oplus x^{-6}$ seeded with bits [0, 1, 2, 3, 4, 5] = 000001; i.e. the sequence is initiated with all stages of the pseudo random sequence generator set to ZERO except the most significant stage which is set to ONE. The sequence generator is driven with all ONES. The sequence is transmitted at the corresponding symbol rate used in the data mode (233,60 kbaud for 1 168 kbit/s transceivers and 386,667 kbaud for 2 320 kbit/s transceivers). The bit to symbol mapping for the S0 is given in table B.3.

Table B.3: S0 bit-to-symbol in-phase mapping

Bit	Symbol
0	-A
1	+A

NOTE: A is the amplitude corresponding to the required transmit power (see subclauses B.5.6.5.1 and B.5.8.4.1).

B.5.6.3.3 S1 signal

The S1 signal is an uncoded 64-CAP signal transmitted at full power. It uses the generating polynomial $1 \oplus x^{-5} \oplus x^{-23}$ in the direction from LTU to the NTU is referred to as CS1. It uses the generating polynomial $1 \oplus x^{-18} \oplus x^{-23}$ in the direction from the NTU to the LTU and is referred to as RS1. The generating polynomials are implemented using the self synchronizing scrambler mode illustrated in figure B.6 with an all ONES input. The uncoded CAP signal constellation is shown in figure B.1.

B.5.6.3.4 S2 signal

The S2 signal is a coded 64-CAP signal transmitted at full power (see subclause B.5.8.4.1). It uses the generating polynomial $1 \oplus x^{-5} \oplus x^{-23}$ in the direction from the LTU to the NTU is referred to as CS2. It uses the generating polynomial $1 \oplus x^{-18} \oplus x^{-23}$ in the direction from the NTU to the LTU and is referred to as RS2. The generating

polynomials are implemented using the self synchronizing scramblers mode illustrated in figure B.5 with an all ONES input. The coded CAP signal constellations are shown in figure B.3.

B.5.6.3.5 S3 signal

The S3 signal is a coded 64-CAP signal that includes framing and is transmitted at full power. It uses the generating polynomial $1 \oplus x^{-5} \oplus x^{-23}$ in the direction from the LTU to the NTU is referred to as CS3. It uses the generating polynomial $1 \oplus x^{-18} \oplus x^{-23}$ in the direction from the NTU to the LTU and is referred to as RS3. The generating polynomials are implemented using the locked scrambler mode illustrated in figure B.6.

B.5.6.4 Timers

The following timers are involved in the loop activation procedure of the HDSL transceiver. The timer values are indicated in table B.4. The timeline of the loop activation sequence is given in figure B.9.

B.5.6.4.1 T1

T1 is the duration of time that an LTU transceiver waits, after the transmission of CS0 for the receipt of RS0 from the corresponding transceiver in an NTU, before, for a two pair transceiver, it initiates the transmission of CS0 to the NTU transceiver on the second channel and, for a one pair transceiver, it retransmits CS0.

B.5.6.4.2 T2

T2 is the duration of time that a two pair LTU waits, before it reverts to the single pair mode of operation, for an RS0 "I'm alerted" response from the transceiver in the NTU after it has sent the CS0 alerting signal to the transceiver, and when it has previously received an RS0 "I'm alerted" response from the other transceiver in the NTU (see figure B.9). It does not revert to the single pair mode of operation unless such mode of operation is enabled.

B.5.6.4.3 T3

T3 is the duration of time that a two pair NTU waits, before it reverts to preparation for the single pair mode of operation, for a CS0 alerting signal to a transceiver after it has sent an RS0 "I'm alerted" signal from its other transceiver. The single pair mode of operation is not established unless such mode of operation of the LTU is enabled.

B.5.6.4.4 T4

T4 is the maximum time that an LTU waits, after the receipt of RS0 from the NTU indicating that it has been alerted, before it initiates the transmission of CS1. (In normal dual channel operation, the timer applies after both transceivers in the NTU have sent RS0 but, in single channel operation (fall-back mode), the timer applies after the transceiver on the channel of interest has sent RS0.)

B.5.6.4.5 T5

T5 is the time an NTU waits for the detection of CS1, as appropriate, after transmitting RS0, before it reverts to the initial alerting mode. For a two pair system, T5 is started only after RS0 is transmitted in response to CS0 in the second channel to be alerted.

B.5.6.4.6 T6

T6 is the maximum time that a transceiver in an NTU requires to detect CS1 and initiate the transmission of RS1 when it first enters the alerted state.

B.5.6.4.7 T7

T7 is the maximum time that an NTU continues to send Silent after it detects the end of the CS1 ideal reference sequence.

B.5.6.4.8 T8

T8 is the time that an LTU transceiver sends Silent following the termination of its transmission of the ideal reference sequence and its detection of RS1 from the NTU transceiver before it initiates the transmission of CS1. The NTU transceiver trains its echo canceller during this interval.

B.5.6.4.9 T9

T9 is the duration of time that a transceiver in an LTU transmits CS1 after the time it detects the RS0 time stamp signal from the transceiver in the NTU before it initiates the Tomlinson coefficient exchange.

B.5.6.4.10 T10

T10 is the maximum time that an NTU transceiver can delay after receiving the Tomlinson coefficients from the LTU transceiver before it initiates transmission of Tomlinson coefficients to the LTU transceiver.

B.5.6.4.11 T11

T11 is the time that an LTU transceiver shall delay after receiving the Tomlinson coefficients from the NTU transceiver before it may lock its descrambler.

B.5.6.4.12 T12

T12 is the time that an NTU transceiver shall delay after completing the transmission of its Tomlinson coefficients before it may lock its descrambler.

B.5.6.4.13 T-Act

The activation timer for the HDSL transceivers (T-Act) is the length of time in which the loop activation procedure in the HDSL transceiver in the LTU or HDSL transceiver in the NTU should have successfully ended, starting from the point in time where the transceiver at the NTU starts to transmit the S1 signal. At the NTU, T-Act starts when transmission of RS1 is initiated and, in the LTU, T-Act starts when the RS1 is detected.

B.5.6.4.14 Timer values

The timer values (in symbol intervals, T) are listed in table B.4:

Table B.4: Timer values for start-up

System	Lower bound (T)		Timer number		Upper bound (T)	LTU/NTU
1P & 2P	2 250	<	T1	<	3 200	NTU & NTU
2P	8 000	<	T2			LTU
1P & 2P	4 000	<	T3	<	6 000	NTU
1P & 2P			T4	<	500	LTU
1P & 2P	1 000	<	T5			NTU
1P & 2P			T6	<	500	NTU
1P & 2P			T7	<	1 000	NTU
1P	35 000	<	T8	<	36 000	LTU
2P	27 000	<	T8	<	28 000	LTU
1P & 2P	575 000	<	T9	<	585 000	LTU
1P & 2P			T10	<	1 000	NTU
1P & 2P	240 000	<	T11	<	250 000	LTU
1P & 2P	240 000	<	T12		250 000	NTU
1P & 2P			T-Act	<	$2,5 \times 10^6$ (2P, 10,7 s & 1P, 6,5 s)	LTU & NTU
NOTE: For 1 168 kbit/s transceivers (2P): T = 1 divided by (1 168 kbit/s divided by 5 bit/symbol) = 4,281 μ s/symbol. For 2 320 kbit/s transceivers (2P): T = 1 divided by (2 320 kbit/s divided by 6 bit/symbol) = 2,5 862 μ s/symbol.						

B.5.6.5 HDSL transceiver activation

The CAP HDSL transceiver start-up procedure is described in this subclause. The complete start-up sequence (for the dual channel mode) is shown in figure B.9.

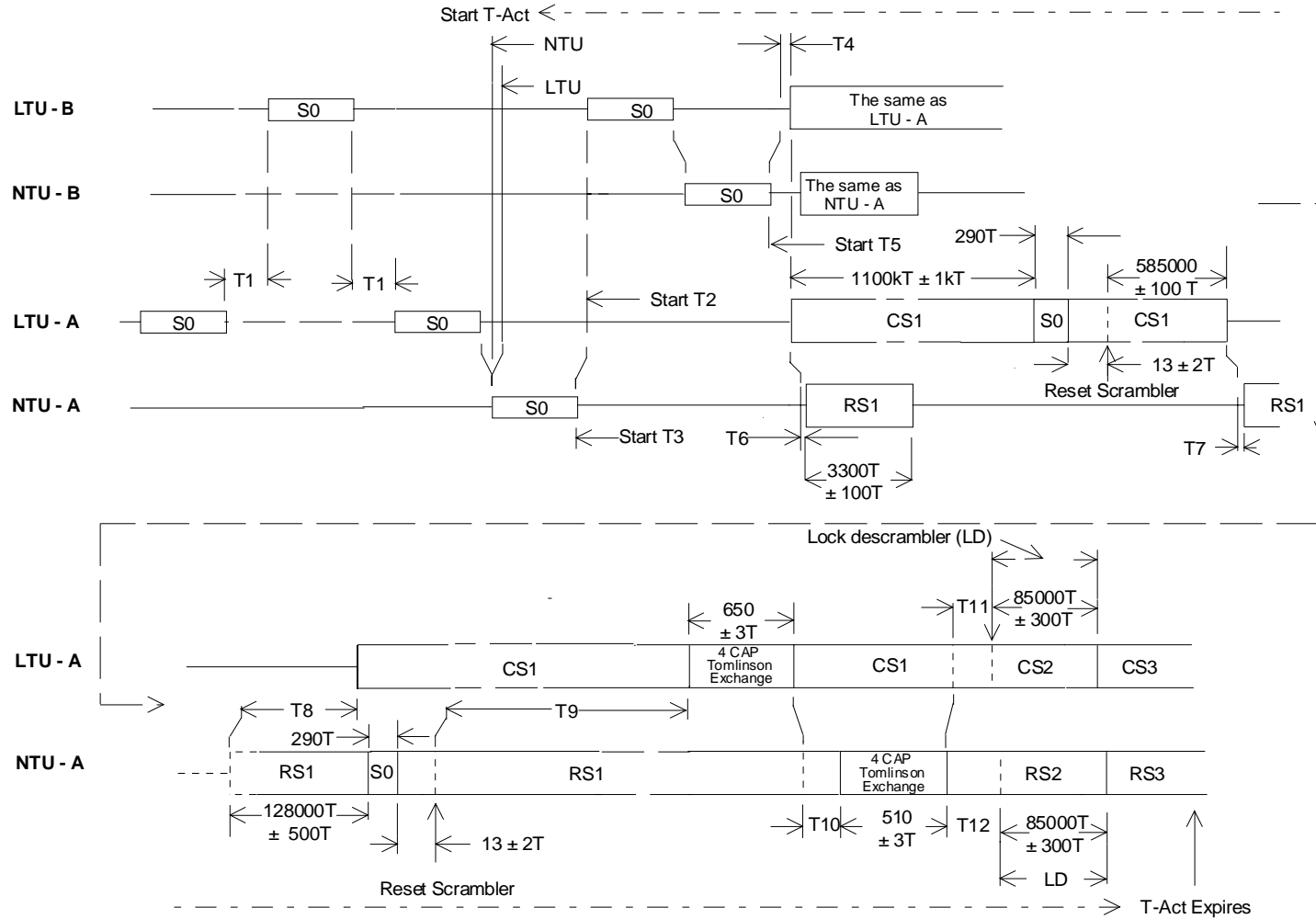


Figure B.9: CAP HDSL Transceiver activation sequences - dual channel mode

B.5.6.5.1 Alerting

B.5.6.5.1.1 Two pair system alerting sequence

B.5.6.5.1.1.1 Alerting in normal dual channel mode

The alerting ("wake up") sequence for both channels A and B is shown in figure B.10.

Alerting is initiated by the HDSL transceiver in the LTU transmitting the CS0 sequence on channel A to alert the corresponding transceiver in the NTU. The HDSL transceiver in the LTU then transmits Silent and monitors for a reply from the NTU. Upon detection of the CS0 sequence, the HDSL transceiver in the NTU replies by transmitting the sequence (RS0). Following the receipt of RS0 in channel A, the LTU transmits CS0 in channel B. The receipt of the sequence RS0 from the NTU transceiver on channel B indicates that the NTU has been alerted and start up procedure continues. Upon the transmission of CS0 in channel B, the NTU starts timer T5 and waits for the receipt of CS1 from the LTU in both channels.

As shown in figure B.10, if no NTU reply is received in response to the transmission of an CS0 sequence for period of T1 symbols, the LTU transceiver repeats the transmission of the CS0 sequence on the other channel in an attempt to alert the associated NTU transceiver. The LTU transceiver alternately transmits the CS0 sequence and Silent, alternatively polling first on the A channel and then on the B channel, until replies are received from both transceivers in the NTU.

If a reply is received from one of the transceivers in the NTU, the LTU continues to alternately transmit the CS0 sequence and Silent to the transceiver on the other channel until it replies or T-Act expires. The LTU proceeds as described in subclause B.5.6.7.2. The single channel mode may then be enabled for the channel that replied and alerting would proceed as described in subclause B.5.6.5.1.1.2. As explained in subclause B.5.6.7, alerting by the LTU is initiated only if ACTREQ is equal to ONE.

When the NTU completes the transmission of the RS0 "I'm alerted" sequence from the first transceiver alerted, it starts timer T3. If the alerting S0 sequence is received from the LTU by the second NTU transceiver before the timer expires, the NTU continues the alerting process for the dual channel mode. The alternative is described in subclause B.5.6.5.1.1.2.

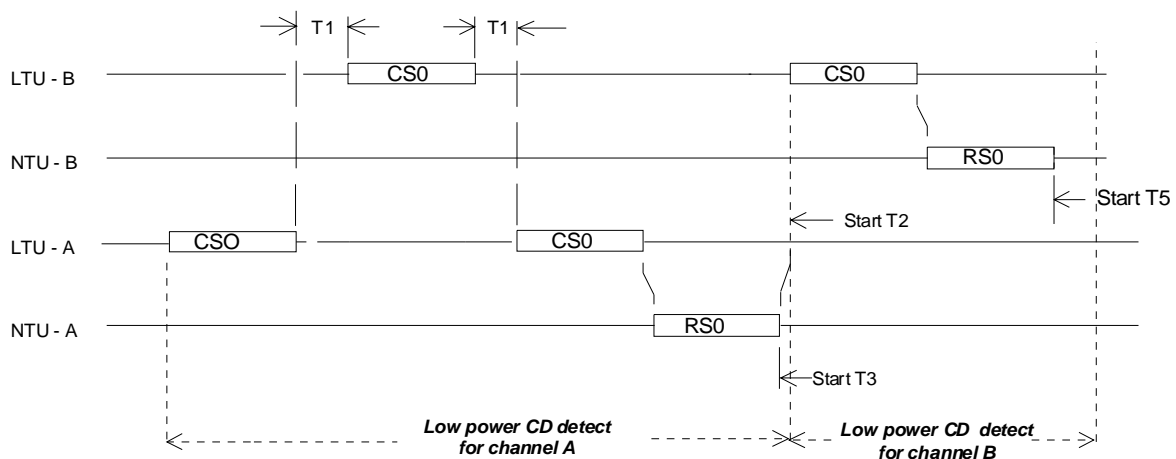


Figure B.10: Alerting sequence for both channels of two pair HDSL transceiver

After receiving a RS0 response, the LTU shall send the corresponding CS0 poll on the other channel as described above.

The LTU continuously polls the NTU transceivers until an RS0 reply is received on both channels or T-Act expires.

The power of the S0 sequences from both the LTU and NTU shall be $-1,5 \text{ dBm} \pm 1 \text{ dB}$ or nominally 15 dB below the high transmit power specified in subclause B.5.8.4.1.

B.5.6.5.1.1.2 Alerting in single channel mode

In the single channel mode of a two pair system, the LTU transceiver on the channel to be activated transmits alternately the CS0 sequence and Silent until it receives a reply from the corresponding NTU transceiver. The sequence is shown in figure B.11.

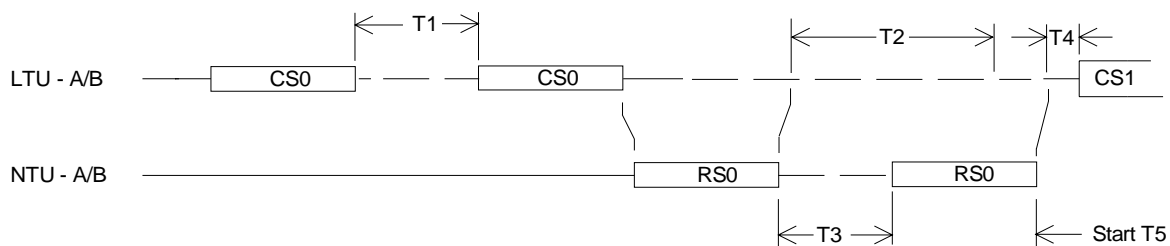


Figure B.11: Alerting sequence for single-channel mode

After the NTU finishes the transmission of the RS0 "I'm alerted" reply, it starts a timer, T3. If no CS0 alerting signal is received by the second transceiver of the NTU before this timer expires, the NTU reverts to activating in the single channel mode and transmits RS0 a second time. In this way, the NTU automatically adopts the single channel mode when such a mode is enabled at the LTU. Activation is completed only if the LTU continues the process by transmitting CS1.

When the LTU receives an RS0 "I'm alerted" reply from the transceiver of the NTU, the LTU starts a timer T2. If the second RS0 is received prior to the time-out of T2 and the LTU wishes to activate the channel in the single channel mode, it continues the activation process as indicated in figure B.11. It delays the initiation of CS1 on the channel until T4 unit intervals after the second RS0 are received. If the second RS0 is not received before timer T2 times out, it may initiate a second attempt to activate the channel by transmitting CS0.

The LTU will activate either channel A or B if the single channel mode of operation is enabled.

B.5.6.5.1.2 One pair transceiver alerting sequence

The alerting sequence for single pair transceivers is essentially the same as for transceivers of two pair systems in the single channel mode. The sequence is shown in figure B.12. The LTU transceiver transmits alternately the CS0 sequence and Silent until it receives a reply from the corresponding NTU transceiver.

After the NTU finishes the transmission of the RS0 "I'm alerted" reply, it starts a timer, T5 and waits for CS1 from the LTU. Upon receiving RS0 from the NTU, the LTU transmits CS1.

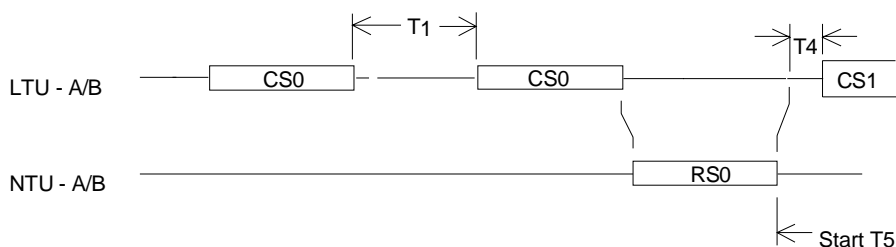


Figure B.12: Alerting sequence for one pair transceiver

B.5.6.5.2 Transmit power mode selection

During alerting, the LTU and NTU transceivers measure the received level of the S0 sequences and choose either the high transmit power (HP) or the low transmit power (LP) mode, which are specified in table B.5 (see also subclause B.5.8.4.1). (The use of the lower transmit power on short lines reduces the required linear range of the receiver). The chosen transmit power modes are maintained during and after activation and are "full power" for the installation. As described in subclause B.5.6.5.6, receivers are informed of the transmit power modes of far end transmitters during the Tomlinson coefficient exchange.

Table B.5: Transmit power mode selection criteria

Power Mode	Line Loss for S0 in dB
HP	> 9
HP or LP	6 to 9
LP	< 6

B.5.6.5.3 Front-end training

Front-end training is initiated after the successful completion of the alerting process. The primary purpose of the front-end training phase is to align any automatic gain control function at the receiver that is ahead of the analogue to digital conversion function. This portion of the start-up sequence is shown in figure B.13.

The LTU transceivers start transmitting CS1 within T_4 symbols after the NTU RS0 alert indication is completed. Transmission continues for a period of $1\ 100\ kT \pm 1\ kT$. Upon receiving this signal, the NTU transceivers initiate transmission of RS1 for a period of $3\ 300\ T \pm 100\ T$. The NTU shall detect and initiate the transmission of RS1 within an interval of T_6 symbols. During the period when a transceiver is transmitting and receiving signals, its front end AGC is trained.

B.5.6.5.4 Timing recovery, echo canceller and equalizer training

This portion of the start-up sequence is shown in figure B.14. After an NTU transceiver stops transmitting RS1, it initiates timing recovery from the CS1 signal received from the LTU transceiver and the LTU transceiver initiates training of its echo canceller.

Following the transmission of CS1, each LTU transceiver transmit CS0 (at full power) as a time stamp signal for a duration of 290 symbols to signal the start of the ideal reference sequence. This alerts the associated NTU transceivers that an ideal reference sequence is about to be transmitted. The ideal reference is initiated by resetting the scrambler 13 ± 1 symbols after CS0 is completed. (The initiation of CS1 may be delayed until the ideal reference signal is initiated or it may be initiated immediately after the completion of CS0 as shown in the figures). The ideal reference sequence is CS1 synchronized with the symbol clock in a defined way; thereby providing a defined pseudo random sequence of symbols. The ideal reference CS1 sequence is initiated with the generator seeded with bits $[0, 1, 2, 3, \text{to}, 23] = 0000-0$; i.e. the sequence is initiated with all stages of the pseudo random sequence generator set to ZERO. The generator is driven with all ONES. The sequence starts with a symbol and the time stamp sequence identifies this starting point at the receiver. The sequence is continued for a period of $585\ 000 \pm 100$ symbols.

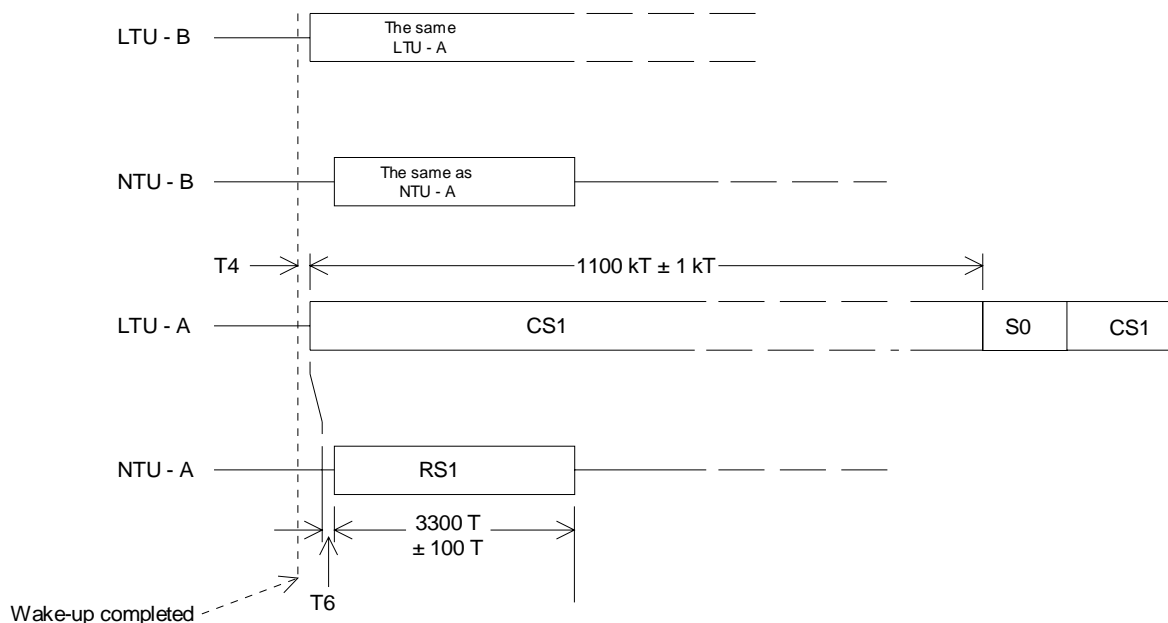


Figure B.13: Start-up sequence - analogue front end training

Upon receiving the ideal reference sequence, the NTU transceivers initiate training of its equalizer. The receiver knows the sequence transmitted and the synchronization of the sequence with its symbol clock and therefore it knows the point in the 64-CAP constellation of each received symbol.

After the LTU transceiver completes transmission of CS1, the NTU transceiver transmits RS1 (but not as an ideal reference) for a period of $128\,000 \pm 500$ symbols. The LTU transceiver is silent for a period T_8 symbol intervals. During this period, while the NTU transceiver is transmitting in the absence of a received signal, the NTU trains its echo canceller. This portion of the start-up sequence is shown in figure B.15. As shown in figure B.15, the LTU transceiver initiates transmission of CS1 after T_8 silent interval.

Once the NTU transceiver has completed transmission of RS1, the NTU transceiver transmits S_0 , for a period of 290 symbols at full power, as a time stamp signal. This signals the beginning of the transmission of the ideal reference sequence by the NTU transceiver having all of the characteristics described above. (As described above for the LTU, the initiation of the CS1 sequence may immediately follow the transmission of CS0 for 290 symbols, as shown in the figures, or it may be delayed until the scrambler is reset). While it is receiving the ideal reference sequence, the LTU transceiver trains its equalizer.

The NTU transceiver shall maintain timing such that it is in synchronization after the interval during which the LTU transceiver is silent.

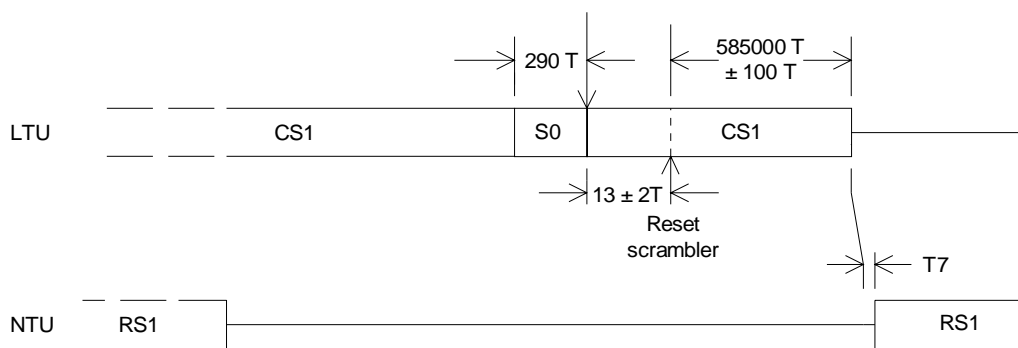


Figure B.14: NTU ideal reference training sequence

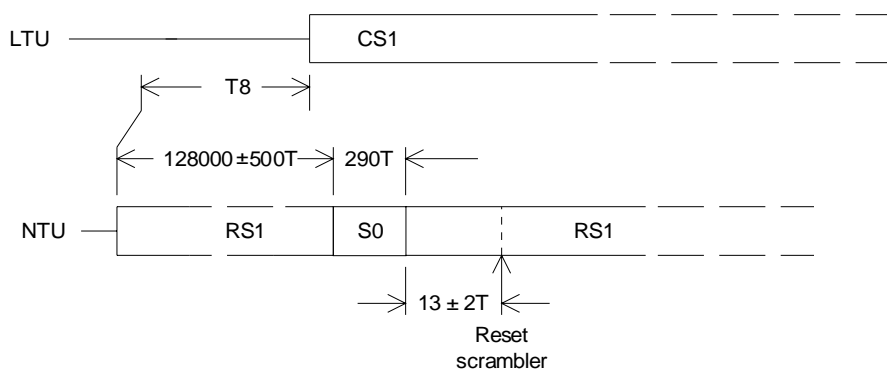


Figure B.15: LTU ideal reference sequence training

B.5.6.5.5 Tomlinson coefficient exchange

After the LTU transceiver has received RS1 for an interval T_9 , the LTU transceiver transmits the decision feedback equalizer coefficients for the Tomlinson precoder for a period of 650 symbols as indicated in figure B.16. Once the LTU transceiver has completed transmission of the Tomlinson coefficients, it continues the transmission of CS1. After the NTU transceiver completes the reception of the Tomlinson coefficients, it transmits its coefficients for a period of 510 symbols. The NTU transceiver may delay transmission of its coefficients by up to T_{10} symbols. The Tomlinson coefficients are the coefficients of the feedback filter in the Tomlinson precoder IEEE Transactions Journal on Selected Areas in Communication [24].

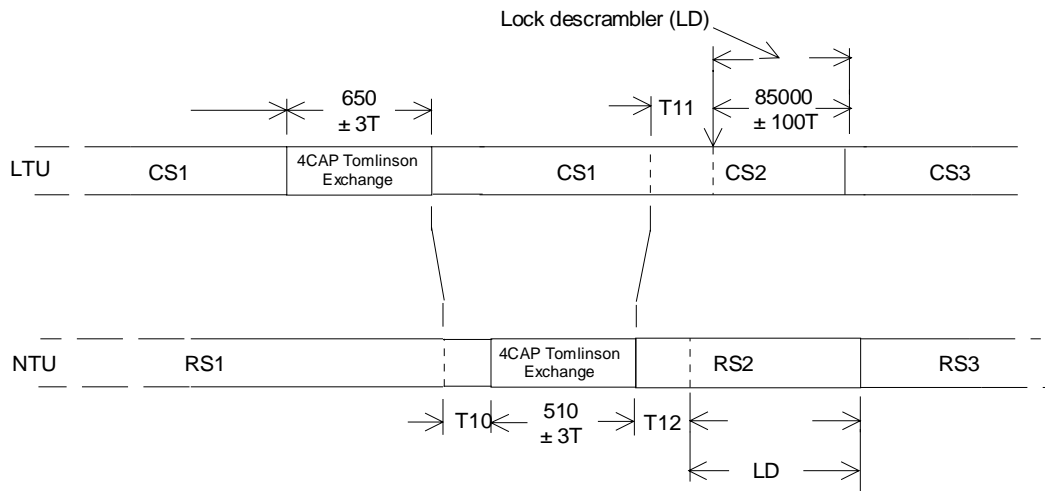


Figure B.16: Start-up sequence - Tomlinson coefficients exchange

The data transfer is done by switching to the 4 CAP signal structure shown in figure B.17. This provides reliable transmission without coding, which is enabled after the transfer is completed.

The data frame structure used to transmit the coefficients is shown in figure B.18. The data frame starts with 128 symbol (4 point) long repetition of ABAB---- (see figure B.17) for synchronization or identification of the start of coefficient data frame. This is followed with a data block marker which is CD (shown in figure B.18) for an HDSL one pair system and channel A of a two pair system and which is DC for channel B of a two pair system. As described in subclause B.5.6.7, these data block markers also provide for pair identification.

The unscrambled data block words are transmitted in 4p symbols as shown in figure B.17 and table B.6. For two pair transceivers, there are 9 inphase and 9 quadrature coefficients. The coefficients for both channels A and B are sent in data frames on both channels. For one pair transceivers, there are 12 inphase and 12 quadrature coefficients. The last 16 bits of a data frame is a checksum equal to the 2's complement of the data block sum.

Data frames for the A and B channels are transmitted simultaneously.

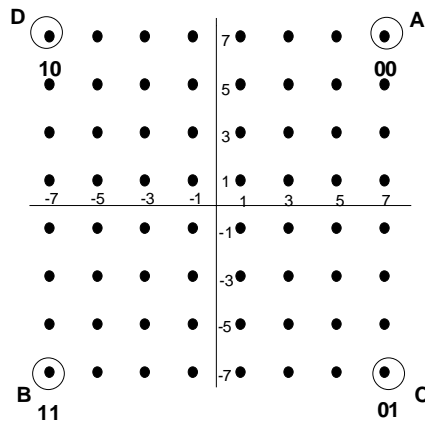


Figure B.17: 4 CAP signal structure - Tomlinson coefficient exchange

As shown in figure B.18, the first 8 bits of a data block defines the size of the data block. The 64 bit control block bit assignments are specified in subclause B.5.6.5.6.

The reserved bits of the data block are followed by 16-bit words, defining the inphase coefficients and the quadrature coefficients, nine words for two pair transceivers and 12 words for one pair transceivers. As indicated in figure B.18, the lsb of each coefficient is transmitted first.

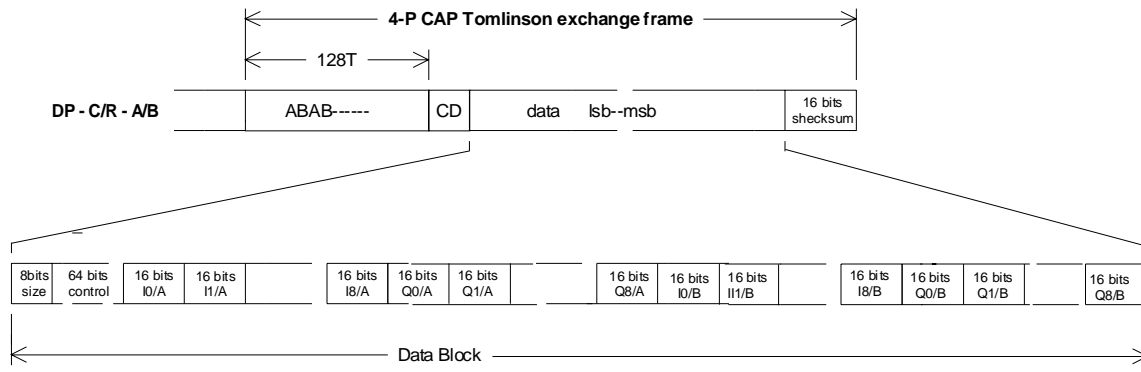


Figure B.18: Tomlinson coefficient frame structure

Table B.6: Tomlinson coefficient data block words

Data block words		
Type	Size - bits	Notes
Block size	8	frame size bits
Control field	64	see subclause B.5.6.5.6
$I[0-N-1]/A$	$16*N$	N inphase coefficients
$Q[0-N-1]/A$	$16*N$	N quadrature coefficients
$I[0-(N-1)]/B$	$16*N$	N inphase coefficients
$Q[0-(N-1)]/B$	$16*N$	N quadrature coefficients
NOTE: N is 9 for two pair transceivers and 12 for one pair transceiver.		

After the Tomlinson coefficients have been transmitted, both the LTU and NTU transceivers again transmit the uncoded 64-CAP sequence. The NTU transceivers transmit this sequence for T10 symbols.

Following this transmission, the LTU and NTU transceivers initiate transmission of S3, a sequence that includes framing and is trellis coded.

B.5.6.5.6 Control field bit assignments

The assignment of bits in the 64 bit control field in the data block of the Tomlinson exchange frame (see figure B.18) are specified in this subclause. The field is broken into four 16 bit words. The two least significant bits of the third 16-bit word is used to send the transmit power identifiers of the transceivers. For a two pair system, the first bit is for channel A and the second bit is for channel B. For a one pair system, the first bit is the transmit power identifier and the second bit is reserved. A ZERO indicates the low transmit power mode. A ONE indicates the high transmit power mode. The transmit power mode is determined, as discussed in subclause B.5.6.5.2, during alerting. The third and fourth bits of the third 16-bit word are reserved for future standardization and the fifth bit is used to identify a regenerator. A ONE indicates the transceiver is in a regenerator while a ZERO indicates that it is not in a regenerator.

The remaining 11 bits of the third 16-bit word are reserved for future standardization. Reserved bits shall be set to ZERO.

The first and the second 16-bit word are reserved for future requirements, the fourth 16-bit word is reserved for vendor-specific applications.

B.5.6.5.7 Transition to data mode

After the Tomlinson coefficients have been transmitted, the NTU transceiver shall transmit the coded 64-CAP sequence RS2. After the LTU transceiver completes the reception of the coefficients, it shall initiate the transmission of the framed sequence CS2 and lock its descrambler. However, it shall wait for an interval T11 before initiating the transmission of CS2, which it shall continue for a period of nominally 3 000 symbols. During this nominally 3 000 symbol period it shall lock its descrambler. Following this period the LTU shall initiate the transmission of CS3, a sequence that includes framing and is trellis coded. The required sequence is shown in figure B.16.

Following the transmission of its Tomlinson coefficients, the NTU transceiver shall initiate the transmission of RS2. It shall continue the transmission of RS2 for a interval of T12 plus nominally 3 000 symbols. It locks its descrambler during the nominally 3 000 symbols interval. Following this interval, it shall initiate the transmission of RS3.

Both the LTU and NTU transceivers shall lock their scramblers prior to initiating the transmission of S3 but after the Tomlinson coefficient exchange. (Scramblers shall be locked during the time when the scramblers are being driven with continuous ONES).

With both transceivers transmitting S3, the transceivers are in the data mode.

B.5.6.6 Retrain procedure

Retrain can be initiated by either the LTU transceiver or the NTU transceiver. To initiate retrain an NTU sends Silent. The LTU transceiver, upon detecting the absence of received signal for period of 1 second, initiates the transmission of S0 and retrain proceeds as above with the alerting sequence. LTU transceiver initiates retrain by sending Silent for 1 second followed by the transmission of the alerting sequence using S0 as shown in figure B.10. Upon recognition of the sequence by the NTU transceiver, retrain proceeds as for initial training. Criteria (conditions - SQ, performance or synchronization) for the initiation of retrain are not specified.

Retrain will be initiated, assuming ACTREQ = ONE, when either the NTU or the LTU goes to the "Inactive State" as implied by the state diagrams discussed in subclause B.5.6.7.

B.5.6.7 Loop activation state diagrams

The following subclauses describe the LTU and NTU state diagrams, as illustrated in figures B.19 and B.20.

B.5.6.7.1 HDSL transceiver states at the NTU

The command QUIET at any state (except the Inactive State) will cause a transition to the Deactivated State. The command QUIET, at the Inactive State, will not cause any transition. When the system is powered on, it enters the Inactive State after it completes all the self tests.

Some of the transitions in the state diagrams depend on the detection of the INDC = ONE status arriving in the incoming data. The LTU transceiver will determine that INDC = ONE only if it detects this condition in 6 consecutive HDSL frames.

B.5.6.7.1.1 Inactive State

During the Inactive State the transmitters in NTU transceivers are silent, LOSW = ONE and LOS = ONE. The NTU transceivers wait for the detection of signal (S0) from the LTU transceiver. Upon detection of this signal the NTU changes to the Activating State (LOS = ZERO).

B.5.6.7.1.2 Activating State

During the Activating State the transmitted signal can be either S0, S1, S2, S3, or Silent. When the transceiver at the NTU enters this state from the Inactive State, it starts the T-Act timer and starts to transmit the RS0 signal from the transceiver on the channel on which it received CS0. LTU/NTU activation proceeds as described in subclause B.5.6.5. When the NTU transmits the RS3 signal and the sync word (CS3) is detected, LOSW = ZERO. If INDR = ONE, the transceiver at the NTU changes to the Active-Rx State. If the NTU senses from CS3 arriving from the transceiver at the LTU with INDC = ONE, the transceiver at the NTU changes to the Active-Tx State. If the T-Act timer expires before CS3 is detected, the transceiver at the NTU goes to the Deactivated State.

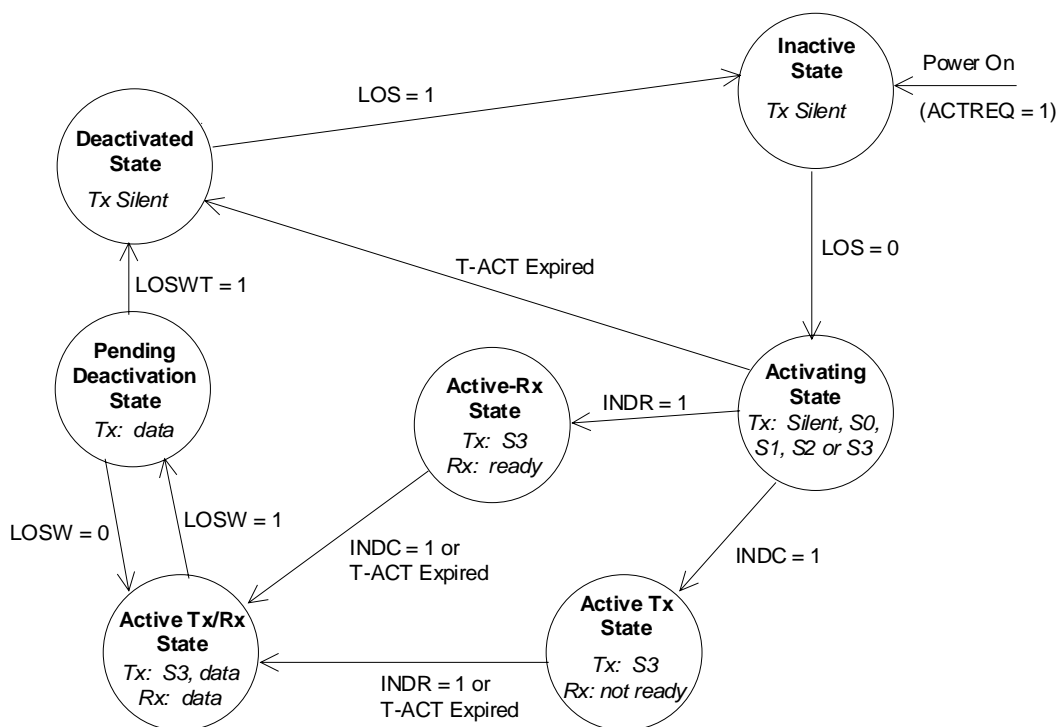


Figure B.19: HDSL transceiver at the NTU loop activation state diagram

B.5.6.7.1.3 Active-Rx State

During the Active-Rx State INDC = ZERO, INDR = ONE and the transceiver at the NTU is transmitting the S3 signal. At the same time the NTU is ready to receive data from the LTU. If the NTU senses from S3 arriving from the LTU that INDC = ONE, or if the T-Act timer expires, the NTU changes to the Active-Tx/Rx State. If frame sync has not been established, the NTU continues to monitor for the frame sync according to figure B.19.

B.5.6.7.1.4 Active-Tx State

During the Active-Tx State INDC = ONE, INDR = ZERO and the NTU is transmitting RS3. At the same time the transceiver at the NTU is receiving the CS3. When frame sync is established, INDR = ONE, or when the T-Act timer expires, the NTU changes to the Active-Tx/Rx State. The NTU continues to monitor the frame sync, if it is not established, according to figure B.19.

B.5.6.7.1.5 Active-Tx/Rx State

Upon entering the Active-Tx/Rx State the T-Act timer is deactivated. The transmitted signal is S3 or data.

If HDSL frame synchronization is lost (LOSW = ONE), the NTU changes to the Pending Deactivation state.

B.5.6.7.1.6 Pending Deactivation State

During the Pending Deactivation State LOSW = ONE, and the transmitted signal is S3 (data). When the NTU enters this state a 2 seconds timer is started. If the HDSL frame synchronization is regained then LOSW = ZERO and the NTU returns to the Active-Tx/Rx State. If the 2 second timer expires, then LOSWT = ONE and the NTI changes to the Deactivated State.

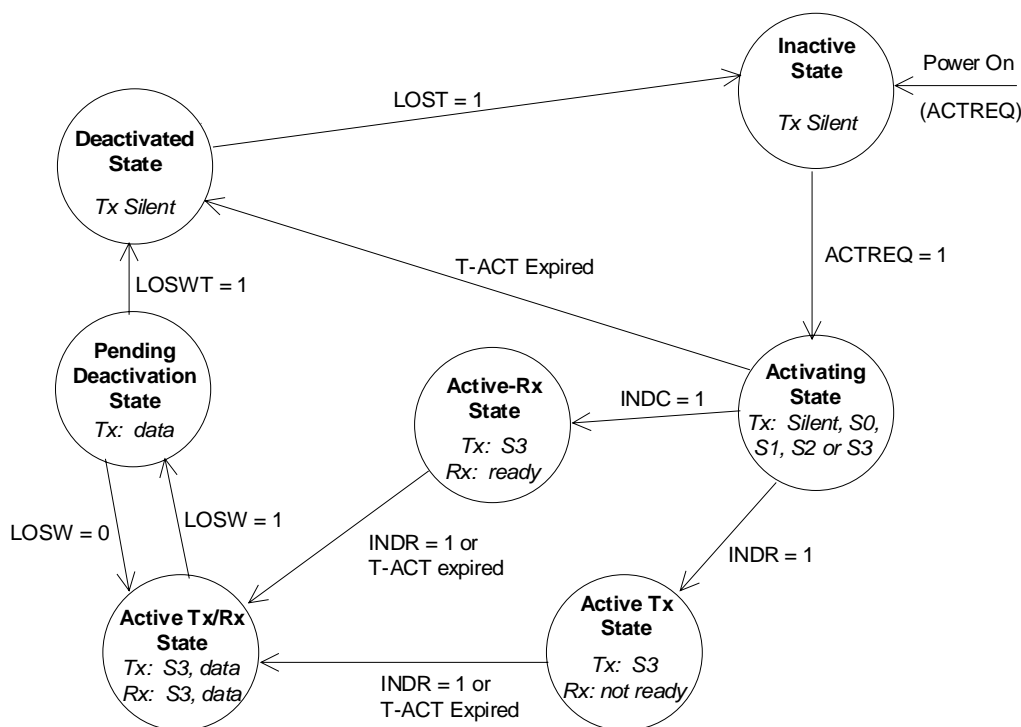


Figure B.20: HDSL transceiver at the LTU loop activation state diagram

B.5.6.7.1.7 Deactivated State

During the Deactivated State, no energy is transmitted to the line (i.e. Silent) and $LOSW = ZERO$. When the NTU enters this state it looks for signal power from the LTU. When no power is detected ($LOS = ONE$) the NTU changes to the Inactive State.

B.5.6.7.2 HDSL transceiver states at LTU

The command QUIET at any state (except the Inactive State) will cause a transition to the Deactivated State. The command QUIET at the Inactive State will not cause any transition. When the system is powered on, it enters the Inactive State after it completes all the self tests.

Some of the transitions in the state diagrams depend on the detection of the $INDR = ONE$ status arriving in the incoming S3 (data). The LTU will decide that $INDR = ONE$ only if it detects this condition in 6 consecutive HDSL frames.

B.5.6.7.2.1 Inactive State

During the Inactive State the LTU transmitters are silent and $LOSW = ONE$. The LTU waits for the $ACTREQ = ONE$ command, and then moves to the Activating State.

B.5.6.7.2.2 Activating State

During the Activating State the transmitted signal can be either S0, S1, S2 or S3. When the LTU enters this state from the Inactive State, it starts to transmit the S0 signal. When an LTU transceiver senses for the first time the S0 signal from the NTU, it starts the T-Act timer and activation proceeds as described in subclause B.5.6.4. During the transmission of the S3 signal, if the HDSL frame synchronization is detected then $LOSW = ZERO$. If the LTU senses from the data arriving from the NTU that $INDR = ONE$, the LTU changes to the Active-Tx State. If $INDC = ONE$ the LTU changes to the Active-Rx State. If the T-Act timer expires, the LTU changes to the Deactivated State.

B.5.6.7.2.3 Active-Rx State

During the Active-Rx State $INDC = ONE$, $INDR = ZERO$ and the LTU transceiver is transmitting S3. At the same time the LTU is ready to receive data from the NTU. When the LTU senses from S3 arriving from the NTU that $INDR = ONE$, or when the T-Act timer expires, the LTU changes to the Active-Tx/Rx State. The LTU continues to monitor the frame sync according to figure B.20.

B.5.6.7.2.4 Active-Tx State

During the Active-Tx State $INDC = ZERO$, $INDR = ONE$ and the LTU is transmitting S3. At the same time the LTU is receiving S3 from the HDSL transceivers at the NTU. When $INDC = ONE$ or when the T-Act timer expires, the LTU changes to the Active-Tx/Rx State. The LTU continues to monitor for frame sync according to figure B.20.

B.5.6.7.2.5 Active State

Upon entering the Active-Tx/Rx State the T-Act timer is deactivated. The transmitted signal is S3 (data).

If the HDSL frame synchronization is lost ($LOSW = ONE$), the LTU changes to the Pending Deactivation State.

B.5.6.7.2.6 Pending Deactivation State

During the Pending Deactivation State $LOSW = ONE$, and the transmitted signal is S3 (data). When the LTU enters this state, a 2 seconds timer is started. If the HDSL frame synchronization is regained then $LOSW = ZERO$ and the LTU returns to the Active-Tx/Rx State. If the 2 seconds timer expires, then $LOSWT = ONE$ and the LTU changes to the Deactivated State.

B.5.6.7.2.7 Deactivated State

During the Deactivated State, no energy is transmitted to the line (i.e. Silent) and $LOSW = ONE$. When the LTU enters this state it looks for signal power from the NTU. When no power is detected ($LOS = ONE$), a 1 second timer is started. When this timer expires ($LOST = ONE$), the LTU changes to the Inactive State.

B.5.6.7.3 The HDSL synchronization state machine

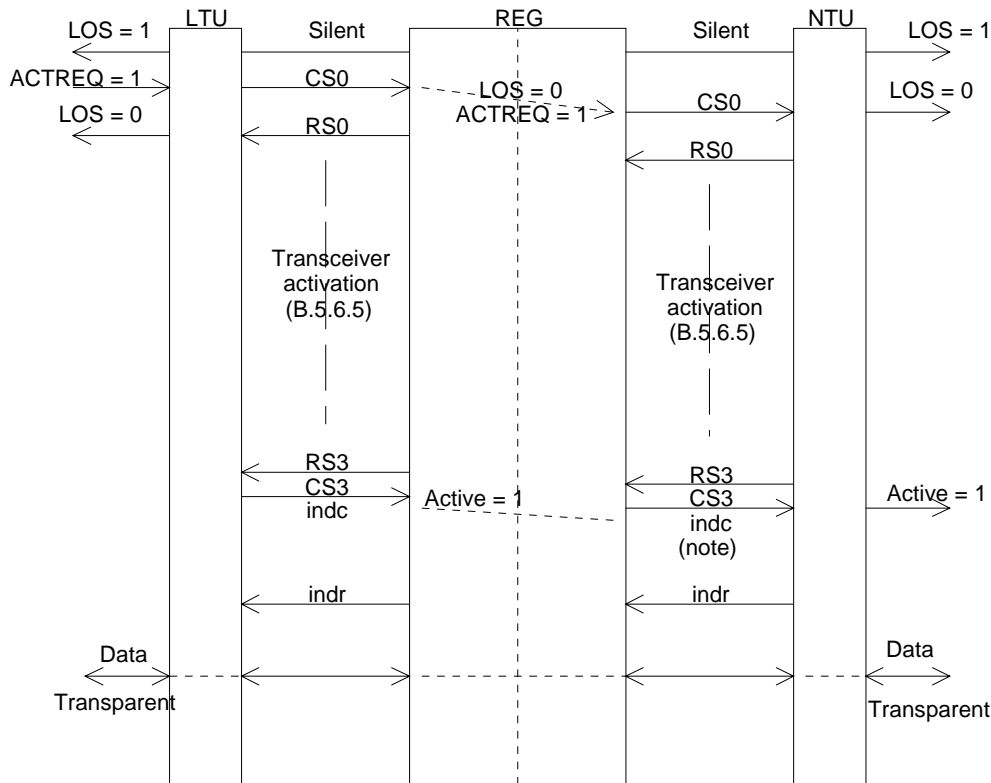
See subclause 5.6.5.3 for a description of the HDSL Synchronization State machine.

B.5.6.8 Regenerator related procedures

In order to achieve data transmission over distances that are greater than can be achieved by a single HDSL link, a regenerator (REG) is necessary. A REG capability is required to be supported where the 2D 8-state trellis code is employed only.

A separate REG has to be provided for each pair. The REG consists of two parts, REG-R for interfacing with the LTU, and REG-C for interfacing with the NTU. An internal connection between the REG-R and REG-C provides communication between the REG-R and REG-C provides communication between the two parts during start-up and normal operation.

The flow diagram in figure B.21 shows the start-up sequence for the link between the LTU and the NTU. While the flow diagram indicates the transmission of CS0 from the REG in response to the detection of CS0 from the LTU, the transmission of CS0 may be delayed until the recovered timing from the LTU is stabilized.



NOTE: The transmission of indc through to the NTU only occurs after both the remote and the network end links are active. Since one link may complete start up before the other, the transmission of indc through to the NTU may be delayed at the REG or it may occur as soon as the remote link is active.

Figure B.21: Start-up procedure with regenerator

B.5.6.9 The pair identification mechanism for two pair system

The pair (path) identification procedure for CAP-HDSL is based on loop identification contained in the messages used to send Tomlinson coefficients as discussed in subclause B.5.6.5.5. The NTU transceivers adopt the identification received from the LTU during this start-up phase. The multiplexing (demultiplexing) of the HDSL frames into (from) the core frame at the NTU adapts to this pair identification.

B.5.7 Operation and Maintenance (O&M)

See subclauses 5.7, 5.7.1, 5.7.2, 5.7.3 and 5.7.4 for requirements concerning O&M, including the description of the messages to be supported by the core. The only exception concerns pair identification. The pair identification mechanism for a two pair system is described in subclause B.5.6.9.

B.5.7.1 Regenerator behaviour

B.5.7.1.1 Response to LOS/LFA

See subclause 5.7.5.1 for the required regenerator response to LOS/LFA.

B.5.7.1.2 Operation of loopback 1A

The activation of loopback 1A in any subsystem of the transceiver is initiated by the LTU using the appropriate eoc message as described in subclause 5.5. The loopback request may be initiated only after the HDSL link is active.

The loopback request may be transmitted toward the REG as soon as signal S3 according to subclause B.5.6 is transmitted in the direction LTU → NTU. After the eoc message has been detected in the REG the loopback is closed accordingly.

If the link is already active, the control unit in the REG closes the loop as soon as the eoc message has been detected. The detailed procedure for reaching the synchronous loopback state is up to the vendor. (It may be necessary to reset the REG-C transceiver, so that its equalizer and echo canceller coefficients may converge under the loopback conditions.) A successfully closed loopback may be detected in the LTU by evaluating the valid received Z-bits or by other means.

The loopback is transparent, i.e., the looped back signal is also transmitted toward the NTU.

During an active loopback 1A, the operation of the HDSL overhead bits shall be as follows:

- the eoc channel is not looped back but is fully operating between the LTU and the REG as described in subclause B.5.5 as long as the messages sent by the LTU contain the REG address "10". When detecting any other address, the REG inserts the "Hold State" message with its own address in the direction REG → LTU.
- all indicator bits, except the REG specific bits hrp, rega, rrbe, which are operating normally, are looped back.

To deactivate loopback 1A, the LTU transmits the "Return to Normal" message together with the address "10" in the eoc channel. After detecting this message, the REG control unit deactivates automatically the REG-C transceiver and cancels the loopback operation.

If the HDSL link between the LTU and the REG is still active, the REG control unit immediately starts to activate the link between the REG and the NTU as described in subclause B.5.6.

The successful completion of the start-up procedure may be detected at the LTU by receipt of indr or by other means.

B.5.8 Electrical characteristics of CAP-based transceivers

B.5.8.1 General

This subclause describes the electrical characteristics of a single HDSL transceiver.

The electrical characteristics of the HDSL transceivers shall assure that the performance requirements of the applications listed in clause 7 are met. In addition, the following specific electrical characteristics are required.

Means should be provided to enable the testing of the electrical characteristics of a single transceiver.

B.5.8.2 Transmitter/receiver impedance and return loss

The nominal driving point impedance of the transceiver line interface shall be 135 Ω .

The minimum return loss with respect to 135 Ω , over the frequency band of 1 kHz to 1 MHz shall as shown in figure B.22 (16 dB from f1 to f2, with 20 dB/decade rise at lower frequencies and a 20 dB/decade drop at higher frequencies to a minimum of 0 dB).

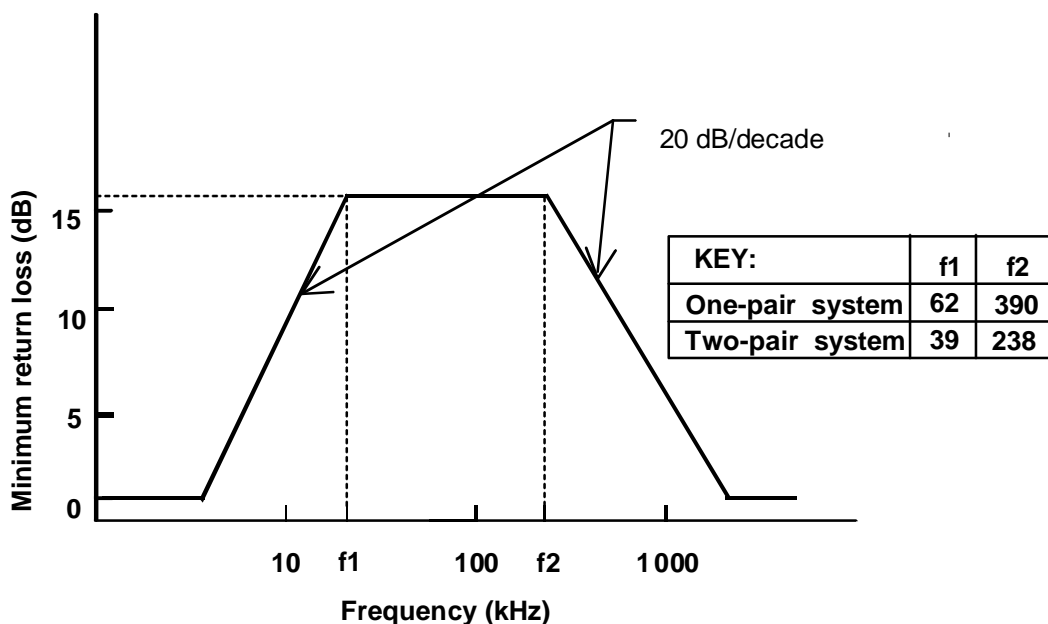


Figure B.22: Minimum return loss of transceiver

B.5.8.3 Transceiver reference clock

B.5.8.3.1 One pair system clock

The reference clock for transceiver for one pair systems shall assure a symbol rate in the range of 386,667 kbaud \pm 90 ppm.

B.5.8.3.2 Two pair system clock

The reference clock for transceivers for two pair systems shall assure a symbol rate in the range of 233,60 kbaud \pm 110 ppm.

B.5.8.4 Transmitter output characteristics

Unless otherwise specified, the following specifications apply with a resistive load impedance of 135 Ω .

B.5.8.4.1 Total power

B.5.8.4.1.1 Two pair system total power

The average transmit power at the transmitter output (excluding remote power feeding) shall be either 13 dBm to 14 dBm (high power mode) or 6 dBm to 8 dBm (low power mode) into a 135 Ω termination. The selection of the high and low power modes is described in subclause B.5.6.5.2.

B.5.8.4.1.2 One pair system total power

The average transmit power at the transmitter output (excluding remote power feeding) shall be either 15 dBm to 16 dBm (high power mode) or 8 dBm to 10 dBm (low power mode) into a 135 Ω termination. The selection of the high and low power modes is described in subclause B.5.6.5.2.

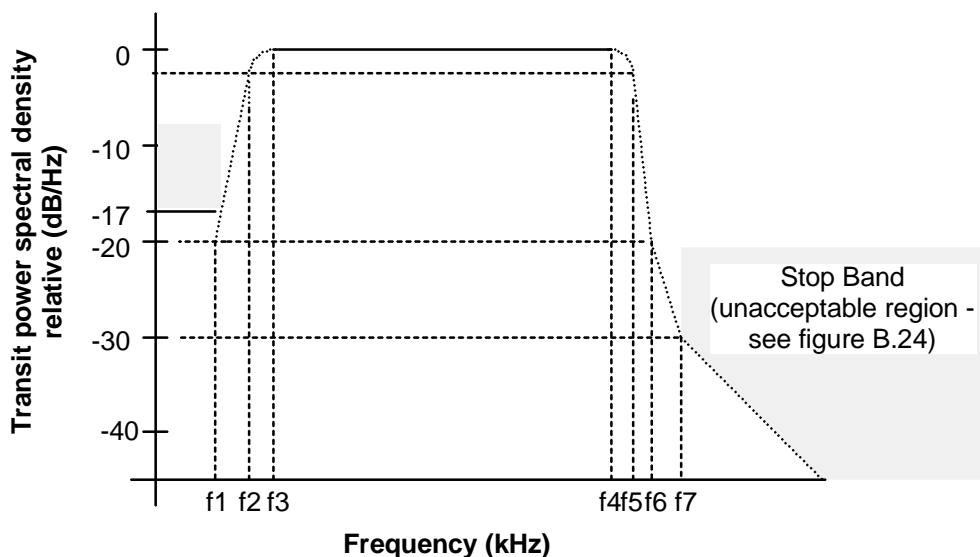
B.5.8.4.2 PSD

Figure B.23 is a template for the CAP HDSL transmit signal spectrum. The template gives the nominal passband PSD. At frequencies below f_3 and above f_4 , as indicated by the dashed line, the template is accurate only at the critical frequencies indicated.

The nominal shape of the transmit signal spectrum is the square root of a raised cosine with a nominal 15 percent excess bandwidth.

The nominal 3 dB points on the spectrum are f_2 and f_5 . This is referred to as the passband in this specification. The spectra of transceiver for one pair and two pair systems are centered around frequencies of 226,33 kHz and 138,30 kHz, respectively.

The signal PSD in the frequency band below f_1 shall be at least 17 dB below the nominal signal power density in the passband. The signal PSD at frequencies above f_7 shall conform to the requirements shown in figure B.24.



KEY:	f1	f2	f3	f4	f5	f6	f7
Two-pair system	3,98	21,50	39,02	237,58	255,10	272,62	297
One-pair system	4,00	33,00	62,00	390,67	419,67	448,67	489,02

Figure B.23: CAP HDSL transmit PSD

Within the band between the frequencies of f_3 and f_4 , the spectral density (dBm/Hz) at any frequency shall be within ± 1 dB of the average density within the band (this means that, for the two pair transceivers, the power/Hz shall be in the range of -40 dBm $\pm 1,5$ dBm). In addition, for one pair transceivers, the maximum spectral density at any frequency shall not exceed -40 dBm/Hz.

The spectral density at f_2 and f_5 shall be -3 dB ± 1 dB relative to the average spectral density in the band of f_3 to f_4 . The spectral density at f_1 and f_6 shall be -20 dB $\pm 3,0$ dB relative the average spectral density in band of f_3 to f_4 . In addition, the spectrum shall comply with the limitations given in figure B.24.

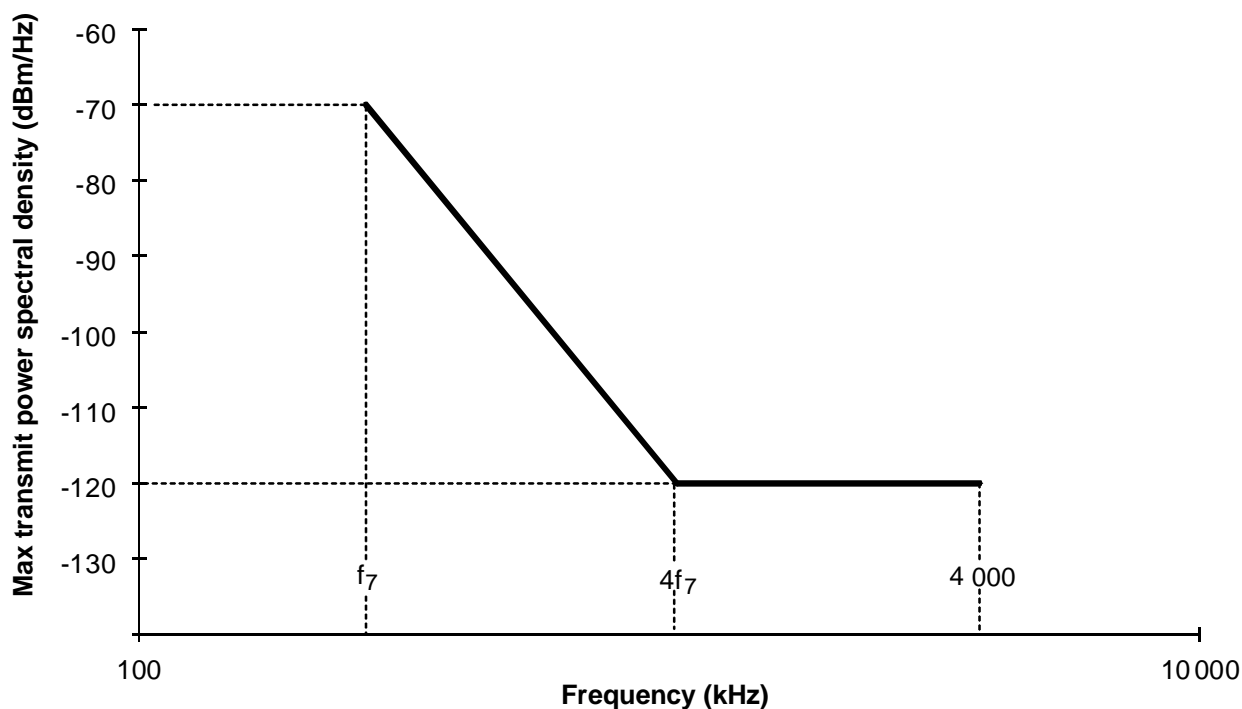


Figure B.24: Maximum out-of-band signal power

B.5.8.5 Unbalance about earth

B.5.8.5.1 Longitudinal Conversion Loss (LCL)

The LCL is given by:

$$- \text{LCL} = 20 \log (e_l/e_m) \text{ dB.}$$

where:

- e_l is the applied longitudinal voltage referenced to the building ground; and
- e_m is the resultant metallic (transverse mode) voltage appearing across a 135 Ω termination.

The LCL of the system shall meet the requirement shown in figure B.25.

See figure 29 for a description of a measurement method for LCL. For direct use of this test configuration, measurement shall be performed with the LTU powered up but inactive (no transmitted signal).

B.5.8.5.2 Longitudinal output voltage

The longitudinal component of the output signal shall have an rms voltage, in any 4 kHz equivalent bandwidth averaged over any 1 second period, < -50 dBV over the frequency range of f_1 to f_2 specified in figure B.25. Compliance with this limitation is required with a longitudinal termination having an impedance of 100 Ω in series with 0,15 μF nominal. The EMC requirements of subclause 9.4 shall be met.

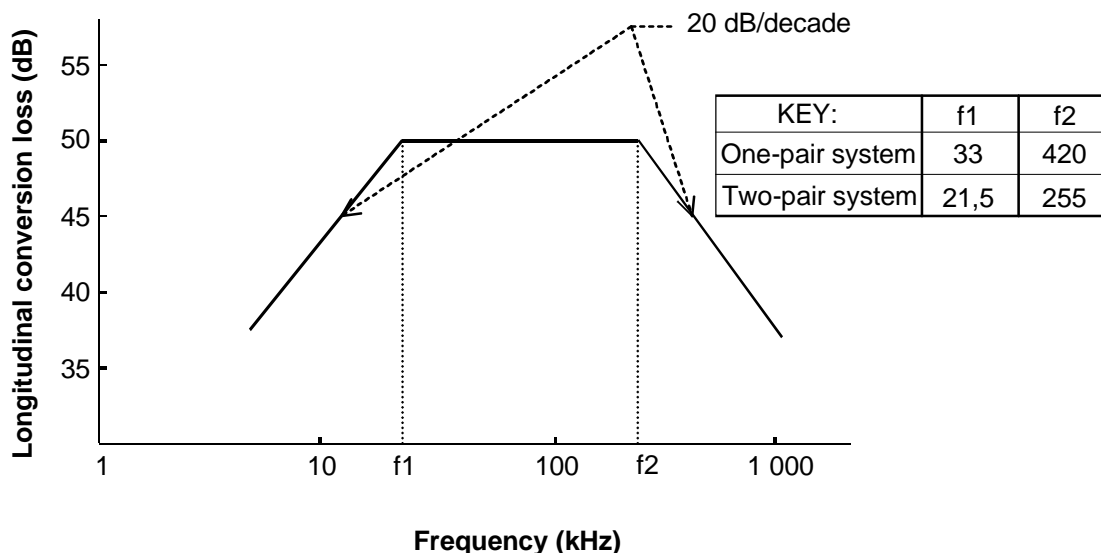


Figure B.25: Minimum LCL

See figure 25 for a description of a measurement method for longitudinal output voltage. For direct use of this test configuration, the IUT (LTU, NTU or REG) should be able to generate a signal in the absence of a signal from the far end.

The ground reference for these measurements shall be the building ground.

B.5.9 Performance of individual HDSL transceivers

B.5.9.1 Performance requirements

Performance limits for the overall system are defined in clause 7. The performance of the individual HDSL transceivers shall be such that these overall performance limits are met. As neither the 1 168 kbit/s or 2 320 kbit/s signal of the individual transceivers is available at an external interface for testing, it is not considered feasible to test the performance of the individual HDSL transceivers. For the purpose of conformance, each HDSL system is required to have an individual performance such that the overall application performance defined in clause 7 for the appropriate application is met.

B.5.9.2 DLL physical models for laboratory testing

Some representative models of DLLs (test loops) for evaluating the performance of transceivers for transmission systems are defined in subclause B.6.2.

B.5.9.3 Jitter and wander

B.5.9.3.1 General

The HDSL transmission system jitter and performance limits are specified in clause 7. These limits are specified at the application interfaces for specific applications. The limits specified here are intended to ensure compatibility of LTUs and NTUs from different manufacturers, i.e. ensure that system performance limits are met by systems employing LTUs and NTUs from different manufacturers.

The following limitations apply at transmission line interfaces of transceivers. However, due to the bi-directional transmission on the two-wire line and due to severe intersymbol interference, no well defined signal transitions are available on the two-wire signal. It is therefore necessary to provide reference clock outputs to enable the following requirements to be tested.

The jitter limits given below shall be satisfied regardless of the length of the local line, provided that it is covered by the transmission media characteristics of subclause B.5.2. The scrambler specified in subclause B.5.3.4 assures that, if the limits are met for one bit sequence, they will be met for all possible transmitted bit sequences. In this subclause, jitter is specified in terms of unit intervals (UI), which are equal to symbol intervals, at the nominal line symbol rates. The symbols rates and UIs are:

- transceiver for one pair system: 386,667 kbaud and UI = 2,586 μ s;
- transceiver for two pair system: 233,600 kbaud and UI = 4,281 μ s.

B.5.9.3.2 Input jitter tolerance at the HDSL transceiver at the NTU

The NTU shall meet the performance objectives specified in clause 7 with the following wander/jitter superimposed on the clock of the test signal source of the received signal and with the received signal symbol rate at any rate in the permitted transceiver clock range specified in subclause B.5.8.3 but with a variation of up to ± 25 ppm. The wander/jitter shall have sinusoidal characteristics at the maximum amplitudes defined in figure B.26 with the values specified in table B.7 for single frequencies in the range of 0,1 Hz to f3.

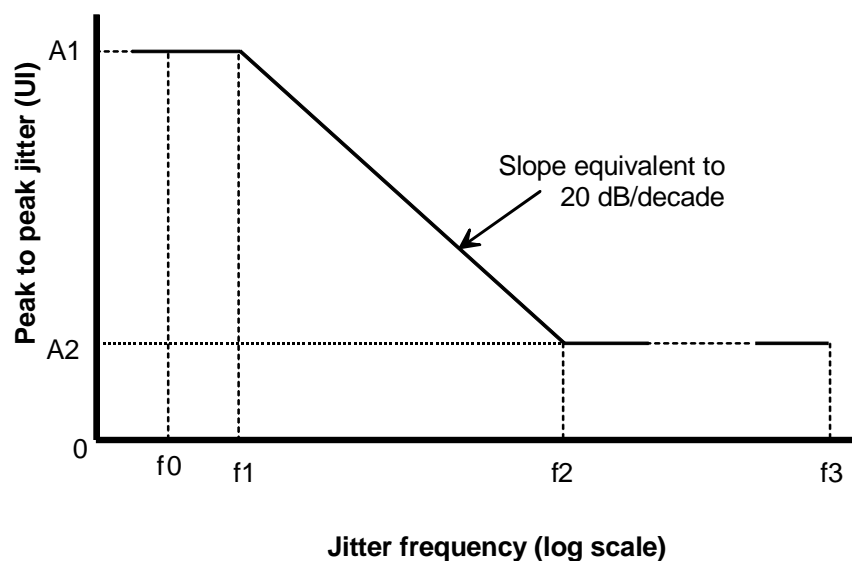


Figure B.26: Single frequency jitter and wander limitation

Table B.7: Single frequency jitter/wander parameters

	Peak amplitude		Frequency			
	A1	A2	f0	f1	f2	f3
NTU input	0,25 UIpp	0,005 UIpp	0,10 Hz	0,20 Hz	20 Hz	20 kHz
LTU input		0,005 UIpp			20 Hz	20 kHz

B.5.9.3.3 Output jitter limitations of an HDSL transceiver in an NTU

With NTU transceiver received signal having the maximum wander/jitter at individual single frequencies given in figure B.26, wander/jitter on the transmitted signal of the NTU towards the LTU shall conform to the following (With the add/delete function specified in subclause B.5.4, the jitter superimposed on the NTU input (application interface) signal does not impact the NTU transceiver output signal jitter).

The maximum NTU output signal jitter shall be equal to or less than that indicated in table B.8. B1 is measured with a bandpass filter having a lower cut-off frequency of f1 and an upper cut-off frequency of f2. B2 is measured with a similar filter where the cut-off frequencies are f2 and f3. Bandpass filters shall have rolloffs above and below cut-off frequencies of nominally 6 dB/octave.

The maximum (peak) departure of the phase of the NTU transceiver output signal from its nominal difference (long-term average) from the phase of the NTU transceiver input (from the LTU) shall not exceed 0,2 UI. That is:

- max. $|\Phi_{\text{inst.}} - \Phi_{\text{average}}| \leq 0,2 \text{ UI}$; where:

$\Phi_{\text{inst.}}$ = instantaneous phase of NTU transmitted signal relative to the average phase of the NTU received signal.
 Φ_{average} = long-term average phase difference between NTU transmitted and received signals.

Table B.8: Maximum output jitter/wander

	Maximum jitter		Measurement filter parameters		
	B1 = f1-f2	B2 = f2-f3	f1	f2	f3
NTU	0,25 U _{pp}	0,005 U _{pp}	0,2 Hz	2 Hz	20 kHz
LTU	0,25 U _{pp}	0,005 U _{pp}	0,2 Hz	2 Hz	20 kHz

B.5.9.3.4 Input jitter tolerance at the HDSL transceiver at the LTU

The LTU shall meet the performance objectives specified in clause 7 with wander/jitter as follows superimposed on the clock of the test signal source of the received signal and with the received signal symbol rate at any rate in the permitted transceiver clock range specified in subclause B.5.8.3 with a variation of up to ± 25 ppm. The wander/jitter shall have sinusoidal characteristics at the maximum amplitudes defined in figure B.26 with the values specified in table B.7 for single frequencies in the range of 0,1 Hz to f3. The wander in the input signal is limited to the wander in the LTU output by the requirement in subclause B.5.9.3.3 that the NTU output track the NTU input within 0,2 UI.

B.5.9.3.5 Output jitter limitation of the HDSL transceiver at the LTU

The maximum jitter and wander on the transmitted signal of the LTU towards the NTU shall be as indicated in table B.8. (The transmitted bit stream is synchronized to a local clock in the LTU transceiver and therefore the wander is determined by the stability of the clock and the jitter is determined by count-down circuit used to derive the symbol rate clock.)

B.6 Common circuitry specification

B.6.1 Delay difference buffer

In order to compensate for any difference in total transmission time of the HDSL frames on different pairs, due to the pair differences described in subclause 5.2.4.2, as well as to delays due to signal processing in the HDSL transceivers in the LTU and NTU and possible REG, a delay difference buffer shall be implemented in the common circuitry. The function of this delay difference buffer is to align the HDSL frames so that the core frames can be correctly reassembled. This buffer should be capable of absorbing a maximum delay difference of 60 μ s.

B.6.2 Laboratory performance measurement tests

B.6.2.1 General

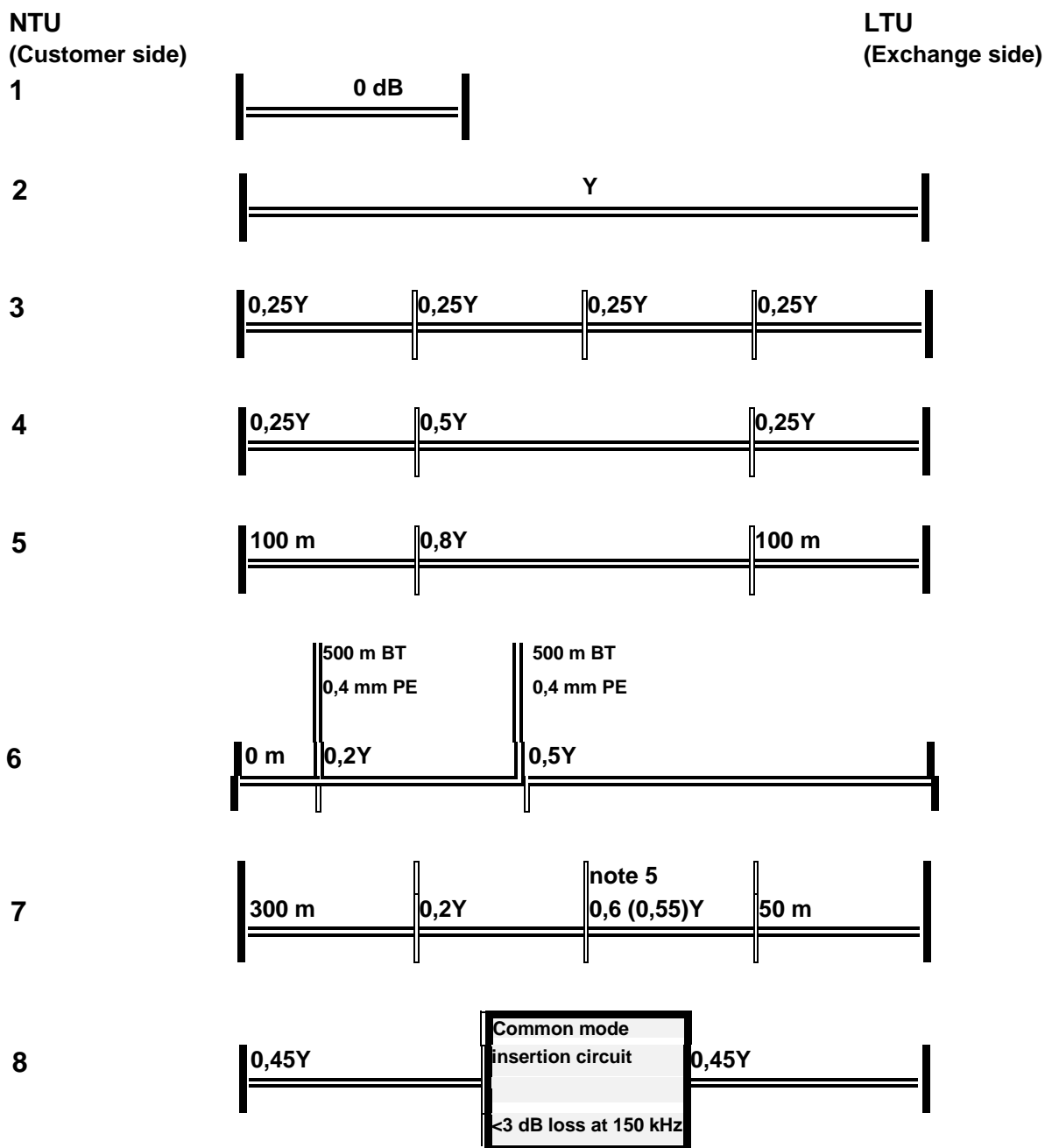
See subclause 6.3.1 for general requirements. The figure showing the defined models of DLLs (test loops) is reproduced here for convenience in figure B.27.

B.6.2.2 Test configuration

See subclause 6.3.2, figure 34, for a description of the test configuration.

Two distinct classes of added disturbance are injected: Test noise (specified in subclauses B.6.2.3.1 and B.6.2.3.2) and impulses (defined in subclause 6.3.4.1). A further test (specified in subclause B.6.2.6) tests the immunity of the system under test to micro-interruptions.

The proposed test sequence for the HDSL system is shown in table B.9.



- NOTE 1: The value for Y (insertion loss in dB at 150 kHz) is to be found in table B.9.
- NOTE 2: Due to mismatches and bridged taps (BTs) the total DLL attenuation differs from the sum of the attenuation of the parts. Annex A provides theoretical values for the transmission parameters of the above loops.
- NOTE 3: Attenuation of separate sections is measured with a 135 Ω termination.
- NOTE 4: These test loops and artificial cable parameters include worst case examples as well as those more typical of a local network. They are chosen to provide the wide range of different echoes and distortions which may occur in European networks.
- NOTE 5: The value in brackets is valid for one pair systems only. The reduction is necessary to compensate the higher attenuation of the fixed sections.
- NOTE 6: See figure 33.

Figure B.27: DLL physical models for laboratory testing

B.6.2.3 Test procedure with random noise source

Most noise on local network lines can be represented by an artificial noise source as described below. Tests shall be as indicated in table B.9. Tests shall be carried out with the injection circuit described in subclause 6.3.3.3 and noise source and test loop calibration shall be as specified in subclause 6.3.3.4.

B.6.2.3.1 Low crest factor noise

This artificial noise is intended to represent intersystem and intrasystem crosstalk. It is defined to assure that essentially the same performance will be obtained in laboratory measurements using noise sources from different test set vendors.

See subclauses 6.3.3.1 and 6.3.3.2 for a description of the low crest factor shaped noise.

B.6.2.3.2 Truncated Gaussian noise

Truncated Gaussian noise is defined to have a nominally Gaussian amplitude distribution. Noise having a Gaussian amplitude distribution is representative of worst case crosstalk. However, the amplitude distribution may be truncated at a crest factor of 5,0.

The noise density shall be $10 \mu\text{V}/\sqrt{\text{Hz}}$ and nominally flat from 10 kHz to 240 kHz. Tests using the noise source described in subclause 6.3.3 is adequate for evaluating the effects of an increased magnitude at frequencies below 10 kHz.

B.6.2.4 Test procedure for impulse noise

B.6.2.4.1 Impulse noise test waveform

See subclause 6.3.4.1 for the specification of impulse noise.

B.6.2.4.2 Impulse noise test measurement

The test impulse shall be applied to the system under test as specified in subclause 6.3.4.3 using the test configuration described in subclause 6.3.4.2. The performance criteria for transceivers for one pair and two pair systems shall be as specified in table 21 except that the value of Y shall be 23 dB and 31 dB, respectively.

B.6.2.4.3 Impulse noise test performance requirements

Table 21 gives the maximum bit error ratio for the three levels of impulse noise. The peak-to-peak amplitude of the test impulse noise is given in mV (and in dB relative to a reference level of 320 mV) measured at the output of the shunt injection circuit, loaded with a 67,5 Ω resistor.

Table B.9: Test sequence

N	loop	Direction	Comment
1	#1 (see note 1)	Forward	Y = 0 dB, Test noise of subclause B.6.2.3.1 with N1 = 300 μ V/ \sqrt Hz and N2 = 30 μ V/ \sqrt Hz
2	#2	Forward	Y = Y1; (see note 2) Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
3	#3	Forward	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
4	#3	Reverse	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
5	#4	Forward	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
6	#4	Reverse	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
7	#5	Forward	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
8	#6	Forward	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
9	#6	Reverse	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
10	#7	Forward	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
11	#7	Reverse	Y = Y1; Test Noise of subclauses B.6.2.3.2 and B.6.2.3.1 with N1 = 100 μ V/ \sqrt Hz and N2 = 10 μ V/ \sqrt Hz
12	#8	Forward	Y = Y1; Common mode rejection test of subclause B.6.2.5
13	(see note 3)	Forward and Reverse	Y = Y2; Test noise of subclause B.6.2.3.1 with N1 = 300 μ V/ \sqrt Hz and N2 = 30 μ V/ \sqrt Hz Worst path of tests 1 to 11
14	(see note 3)	(see note 3)	Y = Y3; No added impairment; Worst path of tests 1 to 11, BER < 10 ⁻⁸
15	#2	Forward	Y = Y1; Impulse test as described in subclause B.6.2.4.4
16	As for subclause B.6.2.6	Forward	Micro-interruption test as described in subclause B.6.2.6
NOTE 1: Test loop = #1 means that the path under test shall be connected with test loop #1 as defined in figure B.27. The path not under test shall be connected with a dummy loop, normally loop #1.			
NOTE 2: Y1 = 23 dB for the one pair system and Y1 = 31 dB for the two pair system, except that, for determining performance in the presence of truncated Gaussian noise (subclause B.6.2.3.2), in which case, Y1 shall be reduced by 1dB. Y2 = Y1 - 10 dB and Y3 = Y1 + 3 dB.			
NOTE 3: The tests are carried out on the worst path in the worst direction from tests 1 to 11, with a dummy loop for the remaining path. If there are no errors, then loop #2 forward for path A is taken as default.			
NOTE 4: The tests 1 to 15 shall be carried out on all pairs. In the case of a fractionally installed two pair HDSL system, the tests shall be carried out only on the installed pair.			

B.6.2.5 Common mode rejection test

See subclause 6.3.5 for common mode rejection requirements.

B.6.2.6 Micro-interruption test

See subclause 6.3.6 (figure 37) for a description of the configuration for micro-interruption susceptibility tests. In this arrangement, a periodic trigger signal stimulates a micro-relay device inducing periodic micro-interruptions on one of the pairs forming the transmission link. Using the test arrangement shown in figure 37, each HDSL transceiver shall not be reset by a micro-interruption of (at least) $t = 10$ ms when stimulated with a signal of period $T = 5$ seconds.

B.7 Application specific requirements

B.7.1 Application specific requirements for ISDN PRA

B.7.1.1 Mapping of 2 048 kbit/s to HDSL

See subclause 7.1.1 for requirements concerning the mapping of 2 048 kbit/s to the HDSL frame.

B.7.1.2 Mapping of HDSL maintenance functions to the interfaces

See subclause 7.1.2 for requirements concerning the mapping of HDSL maintenance functions to the interfaces.

B.7.1.3 Performance

B.7.1.3.1 Performance specification

The overall performance shall be such that the performance limits given in ITU-T Recommendation G.826 [10] can be met. For the purpose of conformance, an HDSL transmission system is required to meet the specific laboratory performance tests that are defined in the following subclauses.

B.7.1.3.2 Signal transfer delay

The one-way signal transfer delay, which is the mean value of the delay time in both directions of transmission between the T and V3 reference points, as defined in ETS 300 233 [1], shall not exceed 1 250 μ s.

The one-way signal transfer delay of elements shall not exceed the following:

Table B.10 Signal transfer delay

element	One pair system	Two pair system
Line	100 μ s	120 μ s
LTU & NTU Tx	420 μ s	420 μ s
LTU & NTU Rx	450 μ s	450 μ s
REG	260 μ s	260 μ s

B.7.1.3.3 Clock specification for external interfaces

See subclause 7.1.3.3 for the specifications concerning of clock tolerances, wander and jitter at the external interfaces.

B.7.2 Additional application specific requirements

See subclauses 7.2, 7.3, 7.4, 7.5 and 7.6 to requirements for the 2 048 kbit/s digital unstructured leased line, for the 2 048 kbit/s digital structured leased line, for fractional installation, for partial operation and for 2 048 kbit/s mapped into TU-12 structure, respectively. However, the provisions of subclause B.5.4.2.1 are applicable for all of the applications specified in subclauses 7.2 through 7.6.

B.8 Power feeding

See clause 8 for power feeding requirements.

B.9 Environmental requirements

See clause 9 for environmental requirements.

Annex C (informative): Transmission system for 1 544 kbit/s two pair system application

For the transport of 1 544 kbit/s based applications a different transmission system has been published in ANSI Committee T1 Technical Report No. 28 [25].

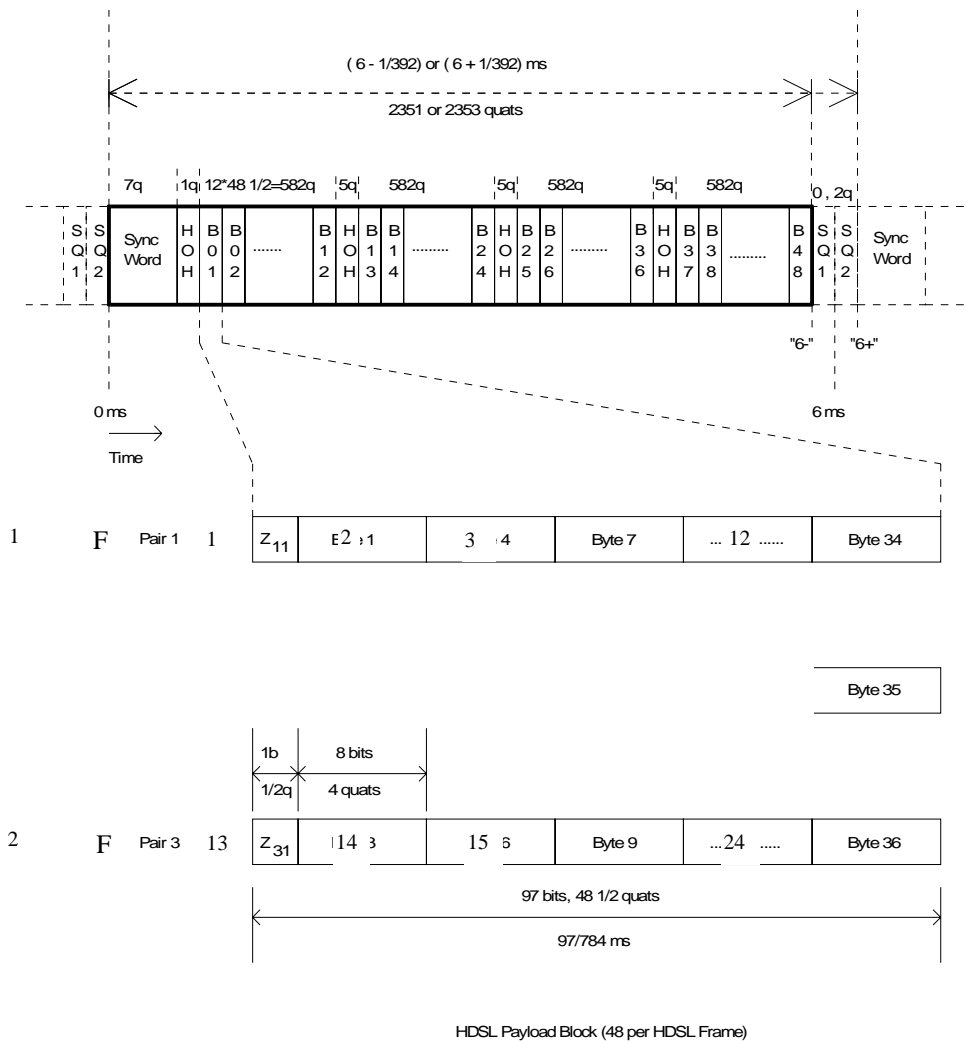
Only two pair systems are proposed in this report. As described in subclause 6.2, no pair identification mechanism for 2 048 kbit/s based applications is possible with this transmission system.

C.1 Frame structure of the two pair system for 784 kbit/s

Figure C.1 illustrates the HDSL frame structure composed of quaternary symbols (quats) and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the seven symbols long synchronization word followed by one HDSL overhead quat and 12 blocks of HDSL payload, each consisting of 48,5 quats, equivalent to 97 bits, containing the framing bit F and 12 bytes of the application frame.

The three groups following the first group have an equal structure. Each consists of five HDSL overhead quats and 12 HDSL payload blocks as described above. So one frame contains a synchronization word, 16 HDSL overhead quats, 48 F-bits and 576 bytes of the application frame payload.

At the end of the frame the possibility of 2 stuffing quats is foreseen. These quats are used always together; this means either none or two stuffing quats are inserted, depending on the relation of the timing. The length of the HDSL frame is either 2 353 quats, which equals $6 + 1/392$ ms for the nominal HDSL clock frequency, or 2 351 quats corresponding to $6 - 1/392$ ms and the average will tend to 2 352 quats or 6 ms. The receiver is able to evaluate the length of an incoming frame by detection of the sync word in the following frame and to adjust the demultiplexing of the data stream.



Symbol	Name, function
B01 to B48	HDLSL system payload blocks
Byte n	Byte n from core frame (n = 1 to 144)
F	Framing bit of application frame
HOH	HDLSL overhead (sw, eoc, crc,...)
quat	Quaternary symbol
SQ1, SQ2	Stuff quats
Sync word	7-symbol Barker codes, "double Barker" → 14 bits
"6-", "6+"	6 - 1/392 ms, 6+1/392 ms

Figure C.1: Frame structure of the two pair system for 784 kbit/s

Table C.1: HDSL frame structure for the two pair system for 784 kbit/s

Time	Frame bit #	HOH bit#	Abbreviated name	Full name	Notes
0 ms	1 to 14	1 to 14	SW 1 to 14	Sync word	Double Barker Code
	15	15	losd	loss of input signal at the far end application interface	
	16	16	febe	far end block error	
	17 to 1 180	-----	B01 to B12	Payload block 1 to 12	HDSL payload
	1 181	17	eoc01	eoc address	
	1 182	18	eoc02	eoc address	
	1 183	19	eoc03	eoc data/opcode	
	1 184	20	eoc04	eoc Odd/Even Byte	
	1 185	21	crc1	cyclic redundancy check	CRC-6
	1 186	22	crc2	cyclic redundancy check	CRC-6
	1 187	23	ps1	NTU power status bit 1	NTU → LTU only
	1 188	24	ps2	NTU power status bit 2	NTU → LTU only
	1 189	25	bpv	bipolar violation	
	1 190	26	eoc05	eoc unspecified	
	1 191 to 2 354	-----	B13 to B24	Payload blocks 13 to 24	HDSL payload
	2 355	27	eoc06	eoc message bit 1	
	2 356	28	eoc07	eoc message bit 2	
	2 357	29	eoc08	eoc message bit 3	
	2 358	30	eoc09	eoc message bit 4	
	2 359	31	crc3	cyclic redundancy check	CRC-6
	2 360	32	crc4	cyclic redundancy check	CRC-6
	2 361	33	hrp	regenerator present	LTU ← REG → NTU
	2 362	34	uib	unspecified indicator bit	
	2 363	35	uib	unspecified indicator bit	
	2 364	36	uib	unspecified indicator bit	
	2 365 to 3 528	-----	B25 to B36	Payload blocks 25 to 36	HDSL payload
	3 529	37	eoc10	eoc message bit 5	
	3 530	38	eoc11	eoc message bit 6	
	3 531	39	eoc12	eoc message bit 7	
	3 532	40	eoc13	eoc message bit 8	
	3 533	41	crc5	cyclic redundancy check	CRC-6
	3 534	42	crc6	cyclic redundancy check	CRC-6
	3 535	43	uib	unspecified indicator bit	
	3 536	44	indr/indr	ready to receive	indr=LTU → NTU indr=NTU → LTU
	3 537	45	uib	unspecified indicator bit	
	3 538	46	uib	unspecified indicator bit	
6 - 1/392 ms	3 539 to 4 702	-----	B37 to B48	Payload blocks 37 to 48	HDSL Payload
	4 703	47	stq1s	stuff quat 1 sign	Frame stuffing
6 ms nominal	4 704	48	stq1m	stuff quat 1 magnitude	Frame stuffing
	4 705	49	stq2s	stuff quat 2 sign	Frame stuffing
6 + 1/392 ms	4 706	50	stq2m	stuff quat 2 magnitude	Frame stuffing

History

Document history		
Edition 1	February 1995	Published as ETR 152
Edition 2	June 1995	Published as ETR 152
Edition 3	December 1996	Published as ETR 152
V1.4.1	February 1998	Publication
V1.5.1	November 1998	Publication
V1.5.2	September 1999	Publication
V1.5.3	September 2000	Publication