ETSI TS 125 213 V8.1.0 (2008-10)

Technical Specification

Universal Mobile Telecommunications System (UMTS);
Spreading and modulation (FDD)
(3GPP TS 25.213 version 8.1.0 Release 8)

Reference

RTS/TSGR-0125213v810

Keywords

UMTS

ETSI

650 Route des Lucioles
F-06921 Sophia Antipolis Cedex - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Siret N° 348 623 562 00017 - NAF 742 C
Association à but non lucratif enregistrée à la
Sous-Préfecture de Grasse (06) N° 7803/88

Important notice

Individual copies of the present document can be downloaded from:
http://www.etsi.org

The present document may be made available in more than one electronic version or in print. In any case of existing or perceived difference in contents between such versions, the reference version is the Portable Document Format (PDF). In case of dispute, the reference shall be the printing on ETSI printers of the PDF version kept on a specific network drive within ETSI Secretariat.

Users of the present document should be aware that the document may be subject to revision or change of status. Information on the current status of this and other ETSI documents is available at
http://portal.etsi.org/tb/status/status.asp

If you find errors in the present document, please send your comment to one of the following services:
http://portal.etsi.org/chaircor/ETSI_support.asp

Intellectual Property Rights

IPRs essential or potentially essential to the present document may have been declared to ETSI. The information pertaining to these essential IPRs, if any, is publicly available for **ETSI members and non-members**, and can be found in ETSI SR 000 314: *"Intellectual Property Rights (IPRs); Essential, or potentially Essential, IPRs notified to ETSI in respect of ETSI standards"*, which is available from the ETSI Secretariat. Latest updates are available on the ETSI Web server (http://webapp.etsi.org/IPR/home.asp).

Pursuant to the ETSI IPR Policy, no investigation, including IPR searches, has been carried out by ETSI. No guarantee can be given as to the existence of other IPRs not referenced in ETSI SR 000 314 (or the updates on the ETSI Web server) which are, or may be, or may become, essential to the present document.

Foreword

This Technical Specification (TS) has been produced by ETSI 3rd Generation Partnership Project (3GPP).

The present document may refer to technical specifications or reports using their 3GPP identities, UMTS identities or GSM identities. These should be interpreted as being references to the corresponding ETSI deliverables.

The cross reference between GSM, UMTS, 3GPP and ETSI identities can be found under http://webapp.etsi.org/key/queryform.asp.

Contents

Intellectual Property Rights 2

Foreword 2

Foreword 5

1 Scope 6

2 References 6

3 Symbols and abbreviations 6
3.1 Symbols 6
3.2 Abbreviations 6

4 Uplink spreading and modulation 7
4.1 Overview 7
4.2 Spreading 7
4.2.1 Dedicated physical channels 7
4.2.1.1 DPCCH/DPDCH 9
4.2.1.2 HS-DPCCH 10
4.2.1.3 E-DPDCH/E-DPCCH 11
4.2.2 PRACH 17
4.2.2.1 PRACH preamble part 17
4.2.2.2 PRACH message part 17
4.2.3 Void 18
4.3 Code generation and allocation 18
4.3.1 Channelisation codes 18
4.3.1.1 Code definition 18
4.3.1.2 Code allocation for dedicated physical channels 19
4.3.1.2.1 Code allocation for DPCCH/DPDCH 19
4.3.1.2.2 Code allocation for HS-DPCCH 19
4.3.1.2.3 Code allocation for E-DPCCH/E-DPDCH 19
4.3.1.3 Code allocation for PRACH message part 20
4.3.1.4 Void 20
4.3.1.5 Void 20
4.3.2 Scrambling codes 20
4.3.2.1 General 20
4.3.2.2 Long scrambling sequence 20
4.3.2.3 Short scrambling sequence 21
4.3.2.4 Dedicated physical channels scrambling code 22
4.3.2.5 PRACH message part scrambling code 22
4.3.2.6 Void 23
4.3.2.7 Void 23
4.3.3 PRACH preamble codes 23
4.3.3.1 Preamble code construction 23
4.3.3.2 Preamble scrambling code 23
4.3.3.3 Preamble signature 23
4.3.4 Void 24
4.4 Modulation 24
4.4.1 Modulating chip rate 24
4.4.2 Modulation 24

5 Downlink spreading and modulation 25
5.1 Spreading 25
5.1.1 Modulation mapper 25
5.1.1.1 QPSK 25
5.1.1.2 16QAM 26
5.1.1.3 64QAM 26
5.1.2 Channelisation 27
5.1.3 IQ combining 27

5.1.4 Scrambling 27
5.1.5 Channel combining 27
5.2 Code generation and allocation 28
5.2.1 Channelisation codes 28
5.2.2 Scrambling code 29
5.2.3 Synchronisation codes 30
5.2.3.1 Code generation 30
5.2.3.2 Code allocation of SSC 31
5.3 Modulation 33
5.3.1 Modulating chip rate 33
5.3.2 Modulation 33

Annex A (informative): Generalised Hierarchical Golay Sequences 34

A.1 Alternative generation 34

Annex B (informative): Change history 35

History 37

Foreword

This Technical Specification (TS) has been produced by the 3rd Generation Partnership Project (3GPP).

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of the present document, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

Version x.y.z

where:

- x the first digit:
  - 1 presented to TSG for information;
  - 2 presented to TSG for approval;
  - 3 or greater indicates TSG approved document under change control.
- y the second digit is incremented for all changes of substance, i.e. technical enhancements, corrections, updates, etc.
- z the third digit is incremented when editorial only changes have been incorporated in the document.

1 Scope

The present document describes spreading and modulation for UTRA Physical Layer FDD mode.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies. In the case of a reference to a 3GPP document (including a GSM document), a non-specific reference implicitly refers to the latest version of that document *in the same Release as the present document*.

[1] 3GPP TS 25.201: "Physical layer - general description".

[2] 3GPP TS 25.211: "Physical channels and mapping of transport channels onto physical channels (FDD)."

[3] 3GPP TS 25.101: "UE Radio transmission and Reception (FDD)".

[4] 3GPP TS 25.104: "UTRA (BS) FDD; Radio transmission and Reception".

[5] 3GPP TS 25.308: "UTRA High Speed Downlink Packet Access (HSDPA); Overall description".

[6] 3GPP TS 25.214: "Physical layer procedures (FDD)".

[7] 3GPP TS 25.212: "Multiplexing and channel coding (FDD)".

3 Symbols and abbreviations

3.1 Symbols

For the purposes of the present document, the following symbols apply:

$C_{ch,SF,n}$: n:th channelisation code with spreading factor SF
$C_{pre,n,s}$: PRACH preamble code for *n*:th preamble scrambling code and signature *s*
$C_{sig,s}$: PRACH signature code for signature *s*
$S_{dpch,n}$: *n*:th DPCCH/DPDCH uplink scrambling code
$S_{r\text{-}pre,n}$: *n*:th PRACH preamble scrambling code
$S_{r\text{-}msg,n}$: *n*:th PRACH message scrambling code
$S_{dl,n}$: DL scrambling code
C_{psc}: PSC code
$C_{ssc,n}$: n:th SSC code

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

16QAM 16 Quadrature Amplitude Modulation
64QAM 64 Quadrature Amplitude Modulation

AICH	Acquisition Indicator Channel
BCH	Broadcast Control Channel
CCPCH	Common Control Physical Channel
CPICH	Common Pilot Channel
DCH	Dedicated Channel
DPCH	Dedicated Physical Channel
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
E-AGCH	E-DCH Absolute Grant Channel
E-DPCCH	E-DCH Dedicated Physical Control Channel
E-DPDCH	E-DCH Dedicated Physical Data Channel
E-HICH	E-DCH Hybrid ARQ Indicator Channel
E-RGCH	E-DCH Relative Grant Channel
FDD	Frequency Division Duplex
F-DPCH	Fractional Dedicated Physical Channel
HS-DPCCH	Dedicated Physical Control Channel (uplink) for HS-DSCH
HS-DSCH	High Speed Downlink Shared Channel
HS-PDSCH	High Speed Physical Downlink Shared Channel
HS-SCCH	Shared Control Physical Channel for HS-DSCH
MBSFN	MBMS over a Single Frequency Network
Mcps	Mega Chip Per Second
MICH	MBMS Indication Channel
OVSF	Orthogonal Variable Spreading Factor (codes)
PICH	Page Indication Channel
PRACH	Physical Random Access Channel
PSC	Primary Synchronisation Code
RACH	Random Access Channel
SCH	Synchronisation Channel
SSC	Secondary Synchronisation Code
SF	Spreading Factor
UE	User Equipment

4 Uplink spreading and modulation

4.1 Overview

Spreading is applied to the physical channels. It consists of two operations. The first is the channelisation operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation, where a scrambling code is applied to the spread signal.

With the channelisation, data symbols on so-called I- and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I- and Q-branches are further multiplied by complex-valued scrambling code, where I and Q denote real and imaginary parts, respectively.

4.2 Spreading

4.2.1 Dedicated physical channels

The possible combinations of the maximum number of respective dedicated physical channels which may be configured simultaneously for a UE in addition to the DPCCH are specified in table 0. The actual UE capability may be lower than the values specified in table 0; the actual dedicated physical channel configuration is indicated by higher layer signalling. The actual number of configured DPDCHs, denoted $N_{max\text{-}dpdch}$, is equal to the largest number of DPDCHs from all the TFCs in the TFCS. $N_{max\text{-}dpdch}$ is not changed by frame-by-frame TFCI change or temporary TFC restrictions.

Table 0: Maximum number of simultaneously-configured uplink dedicated channels

	DPDCH	HS-DPCCH	E-DPDCH	E-DPCCH
Case 1	6	1	-	-
Case 2	1	1	2	1
Case 3	-	1	4	1

Figure 1 illustrates the principle of the spreading of uplink dedicated physical channels (DPCCH, DPDCHs, HS-DPCCH, E-DPCCH, E-DPDCHs).

In case of BPSK modulation , the binary input sequences of all physical channels are converted to real valued sequences, i.e. the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value –1, and the value "DTX" (HS-DPCCH only) is mapped to the real value 0.

In case of 4PAM modulation, the binary input sequences of all E-DPDCH physical channels are converted to real valued sequences, i.e. a set of two consecutive binary symbols n_k, n_{k+1} (with k mod 2 = 0) in each binary sequence is converted to a real valued sequence following the mapping described in Table 0A.

Table 0A: Mapping of E-DPDCH with 4PAM modulation

n_k, n_{k+1}	Mapped real value
00	0.4472
01	1.3416
10	-0.4472
11	-1.3416

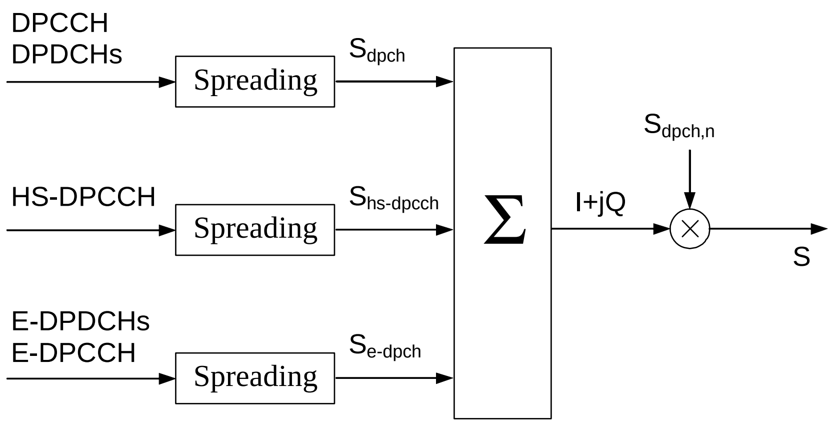

Figure 1: Spreading for uplink dedicated channels

The spreading operation is specified in subclauses 4.2.1.1 to 4.2.1.3 for each of the dedicated physical channels; it includes a spreading stage, a weighting stage, and an IQ mapping stage. In the process, the streams of real-valued chips on the I and Q branches are summed; this results in a complex-valued stream of chips for each set of channels.

As described in figure 1, the resulting complex-valued streams S_{dpch}, $S_{hs\text{-}dpcch}$ and $S_{e\text{-}dpch}$ are summed into a single complex-valued stream which is then scrambled by the complex-valued scrambling code $S_{dpch,n}$. The scrambling code shall be applied aligned with the radio frames, i.e. the first scrambling chip corresponds to the beginning of a radio frame.

NOTE: Although subclause 4.2.1 has been reorganized in this release, the spreading operation for the DPCCH, DPDCH remains unchanged as compared to the previous release.

4.2.1.1 DPCCH/DPDCH

Figure 1a illustrates the spreading operation for the uplink DPCCH and DPDCHs.

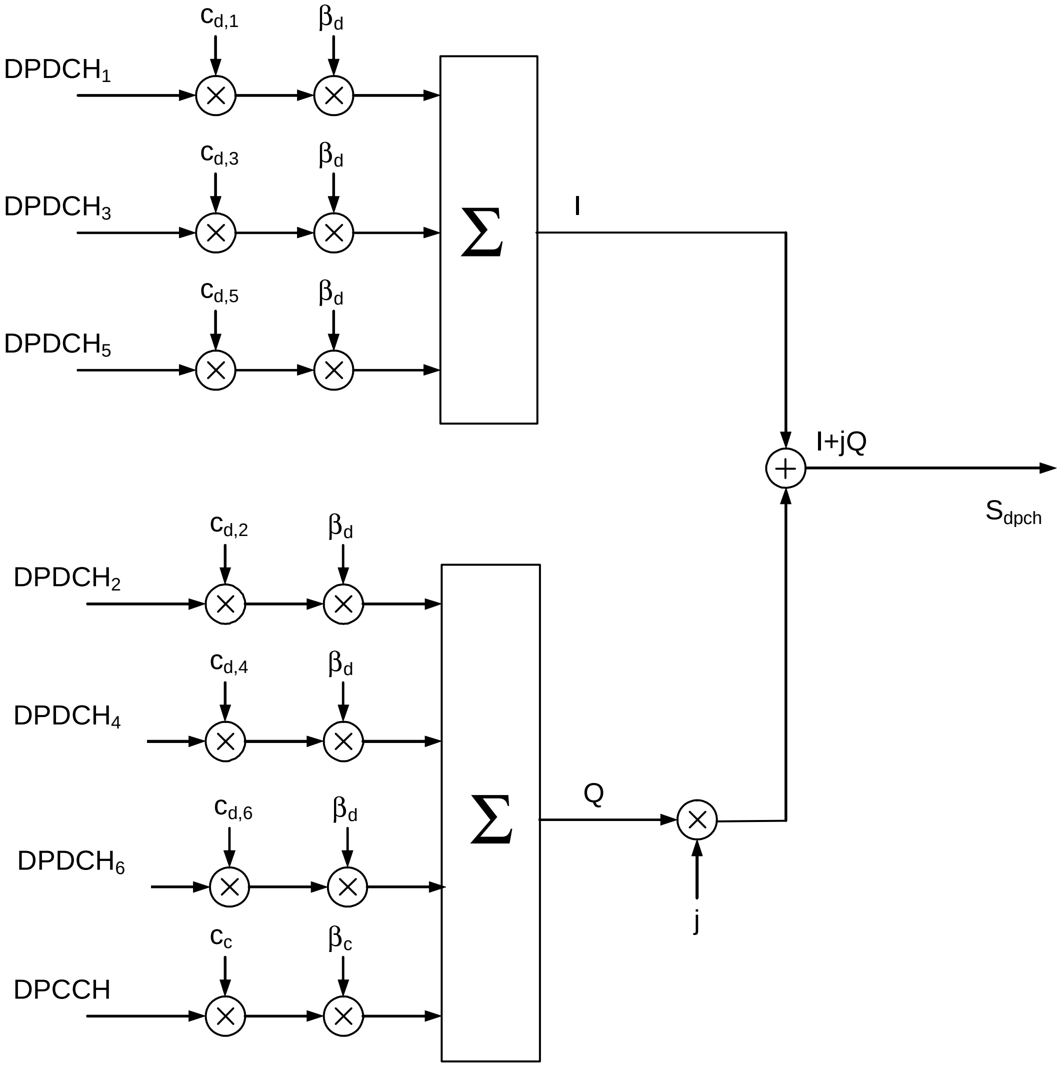

Figure 1A: Spreading for uplink DPCCH/DPDCHs

The DPCCH is spread to the chip rate by the channelisation code c_c. The *n*:th DPDCH called $DPDCH_n$ is spread to the chip rate by the channelisation code $c_{d,n}$.

After channelisation, the real-valued spread signals are weighted by gain factors, β_c for DPCCH, β_d for all DPDCHs.

The β_c and β_d values are signalled by higher layers or derived as described in [6] 5.1.2.5 and 5.1.2.5C. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β_c and β_d values are quantized into 4 bit words. The quantization steps are given in table 1.

Table 1: The quantization of the gain parameters

Signalled values for β_c and β_d	Quantized amplitude ratios β_c and β_d
15	1.0
14	14/15
13	13/15
12	12/15
11	11/15
10	10/15
9	9/15
8	8/15
7	7/15
6	6/15
5	5/15
4	4/15
3	3/15
2	2/15
1	1/15
0	Switch off

4.2.1.2 HS-DPCCH

Figure 1b illustrates the spreading operation for the HS-DPCCH.

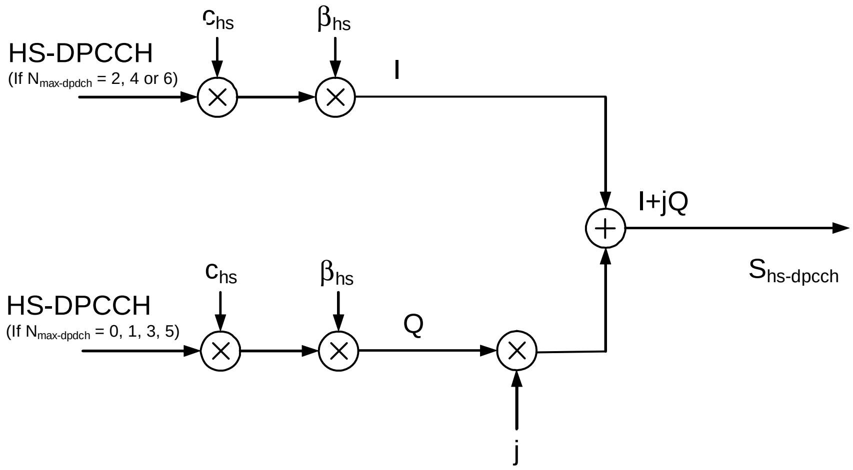

Figure 1B: Spreading for uplink HS-DPCCH

The HS-DPCCH shall be spread to the chip rate by the channelisation code c_{hs}.

After channelisation, the real-valued spread signals are weighted by gain factor β_{hs}

The β_{hs} values are derived from the quantized amplitude ratios A_{hs} which are translated from Δ_{ACK} , Δ_{NACK} and Δ_{CQI} signalled by higher layers as described in [6] 5.1.2.5A.

The translation of Δ_{ACK}, Δ_{NACK} and Δ_{CQI} into quantized amplitude ratios $A_{hs} = \beta_{hs}/\beta_c$ is shown in Table 1A.

Table 1A: The quantization of the power offset

Signalled values for Δ_{ACK}, Δ_{NACK} and Δ_{CQI}	Quantized amplitude ratios $A_{hs} = \beta_{hs}/\beta_c$
9	38/15
8	30/15
7	24/15
6	19/15
5	15/15
4	12/15
3	9/15
2	8/15
1	6/15
0	5/15

HS-DPCCH shall be mapped to the I branch in case $N_{max\text{-}dpdch}$ is 2, 4 or 6, and to the Q branch otherwise ($N_{max\text{-}dpdch}$ = 0, 1, 3 or 5).

4.2.1.3 E-DPDCH/E-DPCCH

Figure 1C illustrates the spreading operation for the E-DPDCHs and the E-DPCCH.

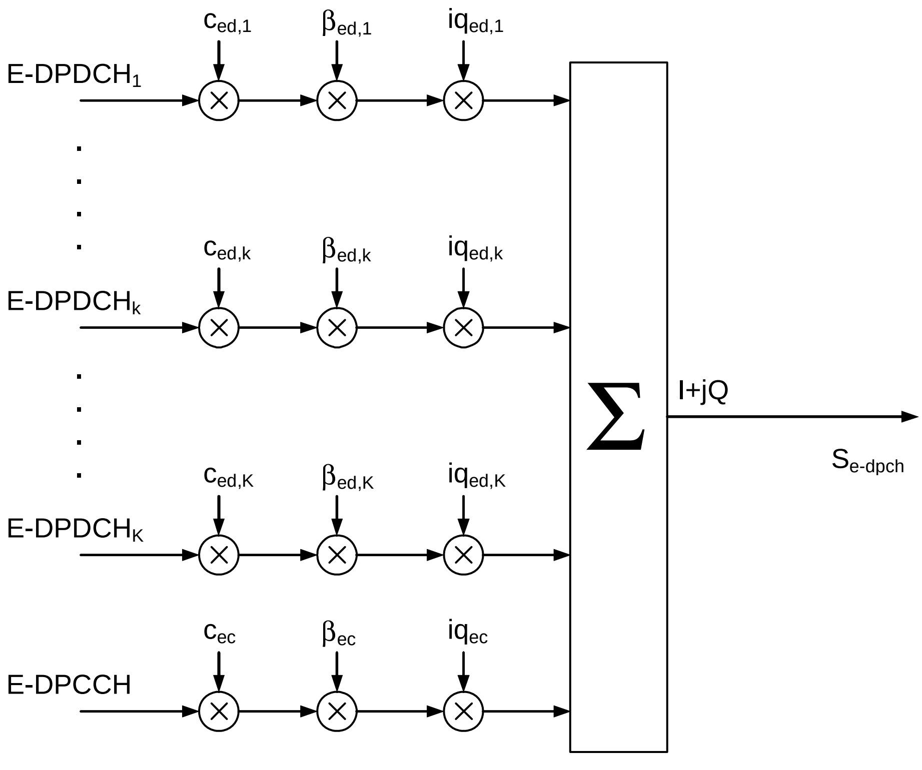

Figure 1C: Spreading for E-DPDCH/E-DPCCH

The E-DPCCH shall be spread to the chip rate by the channelisation code c_{ec}. The *k*:th E-DPDCH, denominated E-DPDCH$_k$, shall be spread to the chip rate using channelisation code $c_{ed,k}$.

After channelisation, the real-valued spread E-DPCCH and E-DPDCH$_k$ signals shall respectively be weighted by gain factor β_{ec} and $\beta_{ed,k}$.

When E-TFCI ≤ $E\text{-}TFCI_{ec,boost}$, where $E\text{-}TFCI_{ec,boost}$ is signalled by higher layers, the value of β_{ec} shall be derived as specified in [6] based on the quantized amplitude ratio A_{ec} which is translated from $\Delta_{E\text{-}DPCCH}$ signalled by higher layers. The translation of $\Delta_{E\text{-}DPCCH}$ into quantized amplitude ratios $A_{ec} = \beta_{ec}/\beta_c$ is specified in Table 1B.

Table 1B: Quantization for $\Delta_{E\text{-}DPCCH}$ for E-TFCI ≤ *E-TFCI$_{ec,boost}$*

Signalled values for $\Delta_{E\text{-}DPCCH}$	Quantized amplitude ratios $A_{ec} = \beta_{ec}/\beta_c$
8	30/15
7	24/15
6	19/15
5	15/15
4	12/15
3	9/15
2	8/15
1	6/15
0	5/15

When E-TFCI > *E-TFCI$_{ec,boost}$* , in order to provide an enhanced phase reference, the value of β_{ec} shall be derived as specified in [6] based on a traffic to total pilot power offset Δ_{T2TP}, configured by higher layers as specified in Table 1B.0 and the quantization of the ratio β_{ec}/β_c as specified in Table 1B.0A.

Table 1B.0: Δ_{T2TP}

Signalled values for Δ_{T2TP}	Power offset values Δ_{T2TP} [dB]
6	16
5	15
4	14
3	13
2	12
1	11
0	10

Table 1B.0A: Quantization for β_{ec}/β_c for E-TFCI > *E-TFCI$_{ec,boost}$*

Quantized amplitude ratios β_{ec}/β_c	E-DPDCH modulation schemes which may be used in the same subframe
239/15	4PAM
190/15	4PAM
151/15	4PAM
120/15	BPSK, 4PAM
95/15	BPSK, 4PAM
76/15	BPSK, 4PAM
60/15	BPSK, 4PAM
48/15	BPSK, 4PAM
38/15	BPSK, 4PAM
30/15	BPSK, 4PAM
24/15	BPSK, 4PAM
19/15	BPSK, 4PAM
15/15	BPSK, 4PAM
12/15	BPSK, 4PAM
9/15	BPSK
8/15	BPSK, 4PAM
6/15	BPSK, 4PAM
5/15	BPSK

The value of $\beta_{ed,k}$ shall be computed as specified in [6] subclause 5.1.2.5B.2, based on the reference gain factors, the spreading factor for E-DPDCH$_k$, the HARQ offsets, and the quantization of the ratio $\beta_{ed,k}/\beta_c$ into amplitude ratios specified in Table 1B.2 for the case when E-TFCI ≤ *E-TFCI$_{ec,boost}$* and Table 1.B.2B, for the case when E-TFCI > *E-TFCI$_{ec,boost}$*.

The reference gain factors are derived from the quantised amplitude ratios A_{ed} which is translated from $\Delta_{E\text{-}DPDCH}$ signalled by higher layers. The translation of $\Delta_{E\text{-}DPDCH}$ into quantized amplitude ratios $A_{ed} = \beta_{ed}/\beta_c$ is specified in Table 1B.1 for the case when E-TFCI ≤ $E\text{-}TFCI_{ec,boost}$ and Table 1.B.2A for the case when E-TFCI > $E\text{-}TFCI_{ec,boost}$

Table 1B.1: Quantization for $\Delta_{E\text{-}DPDCH}$ for E-TFCI ≤ $E\text{-}TFCI_{ec,boost}$

Signalled values for $\Delta_{E\text{-}DPDCH}$	Quantized amplitude ratios $A_{ed} = \beta_{ed}/\beta_c$	E-DPDCH modulation schemes which may be used in the same subframe
29	168/15	BPSK
28	150/15	BPSK
27	134/15	BPSK
26	119/15	BPSK
25	106/15	BPSK
24	95/15	BPSK
23	84/15	BPSK
22	75/15	BPSK
21	67/15	BPSK
20	60/15	BPSK
19	53/15	BPSK, 4PAM
18	47/15	BPSK, 4PAM
17	42/15	BPSK, 4PAM
16	38/15	BPSK, 4PAM
15	34/15	BPSK, 4PAM
14	30/15	BPSK, 4PAM
13	27/15	BPSK, 4PAM
12	24/15	BPSK, 4PAM
11	21/15	BPSK, 4PAM
10	19/15	BPSK, 4PAM
9	17/15	BPSK
8	15/15	BPSK
7	13/15	BPSK
6	12/15	BPSK
5	11/15	BPSK
4	9/15	BPSK
3	8/15	BPSK
2	7/15	BPSK
1	6/15	BPSK
0	5/15	BPSK

Table 1B.2: Quantization for $\beta_{ed,k}/\beta_c$ for E-TFCI ≤ $E\text{-}TFCI_{ec,boost}$

Quantized amplitude ratios $\beta_{ed,k}/\beta_c$	E-DPDCH modulation schemes which may be used in the same subframe
168/15	BPSK
150/15	BPSK
134/15	BPSK
119/15	BPSK
106/15	BPSK
95/15	BPSK
84/15	BPSK
75/15	BPSK
67/15	BPSK
60/15	BPSK
53/15	BPSK, 4PAM
47/15	BPSK, 4PAM
42/15	BPSK, 4PAM
38/15	BPSK, 4PAM
34/15	BPSK, 4PAM
30/15	BPSK, 4PAM
27/15	BPSK, 4PAM
24/15	BPSK, 4PAM
21/15	BPSK, 4PAM
19/15	BPSK, 4PAM
17/15	BPSK
15/15	BPSK
13/15	BPSK
12/15	BPSK
11/15	BPSK
9/15	BPSK
8/15	BPSK
7/15	BPSK
6/15	BPSK
5/15	BPSK

Table 1B.2A: Quantization for $\Delta_{E\text{-}DPDCH}$ for E-TFCI > $E\text{-}TFCI_{ec,boost}$

Signalled values for $\Delta_{E\text{-}DPDCH}$	Quantized amplitude ratios $A_{ed} = \beta_{ed}/\beta_c$	E-DPDCH modulation schemes which may be used in the same subframe
31	377/15	4PAM
30	336/15	4PAM
29	299/15	4PAM
28	267/15	BPSK, 4PAM
27	237/15	BPSK, 4PAM
26	212/15	BPSK, 4PAM
25	189/15	BPSK, 4PAM
24	168/15	BPSK, 4PAM
23	150/15	BPSK, 4PAM
22	134/15	BPSK, 4PAM
21	119/15	BPSK, 4PAM
20	106/15	BPSK, 4PAM
19	95/15	BPSK, 4PAM
18	84/15	BPSK, 4PAM
17	75/15	BPSK, 4PAM
16	67/15	BPSK, 4PAM
15	60/15	BPSK, 4PAM
14	53/15	BPSK, 4PAM
13	47/15	BPSK, 4PAM
12	42/15	BPSK, 4PAM
11	38/15	BPSK
10	34/15	BPSK
9	30/15	BPSK
8	27/15	BPSK
7	24/15	BPSK
6	21/15	BPSK
5	19/15	BPSK
4	17/15	BPSK
3	15/15	BPSK
2	13/15	BPSK
1	11/15	BPSK
0	8/15	BPSK

Table 1B.2B: Quantization for $\beta_{ed,k}/\beta_c$ for E-TFCI > $E\text{-}TFCI_{ec,boost}$

Quantized amplitude ratios $\beta_{ed,k}/\beta_c$	E-DPDCH modulation schemes which may be used in the same subframe
377/15	4PAM
336/15	4PAM
299/15	4PAM
267/15	BPSK, 4PAM
237/15	BPSK, 4PAM
212/15	BPSK, 4PAM
189/15	BPSK, 4PAM
168/15	BPSK, 4PAM
150/15	BPSK, 4PAM
134/15	BPSK, 4PAM
119/15	BPSK, 4PAM
106/15	BPSK, 4PAM
95/15	BPSK, 4PAM
84/15	BPSK, 4PAM
75/15	BPSK, 4PAM
67/15	BPSK, 4PAM
60/15	BPSK, 4PAM
53/15	BPSK, 4PAM
47/15	BPSK, 4PAM
42/15	BPSK, 4PAM
38/15	BPSK
34/15	BPSK
30/15	BPSK
27/15	BPSK
24/15	BPSK
21/15	BPSK
19/15	BPSK
17/15	BPSK
15/15	BPSK
13/15	BPSK
11/15	BPSK
8/15	BPSK

The HARQ offsets Δ_{harq} to be used for support of different HARQ profile are configured by higher layers as specified in Table 1B.3.

Table 1B.3: HARQ offset Δ_{harq}

Signalled values for Δ_{harq}	Power offset values Δ_{harq} [dB]
6	6
5	5
4	4
3	3
2	2
1	1
0	0

After weighting, the real-valued spread signals shall be mapped to the I branch or the Q branch according to the iq_{ec} value for the E-DPCCH and to $iq_{ed,k}$ for E-DPDCH$_k$ and summed together.

The E-DPCCH shall always be mapped to the I branch, i.e. $iq_{ec} = 1$.

The IQ branch mapping for the E-DPDCHs depends on $N_{max\text{-}dpdch}$ and on whether an HS-DSCH is configured for the UE; the IQ branch mapping shall be as specified in table 1C.

Table 1C: IQ branch mapping for E-DPDCH

$N_{max\text{-}dpdch}$	HS-DSCH configured	$E\text{-}DPDCH_k$	$iq_{ed,k}$
0	No/Yes	$E\text{-}DPDCH_1$	1
		$E\text{-}DPDCH_2$	j
		$E\text{-}DPDCH_3$	1
		$E\text{-}DPDCH_4$	j
1	No	$E\text{-}DPDCH_1$	j
		$E\text{-}DPDCH_2$	1
1	Yes	$E\text{-}DPDCH_1$	1
		$E\text{-}DPDCH_2$	j

NOTE: In case the UE transmits more than 2 E-DPDCHs, the UE then always transmits $E\text{-}DPDCH_3$ and $E\text{-}DPDCH_4$ simultaneously.

4.2.2 PRACH

4.2.2.1 PRACH preamble part

The PRACH preamble part consists of a complex-valued code, described in subclause 4.3.3.

4.2.2.2 PRACH message part

Figure 2 illustrates the principle of the spreading and scrambling of the PRACH message part, consisting of data and control parts. The binary control and data parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value –1. The control part is spread to the chip rate by the channelisation code c_c, while the data part is spread to the chip rate by the channelisation code c_d.

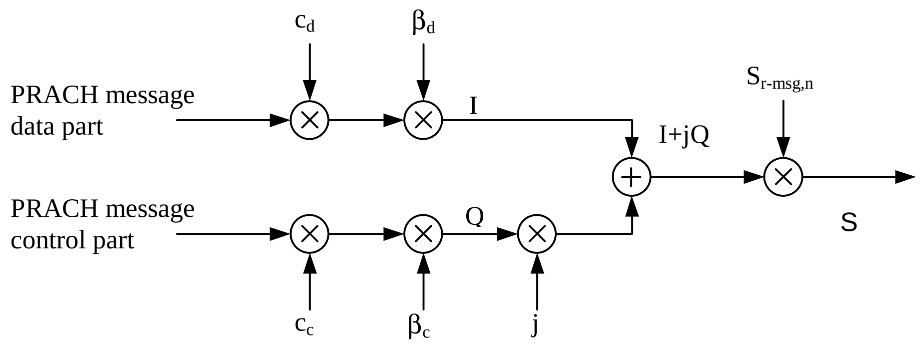

Figure 2: Spreading of PRACH message part

After channelisation, the real-valued spread signals are weighted by gain factors, β_c for the control part and β_d for the data part. At every instant in time, at least one of the values β_c and β_d has the amplitude 1.0. The β-values are quantized into 4 bit words. The quantization steps are given in subclause 4.2.1.

After the weighting, the stream of real-valued chips on the I- and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code $S_{r\text{-}msg,n}$. The 10 ms scrambling code is applied aligned with the 10 ms message part radio frames, i.e. the first scrambling chip corresponds to the beginning of a message part radio frame.

4.2.3 Void

4.3 Code generation and allocation

4.3.1 Channelisation codes

4.3.1.1 Code definition

The channelisation codes of figure 1 are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between a user"s different physical channels. The OVSF codes can be defined using the code tree of figure 4.

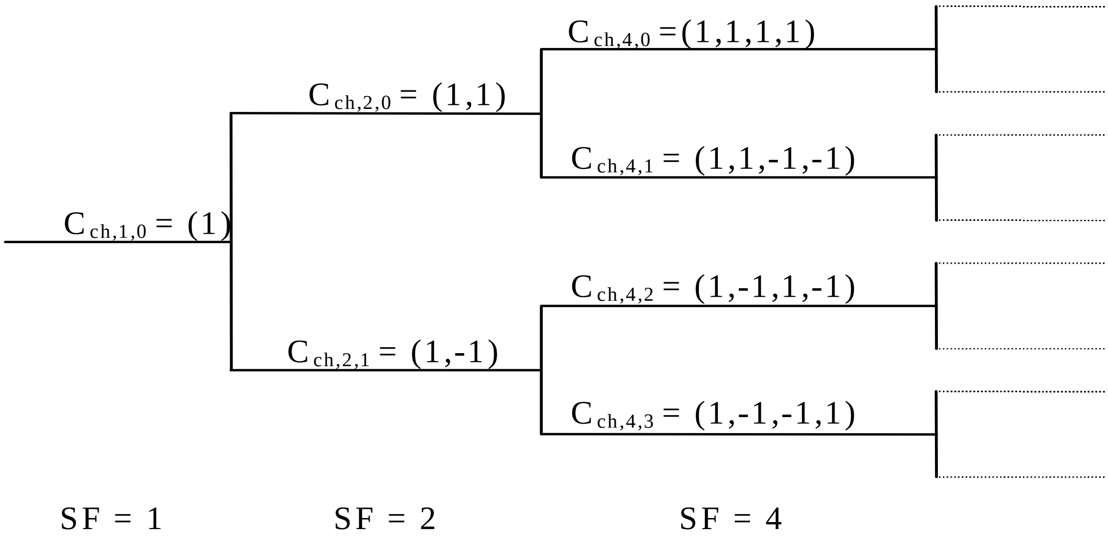

Figure 4: Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes

In figure 4, the channelisation codes are uniquely described as $C_{ch,SF,k}$, where SF is the spreading factor of the code and k is the code number, $0 \le k \le SF-1$.

Each level in the code tree defines channelisation codes of length SF, corresponding to a spreading factor of SF in figure 4.

The generation method for the channelisation code is defined as:

$$C_{ch,1,0} = 1,$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2^{(n+1)},0} \\ C_{ch,2^{(n+1)},1} \\ C_{ch,2^{(n+1)},2} \\ C_{ch,2^{(n+1)},3} \\ \vdots \\ C_{ch,2^{(n+1)},2^{(n+1)}-2} \\ C_{ch,2^{(n+1)},2^{(n+1)}-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix}$$

The leftmost value in each channelisation code word corresponds to the chip transmitted first in time.

4.3.1.2 Code allocation for dedicated physical channels

NOTE: Although subclause 4.3.1.2 has been reorganized in this release, the spreading operation for DPCCH and DPDCH remains unchanged as compared to the previous release.

4.3.1.2.1 Code allocation for DPCCH/DPDCH

For the DPCCH and DPDCHs the following applies:

- The DPCCH shall always be spread by code $c_c = C_{ch,256,0.}$
- When only one DPDCH is to be transmitted, $DPDCH_1$ shall be spread by code $c_{d,1} = C_{ch,SF,k}$ where SF is the spreading factor of $DPDCH_1$ and k= SF / 4.
- When more than one DPDCH is to be transmitted, all DPDCHs have spreading factors equal to 4. $DPDCH_n$ shall be spread by the the code $c_{d,n} = C_{ch,4,k}$, where $k = 1$ if $n \in \{1, 2\}$, $k = 3$ if $n \in \{3, 4\}$, and $k = 2$ if $n \in \{5, 6\}$.

If a power control preamble is used to initialise a DCH, the channelisation code for the DPCCH during the power control preamble shall be the same as that to be used afterwards.

4.3.1.2.2 Code allocation for HS-DPCCH

The HS-DPCCH shall be spread with code c_{hs} as specified in table 1D.

Table 1D: channelisation code of HS-DPCCH

$N_{max\text{-}dpdch}$ (as defined in subclause 4.2.1)	Channelisation code c_{hs}
0	$C_{ch,256,33}$
1	$C_{ch,256,64}$
2,4,6	$C_{ch,256,1}$
3,5	$C_{ch,256,32}$

4.3.1.2.3 Code allocation for E-DPCCH/E-DPDCH

The E-DPCCH shall be spread with channelisation code $c_{ec} = C_{ch,256,1}$.

$E\text{-}DPDCH_k$ shall be spread with channelisation code $c_{ed,k}$. The sequence $c_{ed,k}$ depends on $N_{max\text{-}dpdch}$ and the spreading factor selected for the corresponding frame or sub-frame as specified in [7]; it shall be selected according to table 1E.

Table 1E: Channelisation code for E-DPDCH

$N_{max\text{-}dpdch}$	$E\text{-}DPDCH_k$	Channelisation code $C_{ed,k}$
0	$E\text{-}DPDCH_1$	$C_{ch,SF,SF/4}$ if SF ≥ 4 $C_{ch,2,1}$ if SF = 2
	$E\text{-}DPDCH_2$	$C_{ch,4,1}$ if SF = 4 $C_{ch,2,1}$ if SF = 2
	$E\text{-}DPDCH_3$ $E\text{-}DPDCH_4$	$C_{ch,4,1}$
1	$E\text{-}DPDCH_1$	$C_{ch,SF,SF/2}$
	$E\text{-}DPDCH_2$	$C_{ch,4,2}$ if SF = 4 $C_{ch,2,1}$ if SF = 2

NOTE: When more than one E-DPDCH is transmitted, the respective channelisation codes used for $E\text{-}DPDCH_1$ and $E\text{-}DPDCH_2$ are always the same.

4.3.1.3 Code allocation for PRACH message part

The preamble signature *s*, $0 \leq s \leq 15$, points to one of the 16 nodes in the code-tree that corresponds to channelisation codes of length 16. The sub-tree below the specified node is used for spreading of the message part. The control part is spread with the channelisation code c_c (as shown in subclause 4.2.2.2) of spreading factor 256 in the lowest branch of the sub-tree, i.e. $c_c = C_{ch,256,m}$ where m = 16×s + 15. The data part uses any of the channelisation codes from spreading factor 32 to 256 in the upper-most branch of the sub-tree. To be exact, the data part is spread by channelisation code $c_d = C_{ch,SF,m}$ and SF is the spreading factor used for the data part and m = SF×s/16.

4.3.1.4 Void

4.3.1.5 Void

4.3.2 Scrambling codes

4.3.2.1 General

All uplink physical channels shall be scrambled with a complex-valued scrambling code. The dedicated physical channels may be scrambled by either a long or a short scrambling code, defined in subclause 4.3.2.4. The PRACH message part shall be scrambled with a long scrambling code, defined in subclause 4.3.2.5. There are 2^{24} long and 2^{24} short uplink scrambling codes. Uplink scrambling codes are assigned by higher layers.

The long scrambling code is built from constituent long sequences defined in subclause 4.3.2.2, while the constituent short sequences used to build the short scrambling code are defined in subclause 4.3.2.3.

4.3.2.2 Long scrambling sequence

The long scrambling sequences $c_{long,1,n}$ and $c_{long,2,n}$ are constructed from position wise modulo 2 sum of 38400 chip segments of two binary *m*-sequences generated by means of two generator polynomials of degree 25. Let *x*, and *y* be the two *m*-sequences respectively. The *x* sequence is constructed using the primitive (over GF(2)) polynomial $X^{25}+X^3+1$. The *y* sequence is constructed using the polynomial $X^{25}+X^3+X^2+X+1$. The resulting sequences thus constitute segments of a set of Gold sequences.

The sequence $c_{long,2,n}$ is a 16777232 chip shifted version of the sequence $c_{long,1,n}$.

Let $n_{23} \ldots n_0$ be the 24 bit binary representation of the scrambling sequence number *n* with n_0 being the least significant bit. The *x* sequence depends on the chosen scrambling sequence number *n* and is denoted x_n, in the sequel. Furthermore, let $x_n(i)$ and $y(i)$ denote the *i*:th symbol of the sequence x_n and *y*, respectively.

The *m*-sequences x_n and *y* are constructed as:

Initial conditions:

- $x_n(0)=n_0$, $x_n(1)= n_1$, … $=x_n(22)= n_{22}$,$x_n(23)= n_{23}$, $x_n(24)=1$.

- y(0)=y(1)= … =y(23)= y(24)=1.

Recursive definition of subsequent symbols:

- $x_n(i+25) =x_n(i+3) + x_n(i)$ modulo 2, i=0,…, 2^{25}-27.

- y(i+25) = y(i+3)+y(i+2) +y(i+1) +y(i) modulo 2, i=0,…, 2^{25}-27.

Define the binary Gold sequence z_n by:

- $z_n(i) = x_n(i) + y(i)$ modulo 2, $i = 0, 1, 2, \ldots, 2^{25}-2$.

The real valued Gold sequence Z_n is defined by:

$$Z_n(i) = \begin{cases} +1 & if \ z_n(i) = 0 \\ -1 & if \ z_n(i) = 1 \end{cases} \quad for \ \ i = 0,1,\ldots,2^{25}-2.$$

Now, the real-valued long scrambling sequences $c_{long,1,n}$ and $c_{long,2,n}$ are defined as follows:

$$c_{long,1,n}(i) = Z_n(i), \; i = 0, 1, 2, \ldots, 2^{25} - 2 \text{ and}$$

$$c_{long,2,n}(i) = Z_n((i + 16777232) \text{ modulo } (2^{25} - 1)), \; i = 0, 1, 2, \ldots, 2^{25} - 2.$$

Finally, the complex-valued long scrambling sequence $C_{long, n}$, is defined as:

$$C_{long,n}(i) = c_{long,1,n}(i)\left(1 + j(-1)^i c_{long,2,n}\left(2\lfloor i/2 \rfloor\right)\right)$$

where $i = 0, 1, \ldots, 2^{25} - 2$ and $\lfloor\,\rfloor$ denotes rounding to nearest lower integer.

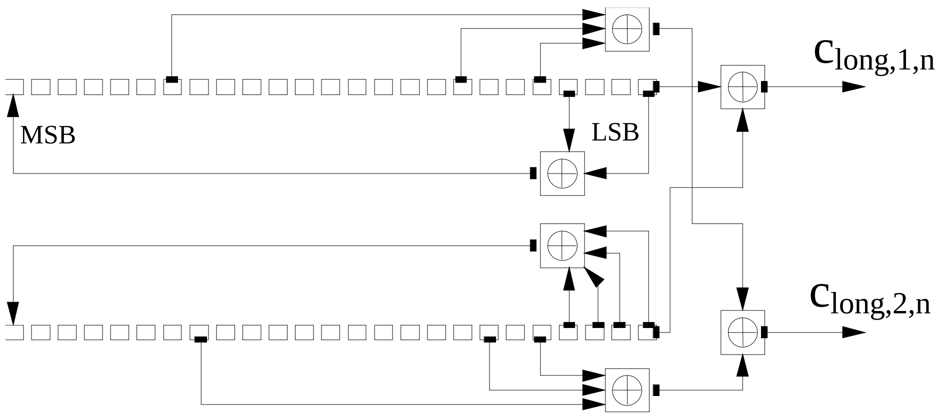

Figure 5: Configuration of uplink scrambling sequence generator

4.3.2.3 Short scrambling sequence

The short scrambling sequences $c_{short,1,n}(i)$ and $c_{short,2,n}(i)$ are defined from a sequence from the family of periodically extended S(2) codes.

Let $n_{23}n_{22}\ldots n_0$ be the 24 bit binary representation of the code number n.

The n:th quaternary S(2) sequence $z_n(i)$, $0 \le n \le 16777215$, is obtained by modulo 4 addition of three sequences, a quaternary sequence $a(i)$ and two binary sequences $b(i)$ and $d(i)$, where the initial loading of the three sequences is determined from the code number n. The sequence $z_n(i)$ of length 255 is generated according to the following relation:

- $z_n(i) = a(i) + 2b(i) + 2d(i)$ modulo 4, $i = 0, 1, \ldots, 254$;

where the quaternary sequence $a(i)$ is generated recursively by the polynomial $g_0(x) = x^8+3x^5+x^3+3x^2+2x+3$ as:

- $a(0) = 2n_0 + 1$ modulo 4;
- $a(i) = 2n_i$ modulo 4, $i = 1, 2, \ldots, 7$;
- $a(i) = 3a(i\text{-}3) + a(i\text{-}5) + 3a(i\text{-}6) + 2a(i\text{-}7) + 3a(i\text{-}8)$ modulo 4, $i = 8, 9, \ldots, 254$;

and the binary sequence $b(i)$ is generated recursively by the polynomial $g_1(x) = x^8+x^7+x^5+x+1$ as

$b(i) = n_{8+i}$ modulo 2, $i = 0, 1, \ldots, 7$,

$b(i) = b(i\text{-}1) + b(i\text{-}3) + b(i\text{-}7) + b(i\text{-}8)$ modulo 2, $i = 8, 9, \ldots, 254$,

and the binary sequence $d(i)$ is generated recursively by the polynomial $g_2(x) = x^8+x^7+x^5+x^4+1$ as:

$d(i) = n_{16+i}$ modulo 2, $i = 0, 1, \ldots, 7$;

$d(i) = d(i\text{-}1) + d(i\text{-}3) + d(i\text{-}4) + d(i\text{-}8)$ modulo 2, $i = 8, 9, \ldots, 254$.

The sequence $z_n(i)$ is extended to length 256 chips by setting $z_n(255) = z_n(0)$.

The mapping from $z_n(i)$ to the real-valued binary sequences $c_{short,1,n}(i)$ and $c_{short,2,n}(i)$, , i = 0, 1, …, 255 is defined in Table 2.

Table 2: Mapping from $z_n(i)$ to $c_{short,1,n}(i)$ and $c_{short,2,n}(i)$, i = 0, 1, …, 255

$z_n(i)$	$c_{short,1,n}(i)$	$c_{short,2,n}(i)$
0	+1	+1
1	-1	+1
2	-1	-1
3	+1	-1

Finally, the complex-valued short scrambling sequence $C_{short,\ n}$, is defined as:

$$C_{short,n}(i) = c_{short,1,n}(i \bmod 256)\left(1 + j(-1)^i c_{short,2,n}\left(2\left\lfloor (i \bmod 256)/2 \right\rfloor\right)\right)$$

where i = 0, 1, 2, … and $\lfloor\ \rfloor$ denotes rounding to nearest lower integer.

An implementation of the short scrambling sequence generator for the 255 chip sequence to be extended by one chip is shown in Figure 6.

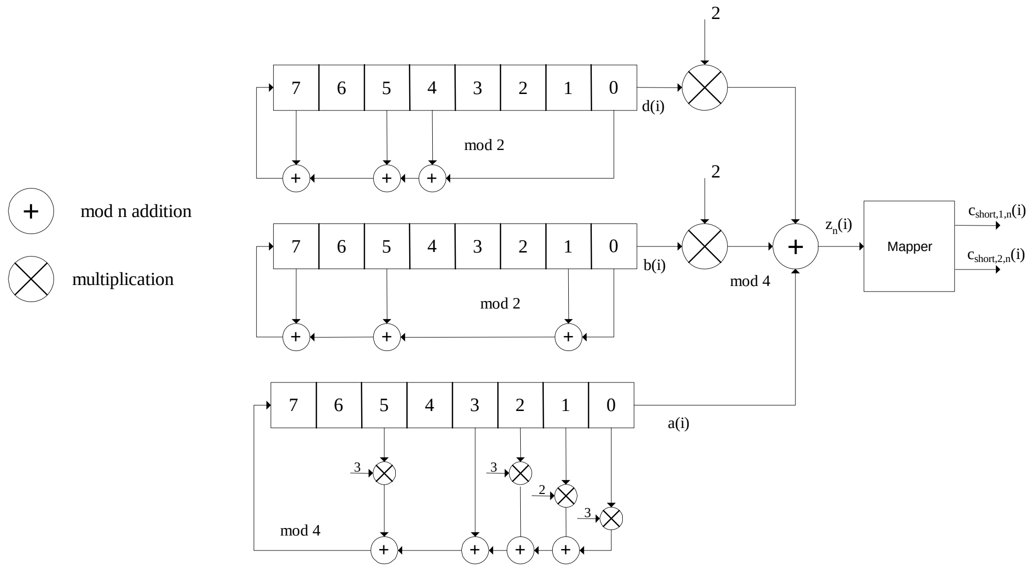

Figure 6: Uplink short scrambling sequence generator for 255 chip sequence

4.3.2.4 Dedicated physical channels scrambling code

The code used for scrambling of the uplink dedicated physical channels may be of either long or short type. The n:th uplink scrambling code, denoted $S_{dpch,\ n}$, is defined as:

$S_{dpch,n}(i) = C_{long,n}(i)$, i = 0, 1, …, 38399, when using long scrambling codes;

where the lowest index corresponds to the chip transmitted first in time and $C_{long,n}$ is defined in subclause 4.3.2.2.

The n:th uplink scrambling code, denoted $S_{dpch,\ n}$, is defined as:

$S_{dpch,n}(i) = C_{short,n}(i)$, i = 0, 1, …, 38399, when using short scrambling codes;

where the lowest index corresponds to the chip transmitted first in time and $C_{short,n}$ is defined in subclause 4.3.2.3.

4.3.2.5 PRACH message part scrambling code

The scrambling code used for the PRACH message part is 10 ms long, and there are 8192 different PRACH scrambling codes defined.

The *n*:th PRACH message part scrambling code, denoted $S_{r\text{-}msg,n}$, where $n = 0, 1, \ldots, 8191$, is based on the long scrambling sequence and is defined as:

$$S_{r\text{-}msg,n}(i) = C_{long,n}(i + 4096), \quad i = 0, 1, \ldots, 38399$$

where the lowest index corresponds to the chip transmitted first in time and $C_{long,n}$ is defined in subclause 4.3.2.2.

The message part scrambling code has a one-to-one correspondence to the scrambling code used for the preamble part. For one PRACH, the same code number is used for both scrambling codes, i.e. if the PRACH preamble scrambling code used is $S_{r\text{-}pre,m}$ then the PRACH message part scrambling code is $S_{r\text{-}msg,m}$, where the number *m* is the same for both codes.

4.3.2.6 Void

4.3.2.7 Void

4.3.3 PRACH preamble codes

4.3.3.1 Preamble code construction

The random access preamble code $C_{pre,n,}$ is a complex valued sequence. It is built from a preamble scrambling code $S_{r\text{-}pre,n}$ and a preamble signature $C_{sig,s}$ as follows:

- $C_{pre,n,s}(k) = S_{r\text{-}pre,n}(k) \times C_{sig,s}(k) \times e^{j(\frac{\pi}{4}+\frac{\pi}{2}k)}$, k = 0, 1, 2, 3, …, 4095;

where k=0 corresponds to the chip transmitted first in time and $S_{r\text{-}pre,n}$ and $C_{sig,s}$ are defined in 4.3.3.2 and 4.3.3.3 below respectively.

4.3.3.2 Preamble scrambling code

The scrambling code for the PRACH preamble part is constructed from the long scrambling sequences. There are 8192 PRACH preamble scrambling codes in total.

The *n*:th preamble scrambling code, $n = 0, 1, \ldots, 8191$, is defined as:

$S_{r\text{-}pre,n}(i) = c_{long,1,n}(i)$, $i = 0, 1, \ldots, 4095$;

where the sequence $c_{long,1,n}$ is defined in subclause 4.3.2.2.

The 8192 PRACH preamble scrambling codes are divided into 512 groups with 16 codes in each group. There is a one-to-one correspondence between the group of PRACH preamble scrambling codes in a cell and the primary scrambling code used in the downlink of the cell. The *k*:th PRACH preamble scrambling code within the cell with downlink primary scrambling code *m*, $k = 0, 1, 2, \ldots, 15$ and $m = 0, 1, 2, \ldots, 511$, is $S_{r\text{-}pre,n}(i)$ as defined above with $n = 16 \times m + k$.

4.3.3.3 Preamble signature

The preamble signature corresponding to a signature s consists of 256 repetitions of a length 16 signature $P_s(n)$, n=0…15. This is defined as follows:

- $C_{sig,s}(i) = P_s(i \text{ modulo } 16)$, $i = 0, 1, \ldots, 4095$.

The signature $P_s(n)$ is from the set of 16 Hadamard codes of length 16. These are listed in table 3.

Table 3: Preamble signatures

Preamble signature	Value of *n*															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
$P_0(n)$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$P_1(n)$	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1
$P_2(n)$	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1
$P_3(n)$	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1
$P_4(n)$	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1
$P_5(n)$	1	-1	1	-1	-1	1	-1	1	1	-1	1	-1	-1	1	-1	1
$P_6(n)$	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1
$P_7(n)$	1	-1	-1	1	-1	1	1	-1	1	-1	-1	1	-1	1	1	-1
$P_8(n)$	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1
$P_9(n)$	1	-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1
$P_{10}(n)$	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1
$P_{11}(n)$	1	-1	-1	1	1	-1	-1	1	-1	1	1	-1	-1	1	1	-1
$P_{12}(n)$	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1
$P_{13}(n)$	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	1	-1	1	-1
$P_{14}(n)$	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1
$P_{15}(n)$	1	-1	-1	1	-1	1	1	-1	-1	1	1	-1	1	-1	-1	1

4.3.4 Void

4.4 Modulation

4.4.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps.

4.4.2 Modulation

Modulation of the complex-valued chip sequence generated by the spreading process is shown in Figure 7 below:

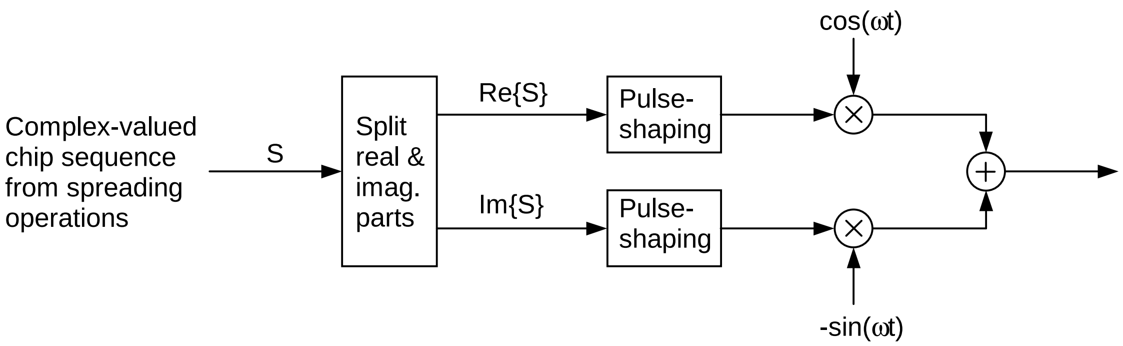

Figure 7: Uplink modulation

The pulse-shaping characteristics are described in [3].

5 Downlink spreading and modulation

5.1 Spreading

Figure 8 illustrates the spreading operation for all physical channel except SCH. The spreading operation includes a modulation mapper stage successively followed by a channelisation stage, an IQ combining stage and a scrambling stage. All the downlink physical channels are then combined as specified in sub subclause 5.1.5.

The non-spread downlink physical channels, except SCH, AICH, E-HICH and E-RGCH consist of a sequence of 3-valued digits taking the values 0, 1 and "DTX". Note that "DTX" is only applicable to those downlink physical channels that support DTX transmission.

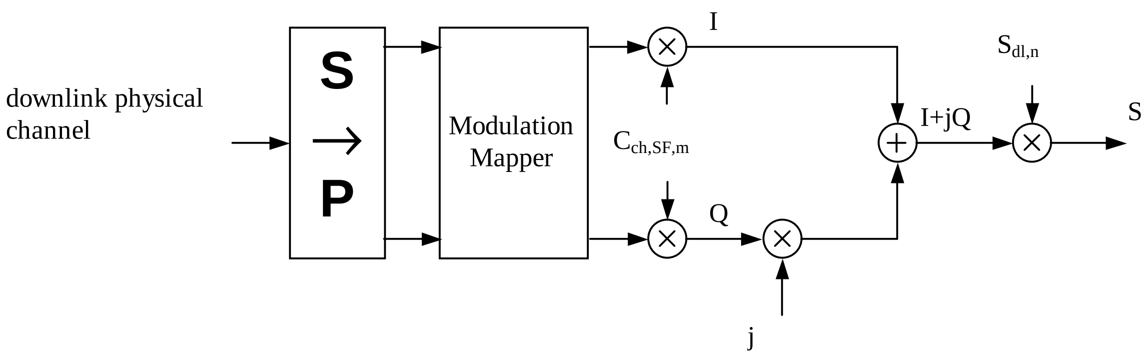

Figure 8: Spreading for all downlink physical channels except SCH

NOTE: Although subclause 5.1 has been reorganized in this release, the spreading operation as specified for the DL channels in the previous release remains unchanged.

5.1.1 Modulation mapper

Table 3A defines which of the IQ mapping specified in subclauses 5.1.1.1 and 5.1.1.2 may be used for the physical channel being processed.

Table 3A: IQ mapping

Physical channel	IQ mapping
HS-PDSCH, S-CCPCH*	QPSK, 16QAM or 64QAM
All other channels (except the SCH)	QPSK

* For MBSFN FACH transmissions, QPSK and 16QAM can be used.

5.1.1.1 QPSK

For all channels, except AICH, E-HICH and E-RGCH, the input digits shall be mapped to real-valued symbols as follows: the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value –1 and "DTX" is mapped to the real value 0.

For the indicator channels using signatures (AICH), the real-valued input symbols depend on the exact combination of the indicators to be transmitted as specified in [2] subclauses 5.3.3.7, 5.3.3.8 and 5.3.3.9.For the E-HICH and the E-RGCH the input is a real valued symbol sequence as specified in [2]

Each pair of two consecutive real-valued symbols is first converted from serial to parallel and mapped to an I and Q branch. The definition of the modulation mapper is such that even and odd numbered symbols are mapped to the I and Q branch respectively. For all QPSK channels except the indicator channels using signatures, symbol number zero is defined as the first symbol in each frame or sub-frame. For the indicator channels using signatures, symbol number zero is defined as the first symbol in each access slot.

5.1.1.2 16QAM

In case of 16QAM, a set of four consecutive binary symbols n_k, n_{k+1}, n_{k+2}, n_{k+3} (with k mod 4 = 0) is serial-to-parallel converted to two consecutive binary symbols ($i_1 = n_k$, $i_2 = n_{k+2}$) on the I branch and two consecutive binary symbols ($q_1 = n_{k+1}$, $q_2 = n_{k+3}$) on the Q branch and then mapped to 16QAM by the modulation mapper as defined in table 3B.

The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,16,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips from all multi-codes is summed and then scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. The scrambling code is applied aligned with the scrambling code applied to the P-CCPCH.

Table 3B: 16QAM modulation mapping

$i_1q_1i_2q_2$	I branch	Q branch
0000	0.4472	0.4472
0001	0.4472	1.3416
0010	1.3416	0.4472
0011	1.3416	1.3416
0100	0.4472	-0.4472
0101	0.4472	-1.3416
0110	1.3416	-0.4472
0111	1.3416	-1.3416
1000	-0.4472	0.4472
1001	-0.4472	1.3416
1010	-1.3416	0.4472
1011	-1.3416	1.3416
1100	-0.4472	-0.4472
1101	-0.4472	-1.3416
1110	-1.3416	-0.4472
1111	-1.3416	-1.3416

5.1.1.3 64QAM

In case of 64QAM, a set of six consecutive binary symbols n_k, n_{k+1}, n_{k+2}, n_{k+3}, n_{k+4}, n_{k+5} (with k mod 6 = 0) is serial-to-parallel converted to three consecutive binary symbols ($i_1 = n_k$, $i_2 = n_{k+2}$, $i_3 = n_{k+4}$) on the I branch and three consecutive binary symbols ($q_1 = n_{k+1}$, $q_2 = n_{k+3}$, $q_3 = n_{k+5}$) on the Q branch and then mapped to 64QAM by the modulation mapper as defined in table 3C.

The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,16,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips from all multi-codes is summed and then scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. The scrambling code is applied aligned with the scrambling code applied to the P-CCPCH.

Table 3C: 64QAM modulation mapping

$i_1q_1i_2q_2\ i_3q_3$	I branch	Q branch		$i_1q_1i_2q_2\ i_3q_3$	I branch	Q branch
000000	0.6547	0.6547		100000	-0.6547	0.6547
000001	0.6547	0.2182		100001	-0.6547	0.2182
000010	0.2182	0.6547		100010	-0.2182	0.6547
000011	0.2182	0.2182		100011	-0.2182	0.2182
000100	0.6547	1.0911		100100	-0.6547	1.0911
000101	0.6547	1.5275		100101	-0.6547	1.5275
000110	0.2182	1.0911		100110	-0.2182	1.0911
000111	0.2182	1.5275		100111	-0.2182	1.5275
001000	1.0911	0.6547		101000	-1.0911	0.6547
001001	1.0911	0.2182		101001	-1.0911	0.2182
001010	1.5275	0.6547		101010	-1.5275	0.6547
001011	1.5275	0.2182		101011	-1.5275	0.2182
001100	1.0911	1.0911		101100	-1.0911	1.0911
001101	1.0911	1.5275		101101	-1.0911	1.5275
001110	1.5275	1.0911		101110	-1.5275	1.0911
001111	1.5275	1.5275		101111	-1.5275	1.5275
010000	0.6547	-0.6547		110000	-0.6547	-0.6547
010001	0.6547	-0.2182		110001	-0.6547	-0.2182
010010	0.2182	-0.6547		110010	-0.2182	-0.6547
010011	0.2182	-0.2182		110011	-0.2182	-0.2182
010100	0.6547	-1.0911		110100	-0.6547	-1.0911
010101	0.6547	-1.5275		110101	-0.6547	-1.5275
010110	0.2182	-1.0911		110110	-0.2182	-1.0911
010111	0.2182	-1.5275		110111	-0.2182	-1.5275
011000	1.0911	-0.6547		111000	-1.0911	-0.6547
011001	1.0911	-0.2182		111001	-1.0911	-0.2182
011010	1.5275	-0.6547		111010	-1.5275	-0.6547
011011	1.5275	-0.2182		111011	-1.5275	-0.2182
011100	1.0911	-1.0911		111100	-1.0911	-1.0911
011101	1.0911	-1.5275		111101	-1.0911	-1.5275
011110	1.5275	-1.0911		111110	-1.5275	-1.0911
011111	1.5275	-1.5275		111111	-1.5275	-1.5275

5.1.2 Channelisation

For all physical channels (except SCH) the I and Q branches shall be spread to the chip rate by the same real-valued channelisation code $C_{ch,SF,m}$, i.e. the output for each input symbol on the I and the Q branches shall be a sequence of SF chips corresponding to the channelisation code chip sequence multiplied by the real-valued symbol. The channelisation code sequence shall be aligned in time with the symbol boundary.

5.1.3 IQ combining

The real valued chip sequence on the Q branch shall be complex multiplied with j and summed with the corresponding real valued chip sequence on the I branch, thus resulting in a single complex valued chip sequence.

5.1.4 Scrambling

The sequence of complex valued chips shall be scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. In case of P-CCPCH, the scrambling code shall be applied aligned with the P-CCPCH frame boundary, i.e. the first complex chip of the spread P-CCPCH frame is multiplied with chip number zero of the scrambling code. In case of other downlink channels, the scrambling code shall be applied aligned with the scrambling code applied to the P-CCPCH. In this case, the scrambling code is thus not necessarily applied aligned with the frame boundary of the physical channel to be scrambled.

5.1.5 Channel combining

Figure 9 illustrates how different downlink channels are combined. Each complex-valued spread channel, corresponding to point S in Figure 8, may be separately weighted by a weight factor G_i. The complex-valued P-SCH and S-SCH, as described in [2], subclause 5.3.3.5, may be separately weighted by weight factors G_p and G_s. All downlink physical channels shall then be combined using complex addition.

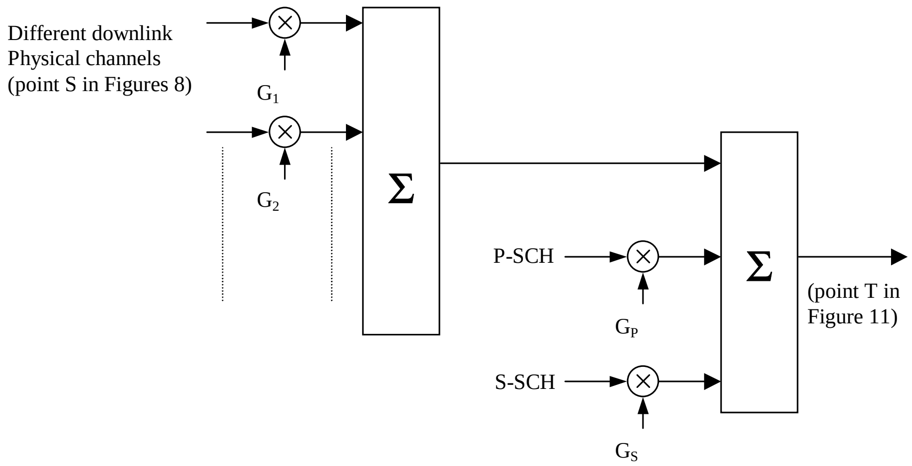

Figure 9: Combining of downlink physical channels

5.2 Code generation and allocation

5.2.1 Channelisation codes

The channelisation codes of figure 8 are the same codes as used in the uplink, namely Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between downlink channels of different rates and spreading factors. The OVSF codes are defined in figure 4 in subclause 4.3.1.

The channelisation code for the Primary CPICH is fixed to $C_{ch,256,0}$ and the channelisation code for the Primary CCPCH is fixed to $C_{ch,256,1}$.The channelisation codes for all other physical channels are assigned by UTRAN.

With the spreading factor 512 a specific restriction is applied. When the code word $C_{ch,512,n}$, with n=0,2,4….510, is used in soft handover, then the code word $C_{ch,512,n+1}$ is not allocated in the cells where timing adjustment is to be used. Respectively if $C_{ch,512,n}$, with n=1,3,5….511 is used, then the code word $C_{ch,512,n-1}$ is not allocated in the cells where timing adjustment is to be used. This restriction shall not apply in cases where timing adjustments in soft handover are not used with spreading factor 512.

When compressed mode is implemented by reducing the spreading factor by 2, the OVSF code used for compressed frames is:

- $C_{ch,SF/2,\lfloor n/2 \rfloor}$ if ordinary scrambling code is used.
- $C_{ch,SF/2,n \bmod SF/2}$ if alternative scrambling code is used (see subclause 5.2.2);

where $C_{ch,SF,n}$ is the channelisation code used for non-compressed frames.

For F-DPCH, the spreading factor is always 256.

For HS-PDSCH, the spreading factor is always 16.

For HS-SCCH, the spreading factor is always 128.

Channelisation-code-set information over HS-SCCH is mapped in following manner: the OVSF codes shall be allocated in such a way that they are positioned in sequence in the code tree. That is, for P multicodes at offset O the following codes are allocated:

$C_{ch,16,O} \ldots C_{ch,16,O+P-1}$

The number of multicodes and the corresponding offset for HS-PDSCHs mapped from a given HS-DSCH is signalled by HS-SCCH.

For E-HICH and for E-RGCH, the spreading factor shall always be 128. In each cell, the E-RGCH and E-HICH assigned to a UE shall be configured with the same channelisation code.

For E-AGCH, the spreading factor shall always be 256.

5.2.2 Scrambling code

A total of 2^{18}-1 = 262,143 scrambling codes, numbered 0…262,142 can be generated. However not all the scrambling codes are used. The scrambling codes are divided into 512 sets each of a primary scrambling code and 15 secondary scrambling codes.

The primary scrambling codes consist of scrambling codes n=16*i where i=0…511. The i:th set of secondary scrambling codes consists of scrambling codes 16*i+k, where k=1…15.

There is a one-to-one mapping between each primary scrambling code and 15 secondary scrambling codes in a set such that i:th primary scrambling code corresponds to i:th set of secondary scrambling codes.

Hence, according to the above, scrambling codes k = 0, 1, …, 8191 are used. Each of these codes are associated with a left alternative scrambling code and a right alternative scrambling code, that may be used for compressed frames. The left alternative scrambling code corresponding to scrambling code k is scrambling code number k + 8192, while the right alternative scrambling code corresponding to scrambling code k is scrambling code number k + 16384. The alternative scrambling codes can be used for compressed frames. In this case, the left alternative scrambling code is used if n<SF/2 and the right alternative scrambling code is used if n≥SF/2, where $c_{ch,SF,n}$ is the channelisation code used for non-compressed frames. The usage of alternative scrambling code for compressed frames is signalled by higher layers for each physical channel respectively.

In case F-DPCH is configured in the downlink, the same scrambling code and OVSF code shall be used in F-DPCH compressed frames and normal frames.

The set of primary scrambling codes is further divided into 64 scrambling code groups, each consisting of 8 primary scrambling codes. The j:th scrambling code group consists of primary scrambling codes 16*8*j+16*k, where j=0..63 and k=0..7.

Each cell is allocated one and only one primary scrambling code. The primary CCPCH, primary CPICH, PICH, MICH, AICH and S-CCPCH carrying PCH shall always be transmitted using the primary scrambling code. The other downlink physical channels may be transmitted with either the primary scrambling code or a secondary scrambling code from the set associated with the primary scrambling code of the cell.

In MBSFN operations, the S-CCPCH carries FACH only and shall always be transmitted using the primary scrambling code. The same primary CCPCH, primary CPICH, MICH and S-CCPCH may be transmitted from multiple cells using the same primary scrambling code when part of MBSFN operations.

The mixture of primary scrambling code and no more than one secondary scrambling code for one CCTrCH is allowable. In compressed mode during compressed frames, these can be changed to the associated left or right scrambling codes as described above, i.e. in these frames, the total number of different scrambling codes may exceed two.

In the case of CCTrCH of type of HS-DSCH then all the HS-PDSCH channelisation codes and HS-SCCH that a single UE may receive shall be under a single scrambling code (either the primary or a secondary scrambling code).

In each cell, the F-DPCH, E-RGCH, E-HICH and E-AGCH assigned to a UE shall be configured with same scrambling code as the assigned phase reference (primary or secondary CPICH).

In each cell the UE may be configured simultaneously with at most two scrambling codes.

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of 38400 chip segments of two binary *m*-sequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. The scrambling codes are repeated for every 10 ms radio frame. Let *x* and *y* be the two sequences respectively. The *x* sequence is constructed using the primitive (over GF(2)) polynomial $1+X^7+X^{18}$. The y sequence is constructed using the polynomial $1+X^5+X^7+ X^{10}+X^{18}$.

The sequence depending on the chosen scrambling code number *n* is denoted z_n, in the sequel. Furthermore, let $x(i)$, $y(i)$ and $z_n(i)$ denote the *i*:th symbol of the sequence *x, y,* and z_n, respectively.

The *m*-sequences *x*and *y* are constructed as:

Initial conditions:

- x is constructed with x (0)=1, x(1)= x(2)=...= x (16)= x (17)=0.
- y(0)=y(1)= … =y(16)= y(17)=1.

Recursive definition of subsequent symbols:

- x(i+18) =x(i+7) + x(i) modulo 2, i=0,…,2^{18}-20.
- y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i) modulo 2, i=0,…, 2^{18}-20.

The n:th Gold code sequence z_n, $n=0,1,2,\ldots,2^{18}-2$, is then defined as:

- $z_n(i) = x((i+n) \text{ modulo } (2^{18} - 1)) + y(i)$ modulo 2, i=0,…, 2^{18}-2.

These binary sequences are converted to real valued sequences Z_n by the following transformation:

$$Z_n(i) = \begin{cases} +1 & if \;\; z_n(i) = 0 \\ -1 & if \;\; z_n(i) = 1 \end{cases} \quad for \quad i = 0,1,\ldots,2^{18}-2.$$

Finally, the n:th complex scrambling code sequence $S_{dl,n}$ is defined as:

- $S_{dl,n}(i) = Z_n(i) + j\, Z_n((i+131072) \text{ modulo } (2^{18}-1))$, i=0,1,…,38399.

Note that the pattern from phase 0 up to the phase of 38399 is repeated.

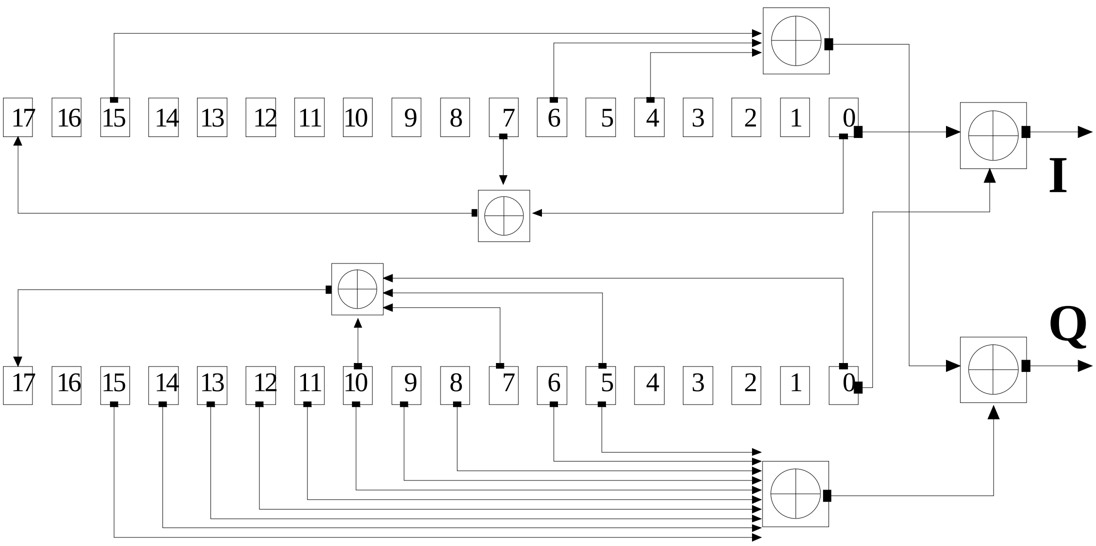

Figure 10: Configuration of downlink scrambling code generator

5.2.3 Synchronisation codes

5.2.3.1 Code generation

The primary synchronisation code (PSC), C_{psc} is constructed as a so-called generalised hierarchical Golay sequence. The PSC is furthermore chosen to have good aperiodic auto correlation properties.

Define:

- $a = \langle x_1, x_2, x_3, \ldots, x_{16} \rangle = \langle 1, 1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1 \rangle$

The PSC is generated by repeating the sequence *a* modulated by a Golay complementary sequence, and creating a complex-valued sequence with identical real and imaginary components. The PSC C_{psc} is defined as:

- $C_{psc} = (1 + j) \times$ <a, a, a, -a, -a, a, -a, -a, a, a, a, -a, a, -a, a, a>;

where the leftmost chip in the sequence corresponds to the chip transmitted first in time.

The 16 secondary synchronization codes (SSCs), $\{C_{ssc,1},\dots,C_{ssc,16}\}$, are complex-valued with identical real and imaginary components, and are constructed from position wise multiplicationof a Hadamard sequence and a sequence *z*, defined as:

- z = <b, b, b, -b, b, b, -b, -b, b, -b, b, -b, -b, -b, -b, -b>, where
- $b = \langle x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, -x_9, -x_{10}, -x_{11}, -x_{12}, -x_{13}, -x_{14}, -x_{15}, -x_{16} \rangle$ and $x_1, x_2, \dots, x_{15}, x_{16}$ are same as in the definition of the sequence *a* above.

The Hadamard sequences are obtained as the rows in a matrix H_8 constructed recursively by:

$$H_0 = (1)$$
$$H_k = \begin{pmatrix} H_{k-1} & H_{k-1} \\ H_{k-1} & -H_{k-1} \end{pmatrix}, \quad k \geq 1$$

The rows are numbered from the top starting with row *0* (the all ones sequence).

Denote the *n*:th Hadamard sequence as a row of H_8 numbered from the top, n = 0, 1, 2, …, 255, in the sequel.

Furthermore, let $h_n(i)$ and $z(i)$ denote the *i*:th symbol of the sequence h_n and *z*, respectively where *i* = 0, 1, 2, …, 255 and *i* = 0 corresponds to the leftmost symbol.

The *k*:th SSC, $C_{ssc,k}$, *k* = 1, 2, 3, …, 16 is then defined as:

- $C_{ssc,k} = (1 + j) \times \langle h_m(0) \times z(0), h_m(1) \times z(1), h_m(2) \times z(2), \dots, h_m(255) \times z(255) \rangle$;

  where $m = 16\times(k - 1)$ and the leftmost chip in the sequence corresponds to the chip transmitted first in time.

5.2.3.2 Code allocation of SSC

The 64 secondary SCH sequences are constructed such that their cyclic-shifts are unique, i.e., a non-zero cyclic shift less than 15 of any of the 64 sequences is not equivalent to some cyclic shift of any other of the 64 sequences. Also, a non-zero cyclic shift less than 15 of any of the sequences is not equivalent to itself with any other cyclic shift less than 15. Table 4 describes the sequences of SSCs used to encode the 64 different scrambling code groups. The entries in table 4 denote what SSC to use in the different slots for the different scrambling code groups, e.g. the entry "7" means that SSC $C_{ssc,7}$ shall be used for the corresponding scrambling code group and slot.

Table 4: Allocation of SSCs for secondary SCH

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 0	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 1	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
Group 2	1	2	1	15	5	5	12	16	6	11	2	16	11	15	12
Group 3	1	2	3	1	8	6	5	2	5	8	4	4	6	3	7
Group 4	1	2	16	6	6	11	15	5	12	1	15	12	16	11	2
Group 5	1	3	4	7	4	1	5	5	3	6	2	8	7	6	8
Group 6	1	4	11	3	4	10	9	2	11	2	10	12	12	9	3
Group 7	1	5	6	6	14	9	10	2	13	9	2	5	14	1	13
Group 8	1	6	10	10	4	11	7	13	16	11	13	6	4	1	16
Group 9	1	6	13	2	14	2	6	5	5	13	10	9	1	14	10
Group 10	1	7	8	5	7	2	4	3	8	3	2	6	6	4	5
Group 11	1	7	10	9	16	7	9	15	1	8	16	8	15	2	2
Group 12	1	8	12	9	9	4	13	16	5	1	13	5	12	4	8
Group 13	1	8	14	10	14	1	15	15	8	5	11	4	10	5	4
Group 14	1	9	2	15	15	16	10	7	8	1	10	8	2	16	9
Group 15	1	9	15	6	16	2	13	14	10	11	7	4	5	12	3
Group 16	1	10	9	11	15	7	6	4	16	5	2	12	13	3	14
Group 17	1	11	14	4	13	2	9	10	12	16	8	5	3	15	6
Group 18	1	12	12	13	14	7	2	8	14	2	1	13	11	8	11
Group 19	1	12	15	5	4	14	3	16	7	8	6	2	10	11	13
Group 20	1	15	4	3	7	6	10	13	12	5	14	16	8	2	11
Group 21	1	16	3	12	11	9	13	5	8	2	14	7	4	10	15
Group 22	2	2	5	10	16	11	3	10	11	8	5	13	3	13	8
Group 23	2	2	12	3	15	5	8	3	5	14	12	9	8	9	14
Group 24	2	3	6	16	12	16	3	13	13	6	7	9	2	12	7
Group 25	2	3	8	2	9	15	14	3	14	9	5	5	15	8	12
Group 26	2	4	7	9	5	4	9	11	2	14	5	14	11	16	16
Group 27	2	4	13	12	12	7	15	10	5	2	15	5	13	7	4
Group 28	2	5	9	9	3	12	8	14	15	12	14	5	3	2	15
Group 29	2	5	11	7	2	11	9	4	16	7	16	9	14	14	4
Group 30	2	6	2	13	3	3	12	9	7	16	6	9	16	13	12
Group 31	2	6	9	7	7	16	13	3	12	2	13	12	9	16	6
Group 32	2	7	12	15	2	12	4	10	13	15	13	4	5	5	10
Group 33	2	7	14	16	5	9	2	9	16	11	11	5	7	4	14
Group 34	2	8	5	12	5	2	14	14	8	15	3	9	12	15	9
Group 35	2	9	13	4	2	13	8	11	6	4	6	8	15	15	11
Group 36	2	10	3	2	13	16	8	10	8	13	11	11	16	3	5
Group 37	2	11	15	3	11	6	14	10	15	10	6	7	7	14	3
Group 38	2	16	4	5	16	14	7	11	4	11	14	9	9	7	5
Group 39	3	3	4	6	11	12	13	6	12	14	4	5	13	5	14
Group 40	3	3	6	5	16	9	15	5	9	10	6	4	15	4	10
Group 41	3	4	5	14	4	6	12	13	5	13	6	11	11	12	14
Group 42	3	4	9	16	10	4	16	15	3	5	10	5	15	6	6
Group 43	3	4	16	10	5	10	4	9	9	16	15	6	3	5	15
Group 44	3	5	12	11	14	5	11	13	3	6	14	6	13	4	4
Group 45	3	6	4	10	6	5	9	15	4	15	5	16	16	9	10
Group 46	3	7	8	8	16	11	12	4	15	11	4	7	16	3	15
Group 47	3	7	16	11	4	15	3	15	11	12	12	4	7	8	16
Group 48	3	8	7	15	4	8	15	12	3	16	4	16	12	11	11
Group 49	3	8	15	4	16	4	8	7	7	15	12	11	3	16	12

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 50	3	10	10	15	16	5	4	6	16	4	3	15	9	6	9
Group 51	3	13	11	5	4	12	4	11	6	6	5	3	14	13	12
Group 52	3	14	7	9	14	10	13	8	7	8	10	4	4	13	9
Group 53	5	5	8	14	16	13	6	14	13	7	8	15	6	15	7
Group 54	5	6	11	7	10	8	5	8	7	12	12	10	6	9	11
Group 55	5	6	13	8	13	5	7	7	6	16	14	15	8	16	15
Group 56	5	7	9	10	7	11	6	12	9	12	11	8	8	6	10
Group 57	5	9	6	8	10	9	8	12	5	11	10	11	12	7	7
Group 58	5	10	10	12	8	11	9	7	8	9	5	12	6	7	6
Group 59	5	10	12	6	5	12	8	9	7	6	7	8	11	11	9
Group 60	5	13	15	15	14	8	6	7	16	8	7	13	14	5	16
Group 61	9	10	13	10	11	15	15	9	16	12	14	13	16	14	11
Group 62	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 63	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10

5.3 Modulation

5.3.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps.

5.3.2 Modulation

Modulation of the complex-valued chip sequence generated by the spreading process is shown in Figure 11 below.

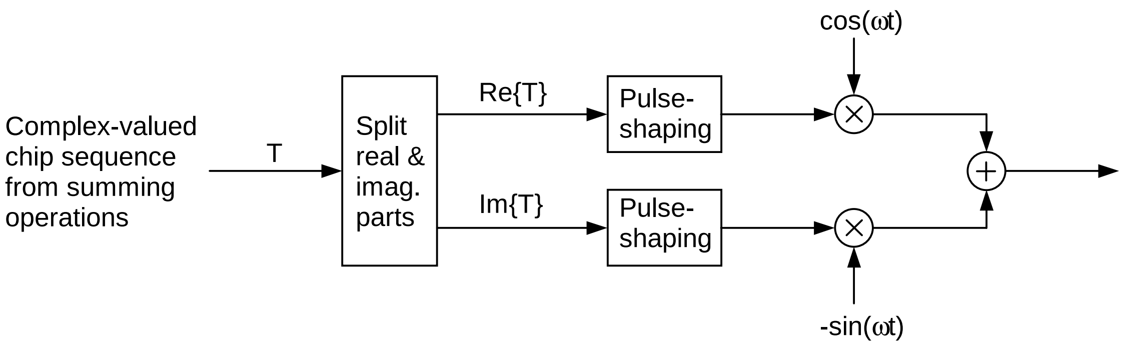

Figure 11: Downlink modulation

The pulse-shaping characteristics are described in [4].

Annex A (informative): Generalised Hierarchical Golay Sequences

A.1 Alternative generation

The generalised hierarchical Golay sequences for the PSC described in 5.2.3.1 may be also viewed as generated (in real valued representation) by the following methods:

Method 1.

The sequence y is constructed from two constituent sequences x_1 and x_2 of length n_1 and n_2 respectively using the following formula:

- $y(i) = x_2(i \bmod n_2) * x_1(i \operatorname{div} n_2)$, $i = 0 \ldots (n_1 * n_2) - 1$.

The constituent sequences x_1 and x_2 are chosen to be the following length 16 (i.e. $n_1 = n_2 = 16$) sequences:

- x_1 is defined to be the length 16 ($N^{(1)}=4$) Golay complementary sequence obtained by the delay matrix $D^{(1)} = [8, 4, 1, 2]$ and weight matrix $W^{(1)} = [1, -1, 1, 1]$.
- x_2 is a generalised hierarchical sequence using the following formula, selecting s=2 and using the two Golay complementary sequences x_3 and x_4 as constituent sequences. The length of the sequence x_3 and x_4 is called n_3 respectively n_4.
- $x_2(i) = x_4(i \bmod s + s*(i \operatorname{div} sn_3)) * x_3((i \operatorname{div} s) \bmod n_3)$, $i = 0 \ldots (n_3 * n_4) - 1$.
- x_3 and x_4 are defined to be identical and the length 4 ($N^{(3)} = N^{(4)} = 2$) Golay complementary sequence obtained by the delay matrix $D^{(3)} = D^{(4)} = [1, 2]$ and weight matrix $W^{(3)} = W^{(4)} = [1, 1]$.

The Golay complementary sequences x_1,x_3 and x_4 are defined using the following recursive relation:

$a_0(k) = \delta(k)$ and $b_0(k) = \delta(k)$;

$a_n(k) = a_{n-1}(k) + W^{(j)}_n \cdot b_{n-1}(k - D^{(j)}_n)$;

$b_n(k) = a_{n-1}(k) - W^{(j)}_n \cdot b_{n-1}(k - D^{(j)}_n)$;

$k = 0, 1, 2, \ldots, 2^{**}N^{(j)} - 1$;

$n = 1, 2, \ldots, N^{(j)}$.

The wanted Golay complementary sequence x_j is defined by a_n assuming $n=N^{(j)}$. The Kronecker delta function is described by δ, k,j and n are integers.

Method 2

The sequence y can be viewed as a pruned Golay complementary sequence and generated using the following parameters which apply to the generator equations for a and b above:

(a) Let $j = 0$, $N^{(0)} = 8$.

(b) $[D_1^0, D_2^0, D_3^0, D_4^0, D_5^0, D_6^0, D_7^0, D_8^0] = [128, 64, 16, 32, 8, 1, 4, 2]$.

(c) $[W_1^0, W_2^0, W_3^0, W_4^0, W_5^0, W_6^0, W_7^0, W_8^0] = [1, -1, 1, 1, 1, 1, 1, 1]$.

(d) For n = 4, 6, set $b_4(k) = a_4(k)$, $b_6(k) = a_6(k)$.

Annex B (informative): Change history

Change history							
Date	**TSG #**	**TSG Doc.**	**CR**	**Rev**	**Subject/Comment**	**Old**	**New**
14/01/00	RAN_05	RP-99589	-		Approved at TSG RAN #5 and placed under Change Control	-	3.0.0
14/01/00	RAN_06	RP-99682	005	1	Harmonization of notations for downlink scrambling codes	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	006	-	Update of downlink spreading description	3.0.0	3.1.0
14/01/00	RAN_06	RP-99682	007	1	Update of TS 25.213 uplink parts	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	008	-	Updated modulation description	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	009	-	Restriction for spreading factor 512 allocation in the UTRA FDD Downlink	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	011	1	CPCH codes in power control preamble	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	012	2	Support of short codes for CPCH	3.0.0	3.1.0
14/01/00	RAN_06	RP-99682	014	1	Editorial Change	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	016	-	Channelization Code Allocation for USTS	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	017	1	Correction (Editorial Change)	3.0.0	3.1.0
14/01/00	RAN_06	RP-99683	019	-	Correction to code allocation for compressed mode	3.0.0	3.1.0
14/01/00	-	-	-		Change history was added by the editor	3.1.0	3.1.1
31/03/00	RAN_07	RP-000063	020	1	Consistent numbering of scrambling code groups	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	021	-	Downlink signal flow corrections	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	022	-	Uplink signal flow corrections	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	023	1	Number of RACH scrambling codes	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	024	1	Editorial changes to 25.213	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	025	3	Number of PCPCH scrambling codes per cell	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	027	-	A typo correction for 5.2.2 and clarification for 5.2.3.1 of TS 25.213V3.1.1	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	028	2	Channelization code allocation method for PCPCH message part	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	029	-	Clarifications to DSCH scrambling and modulation in 25.213	3.1.1	3.2.0
31/03/00	RAN_07	RP-000063	032	-	Clean up of USTS related specifications	3.1.1	3.2.0
26/06/00	RAN_08	RP-000267	033	-	Clarifications to power control preamble sections	3.2.0	3.3.0
26/06/00	RAN_08	RP-000267	034	2	Numbering of the PCPCH access preamble and collision detection preamble scrambling codes	3.2.0	3.3.0
26/06/00	RAN_08	RP-000267	035	-	DPDCH/DPCCH gain factors	3.2.0	3.3.0
16/12/00	RAN_10	RP-000539	037	1	Proposed removal of the option of secondary scrambling code for some downlink common channels	3.3.0	3.4.0
16/03/01	RAN_11	-	-	-	Approved as Release 4 specification (v4.0.0) at TSG RAN #11	3.4.0	4.0.0
16/03/01	RAN_11	RP-010059	038	-	Clarification of channelization codes when SF=512	3.4.0	4.0.0
16/03/01	RAN_11	RP-010059	039	1	Clarification of the scrambling code of a power control preamble	3.4.0	4.0.0
15/06/01	RAN_12	RP-010333	041	1	Clarification of DL channelization code alignment	4.0.0	4.1.0
15/06/01	RAN_12	RP-010333	043	1	Clarification of PDSCH root channelisation code definition	4.0.0	4.1.0
14/12/01	RAN_14	RP-010738	047	-	Correction of section number reference	4.1.0	4.2.0
08/03/02	RAN_15	RP-020058	049	-	The inclusion of HSDPA into 25.213	4.2.0	5.0.0
07/06/02	RAN_16	RP-020309	053	1	Downlink bit mapping	5.0.0	5.1.0
07/06/02	RAN_16	RP-020316	050	-	Consistency of Signal Point Constellation for QPSK and 16QAM	5.0.0	5.1.0
07/06/02	RAN_16	RP-020316	054	-	Clarification of uplink DTX handling and modulation	5.0.0	5.1.0
07/06/02	RAN_16	RP-020316	055	-	Removal of code mapping description over HS-SCCH	5.0.0	5.1.0
07/06/02	RAN_16	RP-020316	056	3	I/Q mapping of HS-DPCCH	5.0.0	5.1.0
07/06/02	RAN_16	RP-020316	057	-	Definition of the amplitude gain factor for HS-DPCCH	5.0.0	5.1.0
16/09/02	RAN_17	RP-020583	058	1	Numbering corrections	5.1.0	5.2.0
16/09/02	RAN_17	RP-020583	059		Correction on the maximum DPDCH in Figure1	5.1.0	5.2.0
16/09/02	RAN_17	RP-020592	060		Power offset values for HS-DPCCH	5.1.0	5.2.0
26/03/03	RAN_19	RP-030135	061	1	Removal of the tiny text in Figure 1 and minor corrections to 4.2.1	5.2.0	5.3.0
21/09/03	RAN_21	RP-030457	062	-	Clarification of 16QAM modulation description	5.3.0	5.4.0
06/01/04	RAN_22	RP-030648	064	1	Correction of figure in combining of downlink physical channels	5.4.0	5.5.0
06/01/04	RAN_22	RP-030648	065	1	Correction of reference to calculation of HS-DPCCH gain factor	5.4.0	5.5.0
06/01/04	RAN_22	RP-030727	067	2	Restriction of DL secondary scrambling codes per CCTrCH	5.4.0	5.5.0
13/01/04	RAN_22	-	-	-	Created for M.1457 update	5.5.0	6.0.0
13/12/04	RAN_26	RP-040539	071	3	Introduction of E-DCH	6.0.0	6.1.0
13/12/04	RAN_26	RP-040450	069	-	Introduction of MICH	6.0.0	6.1.0
14/03/05	RAN_27	RP-050088	070	1	Introduction of F-DPCH	6.1.0	6.2.0
14/03/05	RAN_27	RP-050046	072	-	Correction on E-DPCCH power offset	6.1.0	6.2.0

Change history							
Date	**TSG #**	**TSG Doc.**	**CR**	**Rev**	**Subject/Comment**	**Old**	**New**
14/03/05	RAN_27	RP-050047	073	1	Defining E-DPDCH power offset	6.1.0	6.2.0
16/06/05	RAN_28	RP-050252	074	2	Power offset values for E-DPDCH/E-DPCCH	6.2.0	6.3.0
16/06/05	RAN_28	RP-050252	075	3	Support of different HARQ profiles	6.2.0	6.3.0
16/06/05	RAN_28	RP-050250	077	2	Feature Clean Up: Removal of 'CPCH'	6.2.0	6.3.0
16/06/05	RAN_28	RP-050248	079	-	Feature Clean Up: Removal of DSCH (FDD mode)	6.2.0	6.3.0
16/06/05	RAN_28	RP-050256	080	-	Correction to short scrambling code polynomial	6.2.0	6.3.0
26/09/05	RAN_29	RP-050450	0081	-	Clarification on derivation of β_c and β_d	6.3.0	6.4.0
26/09/05	RAN_29	RP-050450	0082	1	DL Scrambling Code and Phase Reference Combinations	6.3.0	6.4.0
26/09/05	RAN_29	RP-050450	0083	1	Clarification on power offset quantization	6.3.0	6.4.0
20/03/06	RAN_31	RP-060076	0084	1	Correction to number of configured DPDCHs when E-DPDCH is configured	6.4.0	6.5.0
20/03/06	RAN_31	-	-	-	Creation of Release 7 specification (v7.0.0) at RAN#31	6.5.0	7.0.0
07/03/07	RAN_35	RP-070116	0085	2	Introduction of 64QAM for HSDPA	7.0.0	7.1.0
30/05/07	RAN_36	RP-070388	0086	4	Introduction of 16-QAM for HSUPA	7.1.0	7.2.0
30/05/07	RAN_36	RP-070384	0087	1	Support for DL only SFN operation for MBMS FDD	7.1.0	7.2.0
30/05/07	RAN_36	RP-070387	0089	-	CQI and ACK/NACK power setting for MIMO	7.1.0	7.2.0
11/09/07	RAN_37	RP-070644	0090	-	Editorial changes in 25.213 for 16QAM specification	7.2.0	7.3.0
27/11/07	RAN_38	RP-070944	0091	1	Editorial changes in 25.213 for 16QAM specification	7.3.0	7.4.0
04/03/08	RAN_39	-	-	-	Release 8 version further to RAN_39 decision	7.4.0	8.0.0
28/05/08	RAN_40	RP-080439	0093	1	Range of E-DCH amplitude ratios	8.0.0	8.1.0

History

Document history		
V8.1.0	October 2008	Publication