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GROUP REPORT

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Foreword

This Group Report (GR) has been produced by ETSI Industry Specification Group (ISG) TeraHertz (THz).

Modal verbs terminology

In the present document "**should**", "**should not**", "**may**", "**need not**", "**will**", "**will not**", "**can**" and "**cannot**" are to be interpreted as described in clause 3.2 of the [ETSI Drafting Rules](#) (Verbal forms for the expression of provisions).

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Executive summary

The present document focuses on modeling the of (sub-)THz transceivers and their building blocks. It provides a summary of transceiver architectures for communication, sensing and joint communication and sensing. The critical building blocks are discussed in depth with a focus on models and their critical parameters. An effort is made to provide specific numbers that can be used by designers for system simulations. Lastly, practical implementation aspects including packaging, semiconductor and photonic technologies are discussed.

Introduction

The (sub-)THz band (0,1 THz to 10 THz) provided a large amount of untapped bandwidth that can be used for a variety of wireless applications, especially communication and sensing. The ample bandwidth makes it a strong candidate for future technologies such as 6G, wireless backhaul and Integrated Communication And Sensing (ISAC).

The THz band also presents unique challenges. Silicon technology cannot facilitate high performing transceivers beyond ~180 GHz. Even high-performance compound semiconductor devices reach their limit at approximately 300 GHz. Photonic technologies are likely necessary beyond this frequency. Even in the 100 GHz to 200 GHz frequency range, RF impairments such as phase noise and limited transmitter output power will limit the maximum possible modulation order to lower values than currently used by lower-frequency systems.

The present document provides a summary of the critical building block of (sub-)THz transceivers. Models and modeling parameters are proposed for each block. Special focus is placed on summarizing and proposing parameter values that can be useful for system designers.

1 Scope

The present document focused on modeling the of (sub-)THz transceivers and their building blocks.

2 References

2.1 Normative references

Normative references are not applicable in the present document.

2.2 Informative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

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The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

- [i.1] I. Ahmed et al.: "[A Survey on Hybrid Beamforming Techniques in 5G: Architecture and System Model Perspectives](#)", in IEEETM Communications Surveys & Tutorials, vol. 20, no. 4, pp. 3060-3097, 4th quarter, 2018.
- [i.2] M. Rihan, T. Abed Soliman, C. Xu, L. Huang and M. I. Dessouky: "[Taxonomy and Performance Evaluation of Hybrid Beamforming for 5G and Beyond Systems](#)", in IEEETM Access, vol. 8, pp. 74605-74626, 2020.
- [i.3] Y. Huang et al.: "[From Terahertz Imaging to Terahertz Wireless Communications](#)", in Engineering, 2022.
- [i.4] N. Maletic, J. Gutiérrez and E. Grass: "[On the Impact of Residual Transceiver Impairments in mmWave RF Beamforming Systems](#)", in IEEETM Communications Letters, vol. 24, no. 11, pp. 2459-2463, 2020.
- [i.5] C. Han et al.: "[Hybrid Beamforming for Terahertz Wireless Communications: Challenges, Architectures, and Open Problems](#)", in IEEETM Wireless Communications, vol. 28, no. 4, pp. 198-204, 2021.
- [i.6] B. Ning et al.: "[Beamforming Technologies for Ultra-Massive MIMO in Terahertz Communications](#)", in IEEETM Open Journal of the Communications Society, vol. 4, pp. 614-658, 2023.
- [i.7] E. Björnson, J. Hoydis, M. Kountouris and M. Debbah: "Massive MIMO Systems with Non-Ideal Hardware: Energy Efficiency, Estimation, and Capacity Limits", in IEEETM Transactions on Information Theory, vol. 60, no. 11, pp. 7112-7139, 2014.
- [i.8] S. Javed, O. Amin, S. S. Ikki and M.-S. Alouini: "Multiple Antenna Systems with Hardware Impairments: New Performance Limits", in IEEETM Transactions on Vehicular Technology, vol. 68, no. 2, pp. 1593-1606, 2019..
- [i.9] Z. Sha and Z. Wang: "Channel Estimation and Equalization for Terahertz Receiver with RF Impairments", in IEEETM Journal on Selected Areas in Communications, vol. 39, no. 6, pp. 1621-1635, 2021.

- [i.10] E. Vlachos et al.: "[Radio-frequency Chain Selection for Energy and Spectral Efficiency Maximization in Hybrid Beamforming under Hardware Imperfections](#)", in Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences, vol. 476, no. 2244, 2020.
- [i.11] V. Syrjala, M. Valkama, L. Anttila, T. Riihonen and D. Korpi: "[Analysis of Oscillator Phase-Noise Effects on Self-Interference Cancellation in Full-Duplex OFDM Radio Transceivers](#)", in IEEETM Transactions on Wireless Communications, vol. 13, no. 6, pp. 2977-2990, 2014.
- [i.12] N. Ginzberg, D. Regev and E. Cohen: "[Transceiver Architectures for Full Duplex Systems with Unmatched Receiver](#)", in IEEETM Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), pp. 1-4, 2019.
- [i.13] J. W. Kwak et al.: "[Analog Self-Interference Cancellation with Practical RF Components for Full-Duplex Radios](#)", in IEEETM Transactions on Wireless Communications, 2023.
- [i.14] B. Razavi: "RF Microelectronics", Prentice Hall, Second Edition, 2011.
- [i.15] K. Kundert: "Accurate and Rapid Measurement of IP2 and IP3", The Designer Guide Community, 2002.
- [i.16] E. Aguilar, V. Issakov and R. Weigel: "Highly-Integrated <0.14mm2D -Band Receiver Front-Ends for Radar and Imaging Applications in a 130 nm SiGe BiCMOS Technology", in IEEETM 19th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2019.
- [i.17] A. Bilato, V. Issakov, A. Mazzanti and A. Bevilacqua: "A Multichannel D-Band Radar Receiver With Optimized LO Distribution", IEEETM Solid-State Circuits Letters, 2021.
- [i.18] W. Deng, Z. Chen, H. Jia, P. Guan, T. Ma, A. Yan, S. Sun, X. Huang, G. Chen, R. Ma, S. Dong, L. Duan, Z. Wang and B. Chi: "A D-Band Joint Radar-Communication CMOS Transceiver", IEEETM Journal of Solid-State Circuits, 2022.
- [i.19] C. Wang and G. Rebeiz: "A 2-Channel 136-156 GHz Dual Down-Conversion I/Q Receiver with 30 dB Gain and 9.5 dB NF Using CMOS 22nm FDSOI", IEEETM Radio Frequency Integrated Circuits Symposium (RFIC), 2021.
- [i.20] S. Li and G. Rebeiz: "A 134-149 GHz IF beamforming phased-array receiver channel with 6.4-7.5 dB NF using CMOS 45nm RFSOI", in IEEETM Radio Frequency Integrated Circuits Symposium (RFIC), 2020.
- [i.21] Ahmed S. H. Ahmed, Munkyo Seo, Ali A. Farid, Miguel Urteaga, James F. Buckwalter, Mark J. W. Rodwell: "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology", 2020 IEEE/MTT-S International Microwave Symposium (IMS).
- [i.22] M. Hossain, T. Shivan, R. Doerner, S. Seifert, H. Yacoub, T.K. Johansen, W. Heinrich, V. Krozer: "A D-Band Power Amplifier with 12dBm P1dB, 10% Power Added Efficiency in InP-DHBT Technology", 2022 Proceedings of the 16th European Microwave Integrated Circuits Conference.
- [i.23] Senne Gielen, Yang Zhang, Mark Ingels, Patrick Reynaert: "A D-band 20.4 dBm OP1dB Transformer-Based Power Amplifier With 23.6% PAE In A 250-nm InP HBT Technology", 2023 IEEETM Radio Frequency Integrated Circuits Symposium.
- [i.24] Z. Griffith, M. Urteaga and P. Rowell: "A Compact 140-GHz, 150-mW High-Gain Power Amplifier MMIC in 250-nm InP HBT", in IEEETM Microwave and Wireless Components Letters, vol. 29, no. 4, pp. 282-284, April 2019.
- [i.25] A. Alizadeh, U. Soyulu, N. Sharma, G. Xu and M. J. W. Rodwell: "D-Band Power Amplifier with 27 dBm Peak Output Power and 14.9% PAE in 250-nm InP HBT Technology", 2023 IEEETM BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA, 2023, pp. 94-97.
- [i.26] C.-G. Choi, H. -H. Jeong, S. -H. Cho, S. Kim and H. -J. Song: "A 275-GHz InP HBT H-Band Amplifier With Transmission Line-Based Capacitively Coupled Resonator Matching Technique", in IEEETM Transactions on Terahertz Science and Technology, vol. 13, no. 6, pp. 659-670, November 2023.

- [i.27] Ali A, Yun J, Giannini F, Ng HJ, Kissinger D, Colantonio P.: "168-195 GHz Power Amplifier With Output Power Larger Than 18 dBm in BiCMOS Technology", *IEEE™ Access*, 2020; 8:79299-309.
- [i.28] N. Sarmah, K. Aufinger, R. Lachner and U. R. Pfeiffer: "A 200-225 GHz SiGe Power Amplifier with peak Psat of 9.6 dBm using wideband power combination", *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Lausanne, Switzerland, 2016, pp. 193-196, doi: 10.1109/ESSCIRC.2016.7598275.
- [i.29] J. Yu et al.: "A 211-to-263-GHz Dual-LC-Tank-Based Broadband Power Amplifier With 14.7-dBm PSAT and 16.4-dB Peak Gain in 130-nm SiGe BiCMOS", in *IEEE™ Journal of Solid-State Circuits*, vol. 58, no. 2, pp. 332-344, February 2023, doi: 10.1109/JSSC.2022.3192043.
- [i.30] L. Zhao, Y. Li, W. Yu and X. Lv: "A 110-160GHz Wideband Power Amplifier in 0.13 μ m SiGe BiCMOS with 14.12dBm Psat and 9.26% PAE", *2023 IEEE™ MTT-S International Wireless Symposium (IWS)*, Qingdao, China, 2023, pp. 1-3.
- [i.31] P. Stärke, C. Carta and F. Ellinger: "High-Linearity 19-dB Power Amplifier for 140-220 GHz, Saturated at 15 dBm, in 130-nm SiGe", in *IEEE™ Microwave and Wireless Components Letters*, vol. 30, no. 4, pp. 403-406, April 2020.
- [i.32] Zhang J, Wu T, Nie L, Ma S, Chen Y, Ren J.: "A 120-150 GHz Power Amplifier in 28-nm CMOS Achieving 21.9-dB Gain and 11.8-dBm P_{sat} for Sub-THz Imaging System", *IEEE™ Access*. 2021; 9: 74752-62.
- [i.33] B. Philippe and P. Reynaert: "24.7 A 15dBm 12.8%-PAE Compact D-Band Power Amplifier with Two-Way Power Combining in 16nm FinFET CMOS", *2020 IEEE™ International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2020, pp. 374-376.
- [i.34] D. Simic and P. Reynaert: "A 14.8 dBm 20.3 dB Power Amplifier for D-band Applications in 40 nm CMOS", *2018 IEEE™ Radio Frequency Integrated Circuits Symposium (RFIC)*, Philadelphia, PA, USA, 2018, pp. 232-235.
- [i.35] Zuo-Min Tsai et al.: "A 1.2V broadband D-band power amplifier with 13.2-dBm output power in standard RF 65-nm CMOS", *2012 IEEE/MTT-S International Microwave Symposium Digest*, Montreal, QC, Canada, 2012, pp. 1-3.
- [i.36] S. Hassanzadehyamchi, A. Alizadeh, A. M. Niknejad and O. Momeni: "A 200-GHz Power Amplifier With 18.7-dBm Psat in 45-nm CMOS SOI: A Model-Based Large-Signal Approach on Cascaded Series-Connected Power Amplification", in *IEEE™ Journal of Solid-State Circuits*.
- [i.37] H. Bameri and O. Momeni: "A 200-GHz Power Amplifier With a Wideband Balanced Slot Power Combiner and 9.4-dBm P_{sat} in 65-nm CMOS: Embedded Power Amplification", in *IEEE™ Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3318-3330, November 2021.
- [i.38] Rapp C.: "Effects of HPA-nonlinearity on 4-DPSK/OFDM-signal for a digital sound broadcasting system", 1991, p. 179-184.
- [i.39] 3GPP TR 38.807 (V1.0.0): "Study on NR beyond 52.6 GHz".
- [i.40] Nokia: "Realistic power amplifier model for the New Radio evaluation", 3rd Generation Partnership Project (3GPP); 2016. R4-163314. TSG-RAN WG4 Meeting.
- [i.41] Kyunghwan Kim, Jiwon Kang, Kangseop Lee, Seung-Uk Choi, Jiseul Kim and Ho-Jin Song: "A 115.7-139.7 GHz Amplifier with 19.7 dB Peak Gain and 7.9 dB NF in 40nm CMOS", *2023 International Microwave Symposium*.
- [i.42] Behzad Razavi: "Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level", Cambridge University Press, 2020.
- [i.43] Dean Banerjee: "[PLL Performance, Simulation, and Design](#)", 2017.
- [i.44] Jaehong Jung, Seungjin Kim, Wonkang Kim et al.: "A 52MHz -158.2dBc/Hz PN @ 100kHz Digitally Controlled Crystal Oscillator Utilizing a Capacitive-Load-Dependent Dynamic Feedback Resistor in 28nm CMOS", in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*.

- [i.45] [Abracon AK2 Fixed-Frequency Miniature Clock Oscillator Datasheet](#).
- [i.46] [Crystek CCHD-950 Datasheet](#).
- [i.47] [Greenray N623 Datasheet](#).
- [i.48] K. Zheg et al.: "Considerations on Phase Noise Model for 802.11ay", 2016 IEEE™ 802.11.
- [i.49] 3GPP TR 38.808: "Study on supporting NR from 52.6 GHz to 71 GHz".
- [i.50] Ali A. M. A.: "High speed data converters". London, U.K.: IET Press, 2016.
- [i.51] Walden R. H.: "Analog-to-digital converter survey and analysis", IEEE™ J. Sel. Areas Comm., vol. 17, no. 4, pp. 539-550, 1999.
- [i.52] Schreier R. and Temes, G. C.: "Understanding Delta-Sigma Data Converters". New York: Wiley, 2005.
- [i.53] Ali A. M. A. et al.: "A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration", IEEE™ J. Solid-State Circuits, vol. 45, no. 12, pp. 2602-2612, December 2010.
- [i.54] Murmann B.: "The race for the extra decibel: A brief review of current ADC performance trajectories", IEEE™ Solid-State Circuits Magazine, 2015.
- [i.55] Murmann B.: "[ADC performance survey 1997-2022](#)", accessed online on March 15, 2023.
- [i.56] Kull L. et al.: "A 24-to-72GS/s 8b Time-Interleaved SAR ADC with 2.0-to-3.3pJ/conversion and >30dB SNDR at Nyquist in 14nm CMOS FinFET", IEEE™ ISSCC, 2018.
- [i.57] Pisati M. et al.: "A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-Based Transceiver in 7nm FinFET", IEEE™ ISSCC, 2019.
- [i.58] Chen V. H.-C. and Pileggi, L.: "A 69.5mW 20GS/s 6b Time-Interleaved ADC with Embedded Time-to-Digital Calibration in 32nm CMOS SOI", IEEE™ ISSCC, 2014.
- [i.59] Cai S. et al.: "A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS", IEEE™ Symp. VLSI Circuits, 2015.
- [i.60] Xu B. et al.: "A 23mW 24GS/s 6b Time-Interleaved Hybrid Two-Step ADC in 28nm CMOS", IEEE™ Symp. VLSI Circuits, 2016.
- [i.61] Kumar S. S. et al.: "A 750mW 24GS/s 12b Time-Interleaved ADC for Direct RF Sampling in Modern Wireless Systems", IEEE™ ISSCC, 2023.
- [i.62] Ali A. M. A. et al.: "A 12b 18GS/s RF Sampling ADC with an Integrated Wideband Track-and-Hold Amplifier and Background Calibration", IEEE™ ISSCC, 2020.
- [i.63] Moon K.-J. et al.: "A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET", IEEE™ Symp. VLSI Circuits, pp. 172-173, 2022.
- [i.64] P. Caragiulo, C. Daigle, B. Murmann: "[DAC performance survey 1996-2020](#)", GitHub. (Accessed: March 10, 2023).
- [i.65] Tseng W.-H. et al.: "A 14b 16GS/s Time-Interleaving Direct-RF Synthesis DAC with T-DEM Achieving -70dBc IM3 up to 7.8GHz in 7nm", IEEE™ ISSCC, 2023.
- [i.66] Gruber D. et al.: "A 12b 16GS/s RF-Sampling Capacitive DAC for Multi-Band Soft- Radio Base-Station Applications with On-Chip Transmission-Line Matching Network in 16nm FinFET", IEEE™ ISSCC, pp. 174-175, 2021.
- [i.67] Huang H.-Y. et al.: "A 177mW 10GS/s NRZ DAC with Switching-Glitch Compensation Achieving > 64dBc SFDR and < -77dBc IM3", IEEE™ Symp. VLSI Circuits, June 2020.
- [i.68] Caragiulo P. et al.: "A 2× time-interleaved 28-GS/s 8-Bit 0.03-mm² switched-capacitor DAC in 16-nm FinFET CMOS", IEEE™ J. Solid-State Circuits, vol. 56, no. 8, pp. 2335-2346, August 2021.

- [i.69] Nazemi A. et al.: "A 36 Gb/s PAM4 transmitter using an 8b 18 GS/S DAC in 28 nm CMOS", in IEEE™ ISSCC, pp. 58-60, 2015.
- [i.70] Caragiulo P., Mattia O. E., Arbabian A., and Murmann B.: "A compact 14 GS/s 8-bit switched-capacitor DAC in 16 nm FinFET CMOS", in Proc. IEEE™ Symp. VLSI Circuits, 2020.
- [i.71] IEEE 802.15.3d™: "First Standardization Efforts for Sub-Terahertz Band Communications toward 6G", V. Petrov, T. Kurner, and I. Hosako, IEEE™ Communications Magazine, vol. 58, no. 11, pp. 28-33, 2020.
- [i.72] H. -J. Song, N. Lee: "Terahertz Communications: Challenges in the Next Decade", IEEE™ Transactions on Terahertz Science and Technology, vol. 12, no. 2, pp. 105-117, March 2022.
- [i.73] B. Murmann: "[Introduction to ADCs/DACs: Metrics, Topologies, Trade Space, and Applications](#)", ISSCC Short Course Presentation, February 2022.
- [i.74] B. Murmann: "[ADC Performance Survey 1997-2024](#)".
- [i.75] J. C. Candy, G. C. Temes: "Oversampling Delta-Sigma Data Converters", IEEE™ Press, 1992.
- [i.76] F. Maloberti: "High-speed data converters for communication systems", IEEE™ Circuits and Systems Magazine, vol. 1, no. 1, pp. 26-36, 2001.
- [i.77] M. Bolatkale et al.: "Next-Generation ADCs, High-Performance Power Management, and Technology Considerations for Advanced Integrated Circuits: Advances in Analog Circuit Design 2019", Springer, 2020.
- [i.78] H. Lin et al.: "ADC-DSP-Based 10-to-112-Gb/s Multi-Standard Receiver in 7-nm FinFET", IEEE™ Journal of Solid-State Circuits, vol. 56, no. 4, pp. 1265-1277, April 2021.
- [i.79] A. Agrawal et al.: "A 128Gb/s 1.95pJ/b D-Band Receiver with Integrated PLL and ADC in 22nm FinFET", 2023 IEEE™ International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 284-286.
- [i.80] "The Key Contiguous Spectrum Issue for 6G", in ATIS NextG-Spectrum-2022-00022R000.
- [i.81] D. C. M. Horvat et al.: "True Time-Delay Bandpass Beamforming", IEEE™ Journal of Oceanic Engineering, vol. 17, no. 2, pp. 185-192, April 1992.
- [i.82] R. Rotman et al.: "True Time Delay in Phased Arrays", Proceedings of the IEEE, vol. 104, no. 3, pp. 504-518, January 2016.
- [i.83] E. Ghaderi et al.: "An Integrated Discrete-Time Delay-Compensating Technique for Large-Array Beamformers", IEEE™ Transactions on Circuits and Systems, vol. 66, no. 9, pp. 3296-3306, August 2019.
- [i.84] J. M. Eckhardt: "THz Communications in a Data Center: Channel Measurements, Modeling and Physical Layer Analysis", Düren, Germany: Shaker Verlag, 2024.
- [i.85] J. M. Eckhardt, C. Herold, B. K. Jung, N. Dreyer, and T. Kürner: "Modular link level simulator for the physical layer of beyond 5G wireless communication systems", Radio Sci., vol. 57, no. 2, February 2022. doi: 10.1029/2021RS007395.
- [i.86] J. M. Eckhardt, C. Herold, S. Kroos, and T. Kürner: "Impact of RF Impairments on THz Links in a Data Center", COST CA10120 TD(24) 08008.
- [i.87] L. John, A. Tessmann, A. Leuther, P. Neining, T. Merkle, and T. Zwick: "Broadband 300-GHz power amplifier MMICs in InGaAs mHEMT technology", IEEE™ Trans. THz Sci. Technol., vol. 10, no. 3, pp. 309-320, May 2020. doi: 10.1109/TTHZ.2020.2965808.
- [i.88] D. Moro-Melgar, O. Cojocari, I. Oprea, H. Hoefle, and M. Rickes: "High power discrete schottky diodes based 275-305 GHz transceiver for FMCW-radar", in Proc. 29th IEEE™ Int. Symp. Space THz Technol. (ISSTT2018), Pasadena, Ca, USA, Mar. 2018.

- [i.89] M. C. Jeruchim, P. Balaban, and K. S. Shanmugan: "Simulation of Communication Systems: Modeling, Methodology, and Techniques (Information Technology: Transmission, Processing, and Storage)", J. K. Wolf, J. E. Mazo, J. Proakis, and W. H. Tranter, red. Boston, MA: Springer US, 2000. doi: 10.1007/b117713.
- [i.90] L. Anttila, M. Valkama, and M. Renfors: "Frequency-selective I/Q mismatch calibration of wideband direct-conversion transmitters", *IEEE™ Trans. Circuits Syst. II*, vol. 55, no. 4, pp. 359-363, April 2008. doi: 10.1109/TCSII.2008.919500.
- [i.91] M. Hudlička, M. Salhi, T. Kleine-Ostmann, and T. Schrader: "Characterization of a 300-GHz transmission system for digital communications", *J. Infrared Millim. Terahz Waves*, vol. 38, no. 8, pp. 1004-1018, August 1, 2017. doi: 10.1007/s10762-017-0395-9.
- [i.92] J. C. Scheytt, D. Wrana, M. Bahmanian, and I. Kallfass: "Ultra-low phase noise frequency synthesis for THz".
- [i.93] J. M. Eckhardt, T. Doeker, and T. Kürner: "Channel Measurements at 300 GHz for Low Terahertz Links in a Data Center", *IEEE™ Open J. Antennas Propag.*, vol. 5, no. 3, pp. 759-777, 2024. doi: 10.1109/OJAP.2024.3391798.
- [i.94] IEEE Std 802.15.3d™-2017: "IEEE Standard for High Data Rate Wireless Multi-Media Networks--Amendment 2: 100 Gb/s Wireless Switched Point-to-Point Physical Layer", Amendment to IEEE Std 802.15.3™-2016 as amended by IEEE Std 802.15.3e™-2017, vol., no., pp.1-55, 18 October 2017, doi: 10.1109/IEEESTD.2017.8066476.
- [i.95] T. Kürner et al.: "THz Communications and the Demonstration in the ThoR-Backhaul Link", in *IEEE™ Transactions on Terahertz Science and Technology*, doi: 10.1109/TTHZ.2024.3415480.
- [i.96] S. Ravichandran et al.: "Packaging Approaches for mm Wave and Sub-THz Communication", 2019 *IEEE™ MTT-S International Microwave Conference on Hardware and Systems for 5G and Beyond (IMC-5G)*.
- [i.97] S. T. Nicolson, A. Tomkins, K. W. Tang, A. Cathelin, D. Belot and S. P. Voinigescu: "A 1.2V, 140 GHz receiver with on-die antenna in 65nm CMOS", 2008 *IEEE™ Radio Frequency Integrated Circuits Symposium*, Atlanta, GA, USA, 2008.
- [i.98] S. Zeinolabedinzadeh et al.: "A 314 GHz, fully-integrated SiGe transmitter and receiver with integrated antenna", 2014 *IEEE™ Radio Frequency Integrated Circuits Symposium*, Tampa, FL, USA, 2014.
- [i.99] S. Li, Z. Zhang and G. M. Rebeiz: "An Eight-Element 136-147 GHz Wafer-Scale Phased-Array Transmitter With 32 dBm Peak EIRP and >16 Gbps 16QAM and 64QAM Operation", in *IEEE™ Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1635-1648, June 2022.
- [i.100] M. Boers et al.: "A 16TX/16RX 60 GHz 802.11ad Chipset With Single Coaxial Interface and Polarization Diversity", in *IEEE™ Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3031-3045, December 2014.
- [i.101] A. Ahmed, L. Li, M. Jung, S. Li, D. Baltimas and G. M. Rebeiz: "140-GHz 2-D Scalable On-Grid 8 \times 8-Element Transmit-Receive Phased Arrays With Up/Down Converters Demonstrating a 5.2-m Link at 16 Gbps", in *IEEE™ Transactions on Microwave Theory and Techniques*.
- [i.102] S. Oh and J. Oh: "140-GHz Affordable Miniaturized Array Antenna-on-Package for Sub-THz Transceiver", in *IEEE™ Access*, vol. 11, pp. 132780-132791, 2023.
- [i.103] A. Bhutani, B. Goettel, T. Streitz, S. Scherr, W. Winkler and T. Zwick: "Low-cost antenna-in-package solution for 122 GHz radar module", 2016 46th *European Microwave Conference (EuMC)*, London, UK, 2016, pp. 1469-1472.
- [i.104] X. Gu, D. Liu and B. Sadhu: "Packaging and Antenna Integration for Silicon-Based Millimeter-Wave Phased Arrays: 5G and Beyond", in *IEEE™ Journal of Microwaves*, vol. 1, no. 1, pp. 123-134, January 2021.

- [i.105] S. Shahramian et al.: "Practical Approaches to Industrializing Near-THz Communication Systems", 2023 IEEE™ BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA, 2023, pp. 5-8.
- [i.106] M. Urteaga, Z. Griffith, M. Seo, J. Hacker and M. J. W. Rodwell: "InP HBT Technologies for THz Integrated Circuits", in Proceedings of the IEEE, vol. 105, no. 6, pp. 1051-1067, June 2017.
- [i.107] S. Ma et al.: "A 140GHz 4TX-4RX Phased-Array FMCW-FSK Antenna-Packaged Radar Chipset With 25dBm EIRP and 16GHz BW", 2022 IEEE™ Asian Solid-State Circuits Conference (A-SSCC), Taipei, Taiwan, 2022, pp. 1-3.
- [i.108] A. Ahmed, L. Li, M. Jung and G. M. Rebeiz: "A 140 GHz Scalable On-Grid 8×8-Element Transmit-Receive Phased-Array with Up/Down Converters and 64QAM/24 Gbps Data Rates", 2023 IEEE™ Radio Frequency Integrated Circuits Symposium (RFIC), San Diego, CA, USA, 2023, pp. 93-96.
- [i.109] M. Elkhoully et al.: "Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules", 2022 IEEE™ International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 76-78.
- [i.110] Tadao Nagatsuma et al.: "Recent Progress and Future Prospect of Photonics-Enabled Terahertz Communications Research", IEICE Transactions on electronics, E-98-C, (2015) no. 12, pp. 1060-1070.
- [i.111] Tadao Nagatsuma et al.: "Advances in Terahertz Communications Accelerated by Photonics", Nature Photon 10, (2016), pp. 371-379.
- [i.112] Minkyu Sung et al.: "Design Considerations of Photonic THz Communications for 6G Networks", IEEE™ Wireless Communications, 28, (2021), no. 5, pp. 185-191.
- [i.113] Hae Young Rha et al.: "Novel Phase and CFO Estimation DSP for Photonics-Based Sub-Thz Communication", J. Lightwave Technol. 40, (2022), pp. 2710-2716.
- [i.114] Xiang Zhou et al.: "Advanced DSP for 400 Gb/s and Beyond Optical Networks", J. Lightwave Technol. 32, (2014), pp. 2716-2725.
- [i.115] Timo Pfau et al.: "Hardware-Efficient Coherent Digital Receiver Concept With Feedforward Carrier Recovery for *M*-QAM Constellations", J. Lightwave Technol. 27, (2009), pp. 989-999.
- [i.116] NNT Innovative Devices: "[UTC-Photomixer Module](#)".
- [i.117] Sang-Rok Moon et al.: "6G Indoor Network Enabled by Photonics- and Electronics-Based sub-THz Technology", J. Lightwave Technol. 40, (2022), pp. 499-510.
- [i.118] Hiroshi Ito et al.: "Terahertz-wave detector on silicon carbide platform", Appl. Phys. Express 15, (2022).
- [i.119] Sang-Rok Moon et al.: "Demonstration of Photonics-Aided Terahertz Wireless Transmission System with Using Silicon Photonics Circuit", Optics Express 28, (2020), pp. 23397-23408.
- [i.120] C. Castro et al.: "32 GBd 16QAM Wireless Transmission in the 300 GHz Band using a PIN Diode for THz Upconversion", 2019 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, (2019), pp. 1-3.
- [i.121] X. Li et al.: "132-Gb/s Photonics-Aided Single-Carrier Wireless Terahertz-Wave Signal Transmission at 450GHz Enabled by 64QAM Modulation and Probabilistic Shaping", 2019 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, (2019), pp. 1-3.
- [i.122] S. Jia et al.: "Integrated Dual-DFB Laser for 408 GHz Carrier Generation Enabling 131 Gbit/s Wireless Transmission over 10.7 Meters", 2019 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, (2019), pp. 1-3.
- [i.123] Sang-Rok Moon et al.: "Cost-Effective Photonics-Based THz Wireless Transmission Using PAM-N Signals in the 0.3 THz Band", in Journal of Lightwave Technology 39, (2021), pp. 357-362.

- [i.124] Eon-sang Kim et al.: "Cost-effective Photonics-Based THz Wireless Delivery System Using a Directly Modulated DFB-LD", *Optics Communications*, 492, (2021), pp. 126969.
- [i.125] Shiwei Wang et al.: "26.8-m THz wireless transmission of probabilistic shaping 16-QAM-OFDM signals", *APL Photonics* 5, (2020), pp. 056105.
- [i.126] Harter T. et al.: "Generalized Kramers-Kronig receiver for coherent terahertz communications". *Nat. Photonics* 14, (2020), pp. 601-606.
- [i.127] J. Ding et al.: "104-m Terahertz-Wave Wireless Transmission Employing 124.8-Gbit/s PS-256QAM Signal", *2022 Optical Fiber Communications Conference and Exhibition (OFC)*, San Diego, CA, USA, (2022), pp. 1-3.
- [i.128] Sooyeon Kim et al.: "Packaging of an amplifier module for sub-THz wireless transmission based on photonics", *Journal of Electromagnetic Engineering and Science* 23, (2023), pp. 470-481.
- [i.129] W. Li et al.: "Photonics-assisted 320 GHz THz-band 50 Gbit/s Signal Outdoor Wireless Communication over 850 Meters", *2023 Optical Fiber Communications Conference and Exhibition (OFC)*, San Diego, CA, USA, (2023), pp. 1-3.
- [i.130] H. Ibili et al.: "Plasmonic On-Chip Antenna Enabling Fully Passive sub-THz-to-Optical Receiver for Future RoF Systems", *Optical Fiber Communication Conference (OFC)*, 2024.
- [i.131] J.M. Singley, V.J. Urick, J.F. Diehl, K.J. Williams, and F. Bucholtz: "Increased performance of single-channel analog photonic links enabled by optical wavelength-division multiplexing", *IEEE™ Trans. Micro. Theory Tech.* 67 (3) (2019).
- [i.132] Z. Gong et al.: "LNOI waveguide grating based true time delay line for tunable bandpass microwave photonic filter", *Optical and Quantum Electronics*, Vol. 52, no. 427 (2020).
- [i.133] Fortier T. M. et al.: "Generation of ultrastable microwaves via optical frequency division". *Nat. Photon.* 5, 425-429 (2011).
- [i.134] Sun S., Wang B., Liu K. et al.: "Integrated optical frequency division for microwave and mmWave generation". *Nature* 627, 540-545 (2024).

3 Definition of terms, symbols and abbreviations

3.1 Terms

Void.

3.2 Symbols

Void.

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

3GPP	3G (mobile) Partnership Project
6G	Six Generation
A/W	Amperes per Watt of incident radiated power
ACLR	Adjacent Channel Leakage Ratio
ADC	Analog-Digital Converter
AE	Antenna Element
AiP	Antenna-in-Package
AM	Amplitude Modulation
AMAM	AMplitude to Amplitude Modulation

AMPM	AMplitude to Phase Modulation
AoD	Angle of Departure
AR	AutoRegressive
ASE	Amplified Spontaneous Emission
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BF	Beam Forming
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BS	Base Station
BW	BandWidth
CFO	Carrier Frequency Offset
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous Wave
DAC	Digital-Analog Converter
DC	Direct Current
DFB	Distributed FeedBack
DFB-LD	Distributed FeedBack - Laser Diode
DHBT	Double Heterojunction Bipolar Transistor
DL2	Direct Link 2
DR	Dynamic Range
DSP	Digital Signal Processing
EAM	Electro-Absorption Modulator
EDFA	Erbium Doped Fiber Amplifier
EIRP	Effective Isotropically Radiated Power
ENOB	Effective Number Of Bits
EVM	Error Vector Magnitude
FIR	Finite Impulse Response
FMBD	Fermi-level Managed Barrier Diode
FOM	Figure Of Merit
FS	Full Scale
GaN	Gallium Nitride
GS	GigaSample
HBF	Hybrid BeamForming
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
I/Q	In- / Quadrature-
IC	Integrated Circuit
ID	IDentification
IDC	DC Current
IMD	InterModulation Distortion
InP	Indium Phosphide
IPN	Integrated Phase Noise
IQ	In- / Quadrature-
ISAC	Integrated Communication And Sensing
LC	Inductor - Capacitor
LCP	Liquid Crystal Polymers
LD	Laser Diode
LDPC	Low Density Parity Check
LiNbO	Lithium Niobate Oxide
LLS	Link Level Simulator
LNA	Low Noise Amplifier
LNOI	Lithium Niobate On Insulator
LO	Local Insulator
LSB	Least Significant Bit
LTCC	Low Temperature Cofired Ceramic
mA	milli-Amper
MEMS	Micro Electro-Mechanical System
MMIC	Microwave Monolithic Integrated Circuit Transistor
mV	milli-Volt
MZM	Mach-Zehnder Modulator
NF	Noise Figure
NR	New Radio

NRZ	Non Return to Zero
NSD	Noise Spectral Density
OBPF	Optical BandPass Filter
OFD	Optical Frequency Division
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-Off Keying
P2P	Peer to Peer
PA	Power Amplifier
PAE	Power Added Efficiency
PAM-N	Pulse Amplitude Modulation with N levels
PCB	Printed Circuit Board
PD	Photo Diode
pHEMT	pseudomorphic High Electron Mobility Transistor
PIN	Positive - Intrinsic - Negative
PLL	Phase Locked Loop
PM	Phase Modulation
PN	Phase Noise
PRBS	Pseudo Random Bit Sequence
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RIN	Relative Intensity Noise
RRC	Root Raised Cosine
RZ	Return to Zero
SBD	Schottky Barrier Diode
SFDR	Spurious Free Dynamic Range
SiC	Silicon on Carbide
SINAD	Signal to Noise and Distortion ratio
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SOA	Semiconductor Optical Amplifier
SOI	Silicon On Insulator
SQNR	Signal to Quantization Noise Ratio
ToR	Top of Rack
TTD	True Time Delay
UE	User Equipment
UPA	Uniform Planar Array
UTC-PD	Uni-Traveling Carrier PhotoDiode
VOA	Variable Optical Attenuator

4 THz Transceiver Architectures

4.1 Transceivers for Communication and Sensing

Generally, in realizing a co-hardware ISAC platform, there are two representative transceiver design directions, which are:

- 1) the **communication-based** architecture, where sensing functionality is integrated and enabled; and
- 2) the **sensing-based** architecture, where the communication functionality is integrated and enabled [i.1] and [i.2].

From a practical and diverse solution perspective, it is noted that the **communication-based transceiver architecture is preferred** due to the fact that the existing communication networks have generally broader deployment compared to the sensing networks, where enabling the sensing functionality in making adequate use of the existing communication networks is a more feasible solution in terms of complexity, cost and efficiency [i.1] and [i.2], as well as that the merging trend of communication and sensing in terms of a communication-based **co-hardware** platform is observed [i.3].

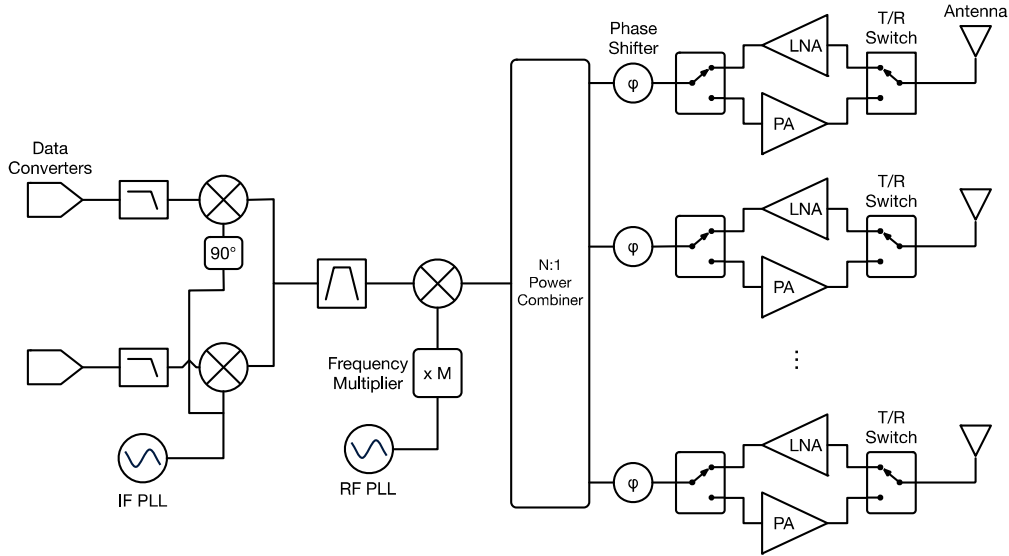


Figure 4.1-1

4.2 Beamforming Architectures

According to the trade-off assessment in literature in terms of the most dominant parameters for practical deployment [i.4] and [i.5], it is concluded that not all types of transceiver architectures are feasible in future communication systems. Specifically, the fully analogue architecture suffers from issues such as flexibility, and the fully digital architecture suffers from high power consumption, computational complexity and cost, especially at high data rates and large bandwidth in the THz band. As a result, it is envisioned that the **Hybrid Beamforming architecture (HBF)** would stand out to be considered as the most feasible solution, which will leverage the benefits of both analogue and digital beamforming architectures. An abstracted hybrid beamforming architecture [i.1] and [i.6] is provided in Figure 4.2-1, where N_s denotes the number of streams, N_{RF} denotes the number of RF chains, and N_t^{AE} denotes the number of Antenna Elements (AEs).

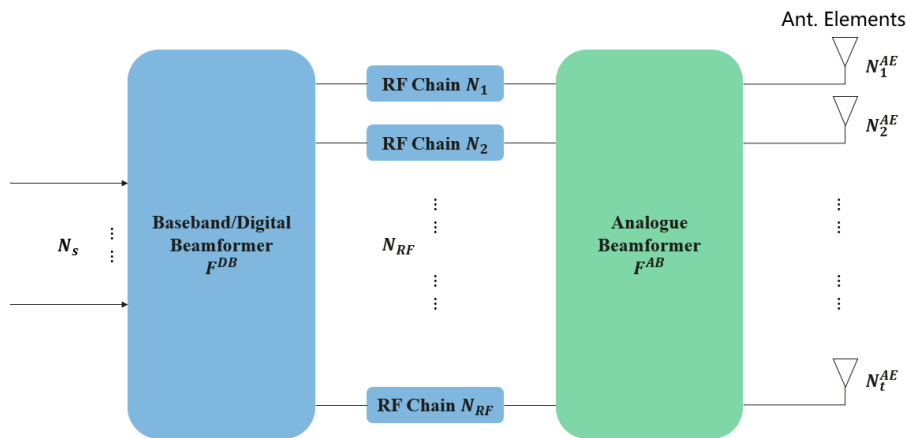


Figure 4.2-1: Abstracted Hybrid Beamforming Architecture

Depending on how the RF chains are connected to the AEs, there are three major types of HBF architectures, which result in different RF modeling considerations in providing an overall impairment model [i.1]. The first architecture is the **fully-connected HBF architecture**, which is demonstrated in Figure 4.2-2, where each RF chain is connected to all phase shifters and AEs, and the transmitted signal on each of the N_{RF} digital transceivers goes through N_t RF paths (mixer, power amplifier, phase shifter, etc.) and then be superimposed before being connected with each AE.

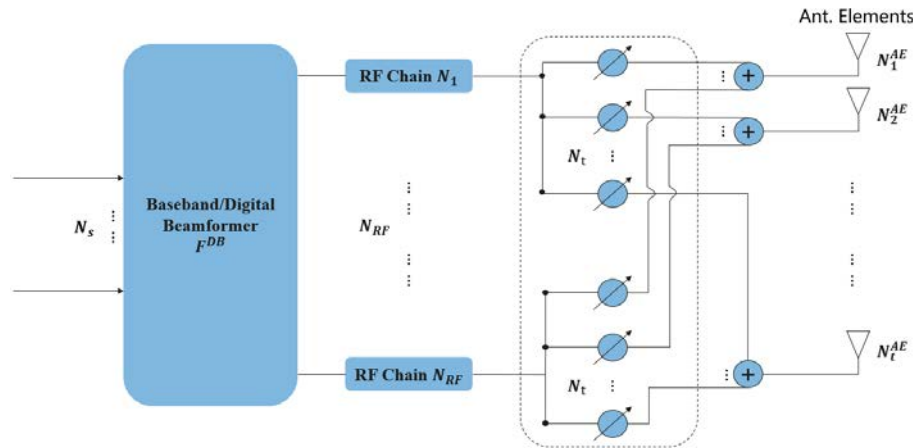


Figure 4.2-2: Fully-Connected Hybrid Beamforming Architecture

The second architecture is the **partially-connected HBF architecture**, which is depicted in Figure 4.2-3, where each of the N_{RF} RF chain is connected to a portion of N_t/N_{RF} number of phase shifters and sub-arrays. Therefore, it is notably different to the fully-connected HBF architecture, and the systematic RF impairment model would also vary.

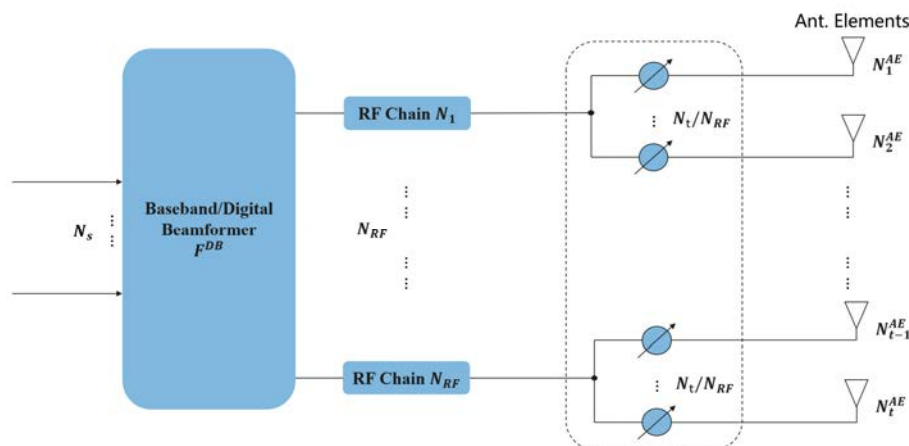


Figure 4.2-3: Partially-Connected Hybrid Beamforming Architecture

Lastly, to provide more adaptive beam control capability, the fixed circuit connection in the partially-connected architecture may also be modified, which gives the **dynamically-connected HBF architecture**, as shown in Figure 4.2-4. As can be noticed, a switching network is added between the RF chains and the AEs to offer more processing freedom. Therefore, as the THz signals are processed depending on the status of the switching circuit, effective building blocks may also vary, and the systematic impairment model may be different.

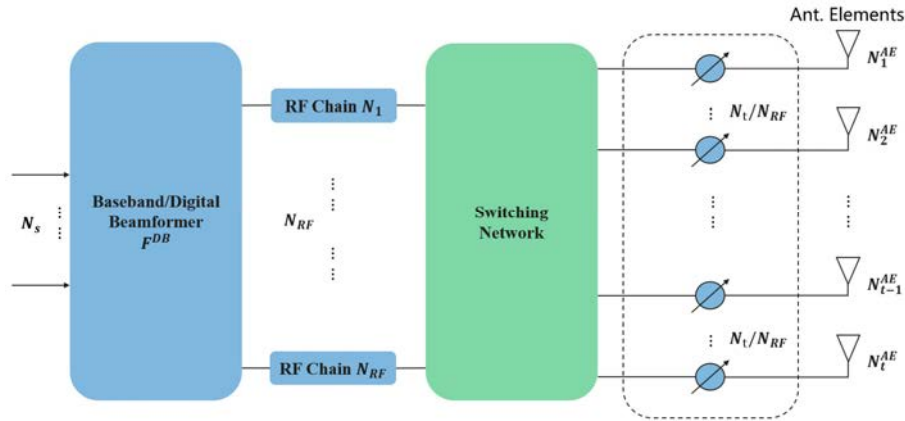


Figure 4.2-4: Dynamically-Connected Hybrid Beamforming Architecture

As the three most representative architectures, their pros and cons are briefly summarized in Table 4.2-1, which suggests more suitable deployment options for modeling the systematic impairment effect. For example, considering stringent constraints at the UE side, such as power, the partially-connected HBF architecture may be considered practical as a practical UE reference architecture, whilst all three HBF architectures may be considered practical as the reference architectures for the BS side.

Table 4.2-1: Brief Summary of Pros and Cons of the Representative Architectures

Architecture	Pros	Cons	Feasible Deployment
Fully-Connected	Better BF flexibility and multi-beam performance	High complexity	BS
Partially-Connected	Low complexity	Worse multi-beam performance	BS, UE
Dynamically-Connected	Better BF flexibility and performance	Complexity (switches)	BS

The necessity of a systematic/overall model can be observed from the fact that the hardware impairments would aggregate, thus changing the impact on the system performance depending on the adopted transceiver architecture, which has also led to the attempts on the aggregated hardware impairments modeling such as [i.7], [i.8] and [i.9]. Therefore, in case the present report only provides the model of each building block, the overall impairment effect on the THz signal would still be unknown. On the contrary, providing overall models of the representative architectures may be easier in latter evaluation of the THz-ISAC systems, as they could be used as benchmarks.

4.3 Interference Cancellation

In clause 4.2, HBF fully-/partially-/dynamically-connected architectures were discussed (as shown in Figures 4.2-1 to 4.2-4). Although the architectures share mostly the same hardware building blocks, it is also noted that:

- 1) in different THz-ISAC transceiver architectures, the transmitted signals go through different paths (mixer, power amplifiers, phase shifters, etc.) and are superimposed before being connected with each AE;
- 2) the systematic RF impairment model depends on the considered architecture and the paths through which the signals are processed [i.1], [i.10] and [i.11].

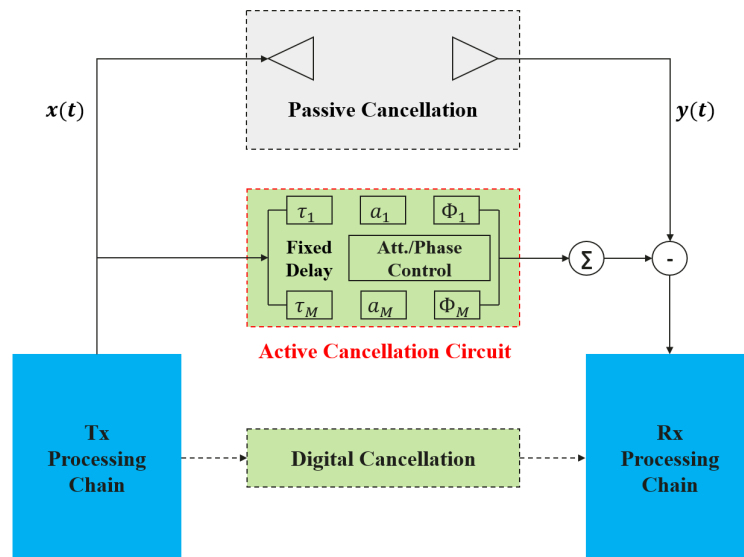


Figure 4.3-1: Example Hardware Modification to the Conventional Architectures (Additional Cancellation Circuit)

In addition, example modifications to the architecture are presented by taking the co-hardware design into consideration, which may also lead to a different impairment model due to the fact that extra blocks may be introduced, and the signals are processed and affected by the **added building blocks**. For example, in a typical ISAC architecture, the co-hardware device is simultaneously used as a communication transmitter and a sensing transceiver. Hence, the reflected echoes of the communication signals are received by the same antenna arrays. With this application in mind, the Simultaneous Transmission And Reception (STAR) mode, as a representative ISAC functionality, may be adopted. Therefore, sufficient Tx-Rx isolation, which refers to the passive self-interference cancellation, may be considered. Besides, **an extra cancelling path** may also be considered [i.12] to further mitigate the leakage effect. As an example, the authors in [i.13] have proposed **an active cancellation circuit**, as depicted in Figure 5.1-1, where the non-ideal attenuators and phase shifters are extensively adopted. Hence, at the Rx side, the output signal that has been processed by the cancellation circuit, which is absent in conventional transceiver architectures, would require a different impairment model to describe the effect.

After considering an architectural perspective on the design aspects of sub-THz transceivers, in the next subsections, several individual RF impairments models such as PA nonlinearities and oscillator phase noise are covered.

5 Modeling of Transceiver Building Blocks

5.1 Signal Path Components

5.1.1 Receiver Noise Figure and Nonlinearity

5.1.1.1 High Level Modeling

The receiver characteristics impact the signal-to-noise-and-distortion ratio (SNDR) and, in turn, the overall system throughput. At low receiver input power, the SNR is primarily determined by thermal noise $N = -174 \text{ dBm/Hz} + \text{NF} + 10\log_{10}(\text{BW})$, i.e. receiver noise figure, channel bandwidth, and ADC (thermal and quantization) noise. At high receiver input power, the nonlinear distortion and phase noise dominate and limit the overall SNDR.

In (sub-)THz frequencies, the potential use of large bandwidth will result in higher noise floor, hence imposing a more challenging noise figure and nonlinearity design margin. Hence, it is important to model the Rx nonlinearity in the link performance evaluation for THz band communication systems.

(Sub-)THz wireless communication receivers feature a complex down-conversion path, including a low noise amplifier, phase shifter, mixers and analog baseband filters. Each stage has its own gain, nonlinearity and noise figure. A simplified illustration of such multi-stage receiver is presented in Figure 5.1-1.

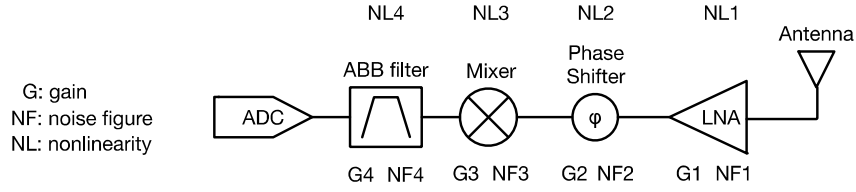


Figure 5.1-1: Simplified illustration of Multi-Stage Receiver

For end-to-end link performance simulation, typically the whole Rx chain before ADC is abstracted with a single gain, nonlinearity and noise figure as in Figure 5.1-2.

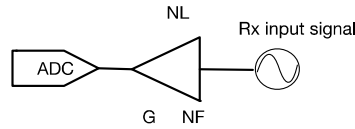


Figure 5.1-2: Simplified illustration of Multi-Stage Receiver

The overall gain and noise figure of the abstracted model are related to the original multi-stage receiver by the Friis formula [i.14] as:

$$G = G_1 G_2 \cdots G_n \quad (1)$$

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots + \frac{NF_n - 1}{G_1 G_2 \cdots G_{n-1}} \quad (2)$$

The nonlinearity of multiple cascaded stages can be aggregated into a single equivalent nonlinearity as well:

$$NL(input) = NL_1(NL_2(\cdots (NL_n(input)) \cdots)) \quad (3)$$

5.1.1.2 Nonlinearity Model of Receiver for THz Band

There are various nonlinearity models proposed in the literature, such as cubic polynomial, Saleh model and Rapp. For large signals where AMPM distortion is severe, models that can predict the AMPM curve are preferable, such as the Saleh model, or the modified Rapp model. For the receiver nonlinearity, on the other hand, due to the operation in the small signal region, AMPM is usually negligible and a simple AMAM distortion only model is adequate. The classical cubic polynomial model between the input amplitude $|x|$ and output amplitude $|y|$ assumed the form.

$$|y| = \alpha|x| + c|x|^3 \quad (4)$$

where α is the linear gain and c is the third order coefficient. The cubic polynomial coefficients and the third order intercept point ($IIP3_{dBm}$) are related by the following formula [i.14] and [i.15]:

$$c = \frac{\alpha}{10^{\frac{IIP3_{dBm} - 30}{10}}} \quad (5)$$

As can be seen, the cubic polynomial can be determined directly through the linear gain and the metric $IIP3_{dBm}$. Furthermore, for the nonlinearity modeling, the magnitude of the linear gain does not matter. Without loss of generality, it may be assumed that $\alpha = 1$.

5.1.1.3 Third-order intercept point IIP3dBm and the SNDR

To recommend the value of the parameter IIP3_{dBm} to be used for end-to-end link performance evaluation, a literature survey of sub-THz band communication systems was conducted. Table 5.1-1 summarizes the findings:

Table 5.1-1: Survey of receiver noise figure and nonlinearity metrics with different processes

Technology	Frequency (GHz)	NF (dB)	IIP3 (dBm)	IIP3_inferred@40 dB gain	Gain (dB)	Reference
130-nm SiGe	114 - 146	12,2	-13,4	-28,4	25	[i.16]
130-nm SiGe	119 - 130	11,8	-4,4	-24,1	20,3	[i.16]
130-nm SiGe	114 - 126	13	5	-22,5	12,5	[i.17]
28-nm CMOS	140 - 160	11	-33,2	-33,2	40	[i.18]
22-nm CMOS SOI	137 - 156	10	-19,2	-29,2	30	[i.19]
45-nm CMOS SOI	137 - 151	7	-25,2	-38,7	26,5	[i.20]

Some of the references report input 1 dB compression point (IP1_{dBm}) as the nonlinearity performance metrics while others report input referred 3rd order intercept (IIP3_{dBm}). The IP1_{dBm} is converted to IIP3_{dBm} through the following formula [i.14] and [i.15]:

$$IP1_{dBm} = IIP3_{dBm} - 9,6 \quad (6)$$

Furthermore, since the linear gain is different among the references, The equivalent IIP3_{dBm} at 40 dB gain is inferred by shifting the IIP3 as:

$$IIP3_{dBm,inferred@40dB\ gain} = IIP3_{dBm,reported} + Gain_{dB} - 40 \quad (7)$$

The performance of SiGe is in general better than CMOS. However, due to the manufacturing cost, CMOS or CMOS SOI is likely the preferred process. Therefore, using IIP3_{dBm} of -30 dBm (in-between [i.18] and [i.19], normalized to gain 40 dB), and noise figure of 12 dB as the baseline for receiver modeling for sub-THz communication system is proposed.

The input power (Pin_{dBm}), the input power 1 dB compression point (IP1_{dBm}), the third order intercept point (IIP3_{dBm}), the third order inter-modulation distortion (IMD3_{dBm}), and the Signal to IMD3 ratio (SDR_{dB}) are related through the following formulae:

$$IMD3_{dBm} = 3 \cdot Pin_{dBm} - 2 \cdot IIP3_{dBm} \quad (8)$$

$$SDR_{dB} = 2 \cdot IIP3_{dBm} - 2 \cdot Pin_{dBm} \quad (9)$$

The maximum SNDR for different possible signal bandwidths is evaluated in Table 5.1-2.

Table 5.1-2: SNDR assessment for NF = 12 dB and IIP3 = -30 dBm

Signal Bandwidth BW	Noise Level: -174 dBm/Hz + NF + 10log10(BW)	Signal Power @ Noise = IMD3	Maximum SNDR (IMD3 = Noise Level)
2 GHz	-69 dBm	-43 dBm	23 dB
4 GHz	-66 dBm	-42 dBm	21 dB
8 GHz	-63 dBm	-41 dBm	19 dB
16 GHz	-60 dBm	-40 dBm	17 dB

5.1.2 Transmitter Output Power

5.1.2.1 Role of Output Power

The most critical transmitter figure-of-merit is the Effective Isotropic Radiated Output Power (EIRP) which is calculated by the following formula:

$$EIRP(dBm) = P_{TX} - L_{TRsw} - L_{routing} + G_{TX} + 20\log(N) \quad (10)$$

Where P_{TX} is the power amplifier output power, L_{TRSW} is the loss of the T/R switch, $L_{routing}$ is the routing loss between the transmitter output and the antenna, G_{TX} is the transmitter antenna gain and N is the number of transmit chains. EIRP is directly related to Friis equation $P_{RX} = P_{TX} + G_{TX} + G_{RX} - 20 \log \frac{\lambda}{4\pi d} = EIRP + G_{RX} - 20 \log \frac{\lambda}{4\pi d}$, capturing the transmitter related terms.

A sub-THz communication system needs to be designed for a target EIRP that meets a certain link margin at the desired distance d . At the same time, the number of transmit chains N needs to be minimized to reduce system complexity and cost. Therefore, it is desirable to start with a power amplifier design that maximizes P_{TX} and does so in the most efficient way.

There are two metrics that are typically used to express P_{TX} :

- 1) output 1 dB compression point (OP1dB); and
- 2) saturated output power (Psat).

The latter is more relevant for constant amplitude modulations while the former is useful for variable envelope modulations. The difference between Psat and OP1dB generally depends on the semiconductor process and the transistor gain at the frequency of operation.

5.1.2.2 Power Amplifier Output Power and Efficiency

There are primarily three semiconductor technologies for sub-THz power amplifiers: Indium Phosphide (InP), Silicon-Germanium (SiGe) and CMOS. PAs designed with InP Heterojunction Bipolar Transistors (HBTs) generally feature better performance than silicon due to the significantly higher electron mobility of this semiconductor. However, there are two drawbacks with InP. First, existing InP processes do not lend themselves to high integration. Second, InP technology is not readily available and in high volume from commercial foundries.

There is a large body of published research covering all three technologies. Tables 5.1-3, 5.1-4 and 5.1-5 summarize the performance of several sub-THz PAs in InP, SiGe and CMOS respectively.

Table 5.1-3: InP Based Power Amplifiers

Source	Technology	Fc (GHz)	Gain (dB)	BW (GHz)	Psat (dBm)	OP1dB (dBm)	Psat-OP1dB	PAE (%)
[i.21]	250-nm InP HBT	140	12,3 - 15,9	43	18,9 - 20,5	17		20,8
[i.22]	800-nm InP-HBT	145	11		14	12	2	10
[i.23]	250-nm InP HBT	115 - 140	19,8	24,4	21	20,4	0,6	23
[i.24]	250-nm InP HBT	132,5	15 - 17,5	35	21 - 21,8			8,2 - 10,5
[i.25]	250-nm InP HBT	139	19 - 21	26	27,4			13 - 16,4
[i.26]	250-nm InP HBT	275	20,8	35	1,8	-3,3	5,1	0,98

Table 5.1-4: SiGe BiCMOS Power Amplifiers

Source	Technology	Fc (GHz)	Gain (dB)	BW (GHz)	Psat (dBm)	OP1dB (dBm)	Psat-OP1dB	PAE (%)
[i.27]	130-nm SiGe BiCMOS	181,5		27	18,7			4,4
[i.28]	130-nm SiGe BiCMOS	210	25	20	9,6	4	5,6	0,5
[i.29]	130-nm SiGe BiCMOS	237	16,4	52	14,7	11,5	3,2	3,13
[i.30]	130-nm SiGe BiCMOS	136,5	24	53	14,2	12,3	1,9	9,26
[i.31]	130-nm SiGe BiCMOS	180	10	80	15	14	1	3,5

Table 5.1-5: CMOS Power Amplifiers

Source	Technology	Fc (GHz)	Gain (dB)	BW (GHz)	Psat (dBm)	OP1dB (dBm)	Psat-OP1dB	PAE (%)
[i.32]	28-nm CMOS	135	21,9	20	11,8			10,7
[i.33]	16-nm FinFET	135	19	22	13,1	7,1	6	11
[i.34]	40-nm CMOS	140	20,3	17	14,8	10,7	4,1	8,9
[i.35]	65-nm CMOS	140	15	> 30	13,2	9,9	3,3	14,6
[i.36]	45-nm SOI	202	14,6	9,4	18,7	12,1	6,6	4,8
[i.37]	65-nm CMOS	202	19,5	14	9,4	6,3	3,2	1

The PAE in all technologies degrades rapidly above 200 GHz and is generally less than 5 %. This is attributed to the fact that most power generated by the PA is lost in passive structures (transmission lines, matching networks, etc.) after the last stage.

InP PAs can achieve the higher output power, above 20 dBm in many cases at 140 GHz with ~20 % PAE. This is by far the highest performance that any other semiconductor process examined in the contribution. As a result, InP could be a viable option for infrastructure components. CMOS and SiGe PA Saturated Output Power (Psat) is approximately the same and limited to below 15 dBm (excluding some outliers). Reasonable output power and efficiency can only be achieved in frequencies below 200 GHz.

5.1.3 Power Amplifier Nonlinearity Modeling

The Rapp model [i.38] is widely used for the amplitude to amplitude (AM-AM) distortion and the amplitude to the phase (AM-PM) distortion. In 5G, the modified Rapp model [i.39] and [i.40] was agreed as the baseline model for link level evaluations. The modified Rapp model can be described by the following equations:

$$F_{AM-AM}(x) = \frac{Gx}{\left(1 + \left|\frac{Gx}{V_{sat}}\right|^{2p}\right)^{\frac{1}{2p}}}, \quad (11a)$$

$$F_{AM-PM}(x) = \frac{Ax^q}{\left(1 + \left|\frac{x}{B}\right|^q\right)^q}, \quad (11b)$$

where $F_{AM-AM}(x)$, $F_{AM-PM}(x)$ are the AM-AM and AM-PM distortions, respectively. G is the small signal gain, p is the smoothness factor, V_{sat} is the saturation voltage. Coefficient A , B , q are AM-PM distortion curve parameters.

AM-AM Rapp model parameters (G , p , V_{sat}) for several recently published sub-THz PAs were extracted by curve fitting of AM-AM (Pout vs Pin) data and are summarize in Table 5.1-6.

Table 5.1-6: Power amplifier parameters in sub-THz band

Source	Technology	Fc (GHz)	Gain (dB)	BW (GHz)	Psat (dBm)	PAE (%)	G	Vsat	p
[i.34]	28-nm CMOS	135	21,9	20	11,8	10,7	12,2 6	0,9	1,93
[i.27]	130-nm SiGe BiCMOS 3 stage cascode topology	160	20,2	27	18,7	3,9	9,88	1,81	2,75
[i.27]	130-nm SiGe BiCMOS Common Emitter	185	6,3	27	13,5	20	4,08	1,41	1,91
[i.27]	130-nm SiGe BiCMOS Cascode topology	185	12,3	27	15,8	19,6	2,05	1,09	2,031
[i.21]	250-nm InP HBT	140	12,3 - 15,9	43	18,9 - 20,5	20,8	10,1 3	0,37	1,38
[i.22]	800-nm InP-DHBT	145	11	N/A	14	10	3,54	0,17 1	1,69
[i.23]	250-nm InP HBT	115 - 140	19,8	24,4	21	23	10,3 8	0,52 3	1,45
[i.41]	40-nm CMOS	115 - 139	7,9	24	-0,7	N/A	9,82	0,03	1,09
Average for sub-THz PA modeling		100 - 200	6,3 - 21,9	20 ~ 43	-0,7 - 21	3 - 23	7,76	0,79	1,78
3GPP [i.39]		30 - 70					16	1,9	1,1

As shown in the Table 5.1-6, $G = 7,76$, $V_{sat} = 0,79$, $p = 1,78$ can be considered as nominal parameters for sub-THz Tx PA nonlinearity modeling. Figure 5.1-3 illustrates AM-AM distortion modeling comparison between 5G NR and sub-THz. It is observed that sub-THz PA has less gain and sharper transition to saturation point than the 5G PA model.

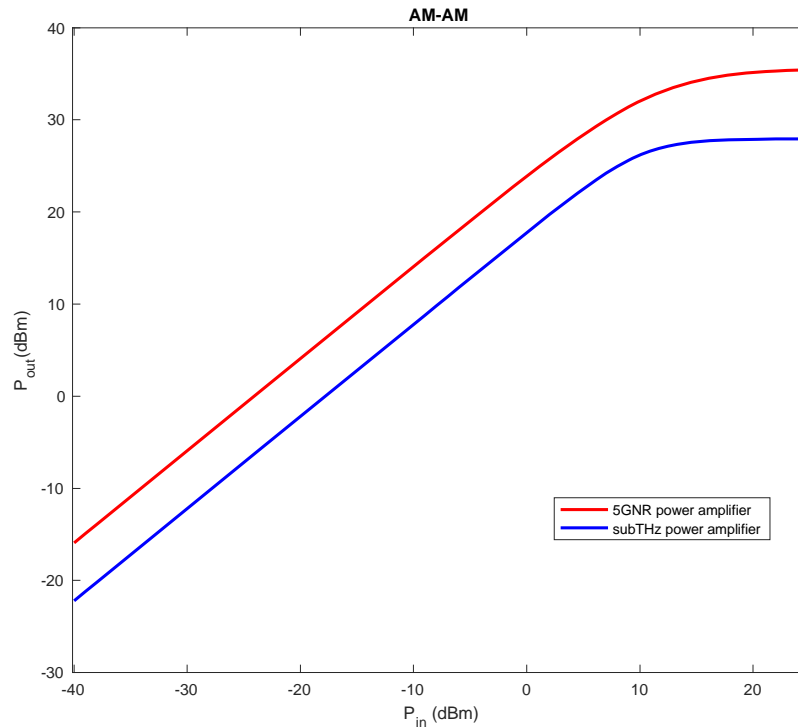


Figure 5.1-3: AM-AM distortion modeling comparison between 5G NR and sub-THz

5.2 Clocking Components

5.2.1 Phase Noise Profiles of Phase Locked Loops and Frequency Multipliers

Ideally, a local oscillator would produce a sinusoidal signal, whose power spectrum is a delta function at the carrier frequency, but in reality its output power appears also in a band around the desired frequency. Several models for the Power Spectral Density (PSD) of the phase $\phi(t)$ can be found. The analysis of real oscillators is based on direct measurements of the PSD of $\phi(t)$ or of the phasor $e^{i\phi(t)}$. These measurements are related to the carrier frequency and are given in dBc/Hz.

As illustrated in Figure 4.1-1, most commonly used RF transceivers employ Phase Locked Loops (PLLs) to partially compensate the phase noise of the RF oscillator. The PLL may be followed by a frequency multiplier to further increase the output frequency of the oscillator. The PLL - Multiplier scheme is typically employed in the first down-conversion (i.e. heterodyning step of the transceiver) where a very high clock frequency is required.

Figure 5.2-1 shows the typical block diagram of a PLL followed by a frequency multiplier. The cascade of the two blocks is sometimes referred as a Frequency Generator. The PLL is a negative feedback system with gain $G_{PLL} = 20 \log_{10}(f_{out}/f_{in})$ within the loop bandwidth f_{BW} . f_{out} and f_{in} are the output and reference frequencies respectively. The PLL bandwidth typically extends from hundreds of kHz up to a few MHz.

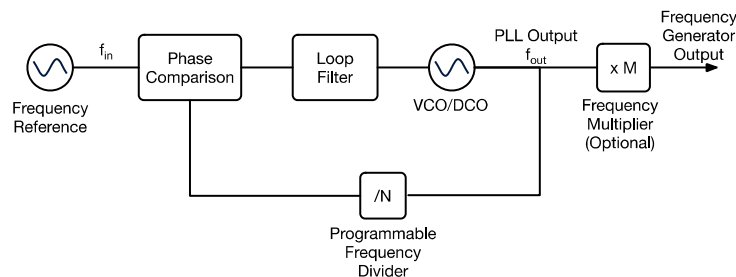


Figure 5.2-1: PLL/Frequency Generator Block Diagram

The phase noise within the loop bandwidth is set by the reference oscillator which employs a very high Q resonator, typically quartz crystal or MEMS based. Outside of the loop bandwidth, the PLL phase noise is determined by the phase noise of the RF oscillator, whose phase noise PSD decreases over frequency with 20 dB/decade slope [i.42] and [i.43].

The frequency multiplier-by-M exhibits phase noise gain similar to the PLL, $G_{mult} = 20 \log_{10}(f_{out}/f_{in})$ at frequency offsets close to the carrier. Being a tuned circuit, the multiplier will introduce some noise filtering at higher offsets. However, at sub-THz frequencies, filtering is expected to be limited due to the low Q factor of tuned LC tanks, unless the channel bandwidth exceeds 10 GHz. For this analysis, any phase noise filtering from buffers or frequency multipliers is ignored.

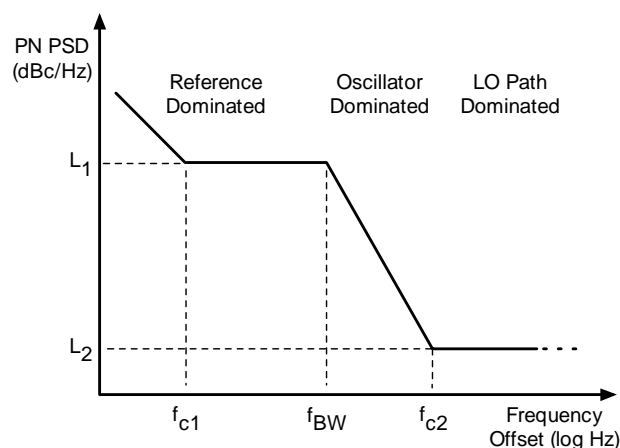


Figure 5.2-2: Typical RF LO Phase Noise Profile

When the RF oscillator noise is multiplied-by-M, its profile will not be altered and will remain decreasing with 20 dB/decade. Beyond a certain frequency offset, the decreasing trend will stop and the phase noise will flatten out as illustrated in Figure 5.2-2. This phase noise region is referred as "LO path dominated". The start frequency and noise level of the LO dominated region depend on the frequency multiplier design and most importantly, on the LO delivery circuits (e.g. LO buffers or splitters if applicable). Figure 5.2-2 illustrates a typical LO phase noise profile along with the three phase noise regions described above. The corner frequency f_{c1} is set by the reference oscillator and corresponds to the frequency where the noise filtering effect by the resonator (i.e. Leeson effect [i.42] and [i.43]) drops below the (white) thermal noise floor, usually set by the buffers following the oscillator. f_{c2} has a similar root cause as f_{c1} , but is set by the RF oscillator and the circuits that follow.

From the above analysis, the phase noise spectrum profile is split into three frequency regions:

- 1) Reference dominated region: A linear decay up to cut-off frequency f_{c1} , and flat spectrum L_1 between f_{c1} and the PLL loop bandwidth f_{BW} .
- 2) Oscillator dominated region: A linear decay slope of -20 dB/decade between f_{BW} and the second cut-off frequency f_{c2} .
- 3) LO Path dominated region: A flat spectrum L_2 beyond f_{c2} .

Reference Dominated Phase Noise

A design-based approach to modeling the reference dominated phase noise is to start from available frequency references and their respective phase noise. Add the phase noise gain of PLL and frequency multiplier along with PLL and frequency multiplier "implementation loss". The implementation loss is primarily due to noise originating from the PLL loop components, upconverted by the oscillator.

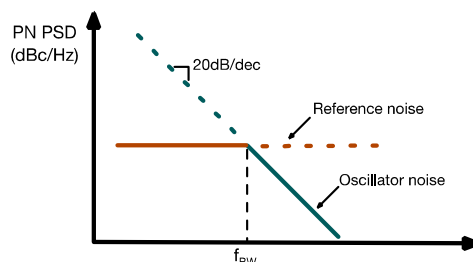
The phase noise profiles of frequency references can vary widely based on their size, power consumption and cost. Some are more suitable for UE or local area BS, e.g. [i.44] and [i.45] while others for medium range or wide area BSs, e.g. [i.46] and [i.47]. After comparing datasheets [i.44], [i.45], [i.46] and [i.47], the f_{c1} and L_1 (scaled to 140 GHz) of Table 5.2-1 are proposed.

Table 5.2-1: Typical RF LO Phase Noise Profile

Parameter	UE or local area BS	Medium range or wide area BS
f_{c1}	50 kHz	50 kHz
L_1	-85 dBc/Hz	-96 dBc/Hz

RF Oscillator Dominated Phase Noise

In the proposed phase noise profile of Figure 5.2-2, the noise of the RF oscillator is modelled by the loop bandwidth of the PLL, f_{BW} . The reasoning is that the PLL bandwidth is set to the frequency at which the amplified reference noise intersects with the oscillator noise [i.42] and [i.43] as illustrated in Figure 5.2-3. Assuming that the reference noise is fixed, higher oscillator noise requires higher f_{BW} to reduce the total (integrated) phase noise.

**Figure 5.2-3: PLL loop bandwidth as a trade-off between reference and RF oscillator noise**

In general, lower oscillator noise requires higher power dissipation. As a result, in portable devices, it is preferable to keep oscillator current low and use the widest possible loop bandwidth. Modern digital PLLs can achieve loop bandwidths of about 1 MHz to 2 MHz with excellent phase noise [i.88] and [i.89]. f_{BW} set to 1 MHz regardless of the RF LO frequency is proposed.

Medium range or wide area BSs can afford higher RF oscillator power dissipation. After comparing the phase noise data of the high-performance oscillators [i.90], [i.91], [i.92] and [i.93] and assuming $L_1 = -96$ dBc/Hz, f_{BW} set to 0,9 MHz regardless of the RF LO frequency for this device category is proposed.

LO Path Dominated Phase Noise

The LO path dominated phase noise indicated in Figure 5.2-2 is often ignored in the literature, but it is especially important for future THz communication and sensing systems. The receiver SNR cannot exceed the Integrated single sideband Phase Noise (IPN) from a few kHz up to the channel bandwidth. As channel bandwidth increases, the contribution of the LO path dominated phase noise will also increase, eventually setting an upper limit to the receiver SNR.

The authors in [i.94] consider several phase noise models, including the ones for IEEE, 3GPP (30-A, 60-B) and low frequency commercial devices (LMX2591 and MLLMS6013). If the scaled profile of MLLMS6013, which is an outlier, is excluded, phase noise above 100 MHz falls in the -120 dBc/Hz to -130 dBc/Hz range. Reasonable consensus values for SNR analysis are $L_2 = -125$ dBc/Hz above $f_{c2} = 100$ MHz for portable devices and $L_2 = -130$ dBc/Hz above $f_{c2} = 450$ MHz for wide area base-station devices. When the LO frequency is different from 140 GHz, the proposed numbers should be scaled by the $20 \log_{10}(f_{out}/f_{in})$ rule.

The phase noise profile parameters are summarized in Table 5.2-2.

Table 5.2-2: Typical RF LO Phase Noise Profile

Parameter	UE or local area BS	Medium Range or Wide Area Base Station
f_{c1}	50 kHz	50 kHz
Decay rate 1 (up to f_{c1})	-20 dB/decade	-20 dB/decade
L_1	-85 dBc/Hz	-96 dBc/Hz
f_{BW}	1 MHz	0,9 MHz
Decay rate 1 (f_{BW} to f_{c2})	-20 dB/decade	-20 dB/decade
f_{c2}	100 MHz	45 MHz
L_2	-125 dBc/Hz	-130 dBc/Hz

5.2.2 Generation of Time Domain Phase Noise Samples

5.2.2.1 Discrete Time Phase Noise Model

In the literature, a Wiener process is used to model the PN of a free-running oscillator, while a Gaussian process with a targeted PSD is used for modeling the PN of a PLL output. To generate a discrete-time PN model, the PSD profile specification is fit with a parameterized smooth function and convert that to a discrete-time process. There are several such parameterized PSD functions. Below are three representative examples:

- 1) Single-pole, single-zero of fixed (first) order PSD from IEEE 802.11 [i.48]:

$$S(f) = PSD0 \frac{1+(f/f_z)^2}{1+(f/f_p)^2} \quad (12)$$

- 2) Multi-pole, multi-zero of arbitrary order PSD from 3GPP [i.49]:

$$S(f) = PSD0 \frac{\prod_{n=1}^N 1+(\frac{f}{f_{z,n}})^{\alpha_{z,n}}}{\prod_{m=1}^M 1+(\frac{f}{f_{p,m}})^{\alpha_{p,m}}} \quad (13)$$

- 3) Sum of two AR(1) processes + flat spectrum from [i.56] (equivalent to multi-pole, multi-zero model of fixed (first) order PSD):

$$S(f) = \frac{P_1}{1+(f/f_{p,1})^2} + \frac{P_2}{1+(f/f_{p,2})^2} + P_3 \quad (14)$$

The benefit of the model in [i.49] is that the arbitrary pole/zero order is capable of fitting a complex shape of PN PSD, while the fixed order model from [i.48] and [i.49] have somewhat limited data explaining capability. On the other hand, the first order model corresponds to an AR model / IIR filter and can be easily realized through summation of AR models or discrete IIR filtered white Gaussian noise. It is therefore preferable to fix the pole/zero order if the corresponding parameterized PSD models a PN spectrum reasonably well.

As presented in Figure 5.2-2, the key elements of a PN spectrum are:

- The reference clock dominated noise: shaped with 20 dB per decade slope until the frequency corner $f_{c1} = 50$ kHz, followed by the flat part until PLL loop bandwidth $f_{BW} = 1$ MHz.
- The oscillator dominated noise which decays by 20 dB per decade until $f_{c2} = 100$ MHz.
- The LO generation path with a flat far out noise.

A first order pole-zero model with 2-pole and 2-zero (sum of two AR(1) processes and a white noise) can fit the profile of Figure 5.2-2 well enough as shown in Figure 5.2-4 where the fitting is done with the parameter set in Table 5.2-3.

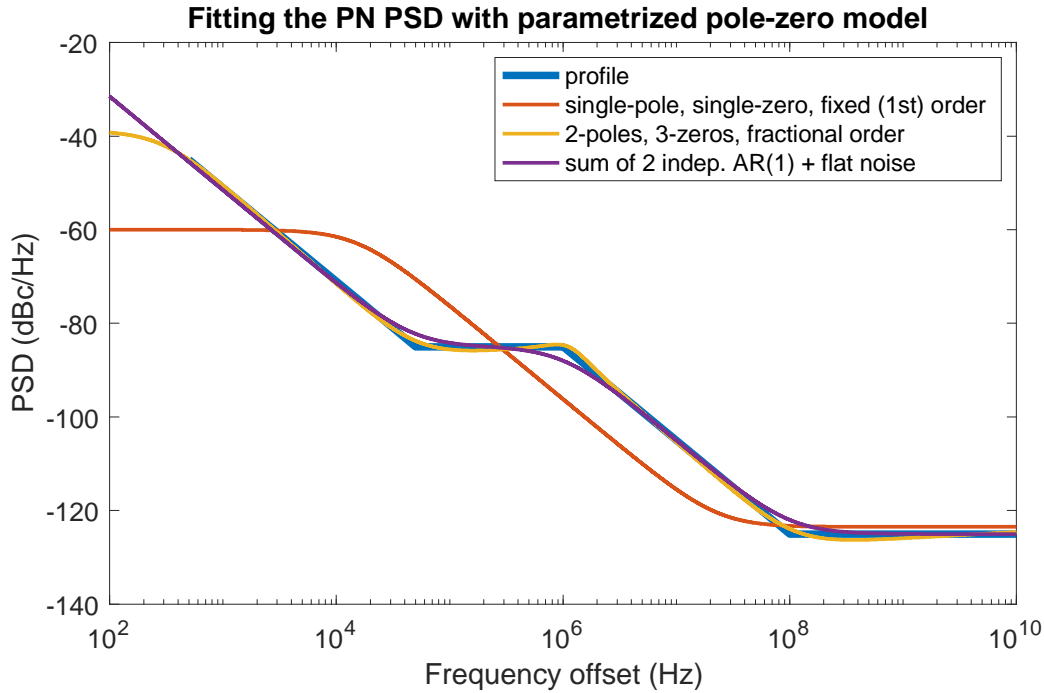


Figure 5.2-4: Fitting the 140 GHz Phase Noise profile with parameterized pole-zero model

The sum of two AR(1) processes + flat spectrum (equivalent to two-pole, one-zero models) is suitable for modeling PN PSD for the purpose of THz link-level simulation study, where the impact of the phase noise can be simulated in below three steps.

Table 5.2-3: Typical RF LO Phase Noise Profile

Parameter	Portable device
P_1	0 dBc/Hz
P_2	-85 dBc/Hz
P_3	-125 dBc/Hz
$f_{p,1}$	2,65 Hz
$f_{p,2}$	1 MHz

Step 1: Generate two AR(1) processes and a white Gaussian processes according to a baseline parameter table set, e.g. Table 5.2-3.

Step 2: Superpose the three processes in step 1 to obtain the phase processes $\underline{\phi}$ with PSD of:

$$S(f) = \frac{P_1}{1+(f/f_{p,1})^2} + \frac{P_2}{1+(f/f_{p,2})^2} + P_3 \quad (15)$$

Step 3: Apply the phase noise to the signal of interest through time-domain phasor sample-wise multiplication $e^{i\phi} \cdot \underline{s}$.

5.2.2.2 Phase Noise Power Spectral Density Sampling

The PSD $S(f)$ is initially described for a frequency value f that belongs to the continuous frequency domain. To generate Γ_k , the PSD component at the k -th frequency bin, a uniform sampling of the frequency domain is assumed.

Firstly, define F_{min} the lower bound of the frequency interval in which the PSD is observed. Secondly, define the sampling step δ such that at the frequency index (or bin) k is observed the value $S(F_{min} + k \cdot \delta)$. Thirdly, define K the number of bins to be represented, i.e. $k \in \{0, \dots, K - 1\}$, such that the upper bound of the observation interval is $F_{max} = F_{min} + (K - 1)\delta$. This also verifies that $\delta = (F_{max} - F_{min})/(K - 1)$.

5.2.2.3 Discrete PSD scaling

The sampling settings F_{min}, F_{max}, δ determine P_{tot} the total power carried by the resulting discrete PSD $\{S(F_{min} + k \cdot \delta)\}_{k \in \{0, \dots, K-1\}}$:

$$P_{tot} = \delta \sum_{k=0}^{K-1} S(F_{min} + k \cdot \delta) = \frac{F_{max} - F_{min}}{K-1} \sum_{k=0}^{K-1} S(F_{min} + k \cdot \delta) \quad (16)$$

The multiplicative factor is integrated in the PSD samples to obtain scaled PSD samples

$$\Gamma_k = S(F_{min} + k \cdot \delta) \frac{F_{max} - F_{min}}{K-1}.$$

Integrating the sampling step within the sample helps differentiate between any two sampling processes whose sampling settings are different.

5.2.2.4 Phase noise samples generation

5.2.2.4.1 Randomness inclusion

Generate a noise vector $\underline{z} = [z_0 \ z_1 \ \dots \ z_{K-1}]$ to multiply with the square root of the scaled PSD:

$$\underline{\Psi} = \sqrt{\underline{\Gamma}} \odot \underline{z} \quad (17)$$

Any k -th component z_k of the noise \underline{z} is a complex random value. The first component z_0 and the last component z_{K-1} are though constrained to be real-valued. Thus, once \underline{z} is generated, set z_0 to $\Re(z_0)$ and set z_{K-1} to $\Re(z_{K-1})$. The rationale behind this special treatment is it allows the final phase vector (see clause 5.2.2.4.2) to be real-valued. Furthermore, for any index $k \in \{0, \dots, K-1\}$, reduce z_k such that:

$$\mathbb{E}[|z_k|^2] = 1 \quad (18)$$

5.2.2.4.2 Phase samples generation

To obtain a real-valued phase vector $\underline{\phi} = [\phi_0 \ \dots \ \phi_{N-1}]$ with $N = 2(K-1)$ out of the noisy scaled PSD $\underline{\Psi}$, it is required to make $\underline{\Psi}$ a bilateral vector and to map it to the time-domain applying an inverse Fourier transform. The bilateral operation in conjunction with setting z_0 and z_{K-1} in the real domain ensures that output of the inverse Fourier transform is real. The phase vector is:

$$\underline{\phi} = \mathbf{F}_N^{-1} [\underline{\Psi}_{0:K-2} \ \text{FLIP}(\underline{\Psi}_{1:K-1}^*)], \quad (19)$$

with \mathbf{F}_N^{-1} the inverse Fourier transform of order N , $\text{FLIP}(\cdot)$ the operation that exchanges the k -th component of a K -length input vector with the $(K-1-k)$ -th component, and $(\cdot)^*$ the usual conjugate operation. It is though possible to write down these two operations under a unique operation. Indeed, compute the phase vector $\underline{\phi} = [\phi_0 \ \dots \ \phi_{N-1}]$ with $N = 2(K-1)$ such that for any index $n \in \{0, \dots, N-1\}$:

$$\phi_n = \frac{2 \Re \left(\sum_{k=0}^{K-1} \Psi_k e^{i2\pi \frac{kn}{N}} \right) - \Psi_0 z_0 - \Psi_{K-1} (-1)^n}{N} \quad (20)$$

This process does not constraint ϕ_n to belong to $]-\pi; \pi[$ as a genuine phase. However, the below operation is not impacted due to the trigonometric 2π -periodicity.

5.2.2.4.3 Phase noise samples generation

Generate the phase noise vector, also known as the phasor, as $e^{i\phi}$.

5.2.2.5 Single long generation

Instead of generating multiple vectors of phase noise $e^{i\phi}$ when generating multiple signals that could be time consuming given the above operations, it is recommended to generate a single long phase noise vector $e^{i\phi}$ whose length N is much greater than the signal length L . This way, the experimenter would randomly extract one sequence of L samples within the phase noise vector $e^{i\phi}$ for one signal.

5.2.2.6 Recommendation

In clause 5.2.2.4.1. is inserted the noise vector \underline{z} to generate some randomness in the resulting phase vector. In the state-of-art \underline{z} is usually a complex vector following a standard normal distribution (mean is zero, variance is one).

The condition on the variance of z_k in clause 5.2.2.4.1. complies with the variance value of the standard normal distribution but there are no more existing guidelines to specify how this value should be distributed over the real part of z_k and the imaginary part of z_k . Therefore, this distribution is left to the experimenter choice. In addition, the value of the mean has no mathematical justification, i.e. selecting another value than zero is not precluded. Therefore, this selection is left to the experimenter choice.

As a consequence, in order to operate a well-controlled phase noise generation, it is highly recommended that the experimenter generates phase noise samples according to the above mechanism with various settings of the parameters of the noise vector \underline{z} regarding the mean and the variance of its coordinates to observe the associated impact on the resulting phasor $e^{i\phi}$.

5.3 Data Converters and Baseband Filters

5.3.0 Introduction

Since data converters act as a "bridge" between the digital baseband and the Radio Frequency (RF) front end, the performance of data converters can be a bottleneck for the whole system. As the transmission bandwidth in THz bands can be large, the requirements on the speed of data converters increase considerably. For instance, IEEE 802.15.3d [i.71] defines several channel bandwidth configurations in the frequency range between 252,72 GHz and 321,84 GHz depending on the channel ID. In [i.71], the bandwidth can be configured to vary between the lowest bandwidth setup of 2,16 GHz, and can be increased to support a massive bandwidth of 69,12 GHz. It is further worth noting that the power consumption of data converters grows exponentially as the resolution increases. Therefore, the power/speed/precision issues for data converters should be considered [i.72]. To notify the reader on the bandwidth variability supported by the IEEE 802.15.3d [i.71], Figure 3 shows the possible bandwidth configurations that can be supported.

5.3.1 Data Converters

5.3.1.0 Introduction

Data converters are the interface between the analog real world and the digital processing realm. They are divided into Analog-to-Digital Converters (ADCs), which are employed in communication receivers to convert the received analog signal into a digital sequence for decoding and further processing, and Digital-to-Analog Converters (DACs), which are employed in transmitters to convert the digital sequence into an analog signal to be transmitted by the antenna.

Data converters play a crucial rule in communication systems that often determines the channel bandwidth, modulation order and Signal-to-Noise Ratio (SNR) of the system. Their feasibility and power consumption can be one of the bottlenecks in achieving high throughputs. This is more pronounced in the (sub-)THz communication where the wide bandwidth of up to 10 GHz to 20 GHz would require baseband data converters with sampling rates greater than 10 GS/s.

The present document describes some of the critical characterization parameters of data converters and their trends with a focus on the high-speed converter space that is capable of handling RF bandwidths greater than or equal to 10 GHz. Data converters have multiple dimensions of performance that are necessary to characterize and understand their impact on the system performance [i.50]. Those include resolution, sampling rate, noise, jitter, phase noise, distortion parameters, gain error, offset, full scale, etc. In the present document, the discussion will be limited to the fundamental and critical characterization parameters that dictate the feasibility and power of the data converter in the high-speed space.

5.3.1.1 Data Converter Performance Metrics

Data conversion is the process of converting between a continuous-time and continuous-amplitude analog signal into a discrete-time and discrete-amplitude digital sequence. As shown in Figure 5.3-1, in an ADC, the conversion includes sampling, which converts the analog signal into a discrete-time signal, and quantization, which converts the sampled signal into a discrete-amplitude signal. In a DAC, the digital input is converted to a train of pulses that are essentially a quantized sampled-and-held analog representation of the digital input, followed by a filter.

If the sampling operation happens every T_s seconds, then the sampling rate f_s is given by:

$$f_s = \frac{1}{T_s} \quad (21)$$

The sampling operation limits the maximum allowed bandwidth that can be digitized faithfully in theory to the Nyquist frequency, which is half the sampling rate. That is: the maximum recoverable bandwidth B is given by:

$$B \leq f_s/2 \quad (22)$$

In practice, over-sampling is usually required to accommodate the real anti-aliasing filters for ADCs and the sinc function roll-off and filtering in DACs, as will be shown later, which limits the practical bandwidth to values that are smaller than $f_s/2$.

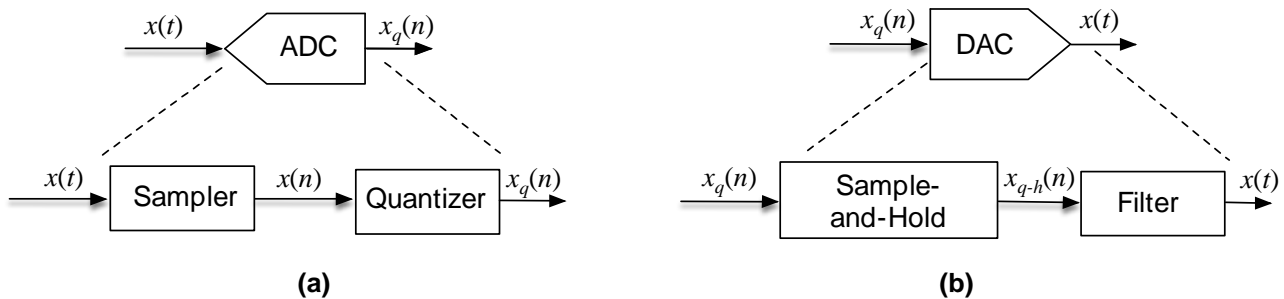


Figure 5.3-1: Simplified representation of (a) an Analog-to-Digital Converter (ADC) and (b) a Digital-to-Analog Converter (DAC)

The quantization is represented by the resolution of the converter N in bits, such that the number of quantization bins or levels (L) is given by:

$$L = 2^N \quad (23)$$

and the elementary quantization step or the least significant bit (LSB) Δ in volts is given by:

$$\Delta = \frac{V_{FS}}{2^N} \quad (24)$$

where V_{FS} is the full-scale of the converter. This is shown in Figures 5.3-2a and 5.3-2b for an ideal 4-bit ADC. Table 5.3-1 shows the relationship of LSB values and resolutions for typical ADCs. As can be seen, the number of quantization bins increases exponentially over the number of bits, and hence the value of LSB (usually represents the resolution of ADCs) decreases exponentially over the number of bits.

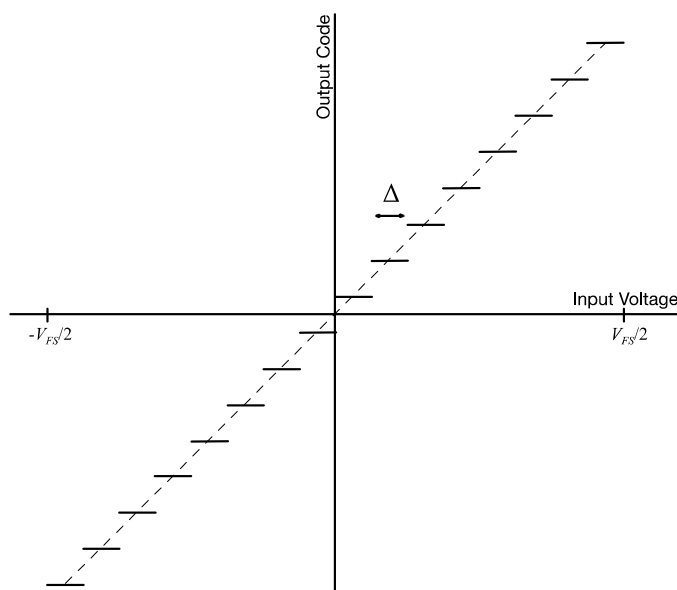


Figure 5.3-2a: Transfer characteristic of an ideal mid-rise 4-bit quantizer

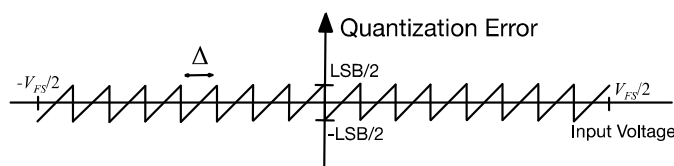


Figure 5.3-2b: Quantization error of an ideal mid-rise 4-bit quantizer

Table 5.3-1: Relationship of ADCs LSB values and ADCs resolutions

ADCs Resolution		The value of one LSB	
Number of Bits (N)	Number of Increments (2^N)	0 to 10 V Range (mV)	10 V Range (mV)
16	65 536	0,152	0,305
12	4 096	2,44	4,88
11	2 048	4,88	9,77
10	1 024	9,77	19,5
9	512	19,5	39,1
8	256	39,1	78,2

The quantization operation creates errors that are sometimes referred to as "noise", whose power is given approximately by:

$$N_Q = \frac{\Delta^2}{12} \quad (25)$$

The ratio of the signal power (or the converter full-scale) to the noise power is referred to as the converter's SNR in dB (or in dBFS if referred to the full-scale). The quantization error limits the maximum achievable signal-to-noise ratio SNR for a sinusoidal signal to:

$$SQNR(\text{in dB}) = 6N + 1,76 \quad (26)$$

Where $SQNR$ is the signal-to-quantization-noise ratio in dB. The achievable SNR for a Gaussian random signal is given by:

$$SQNR(\text{in dB}) = 6N - 1,25 \quad (27)$$

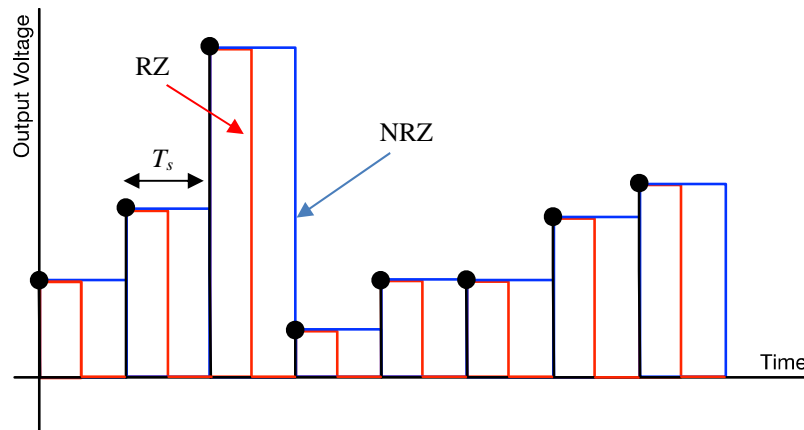


Figure 5.3-3a: DAC's operation switching modes (a) NRZ and RZ

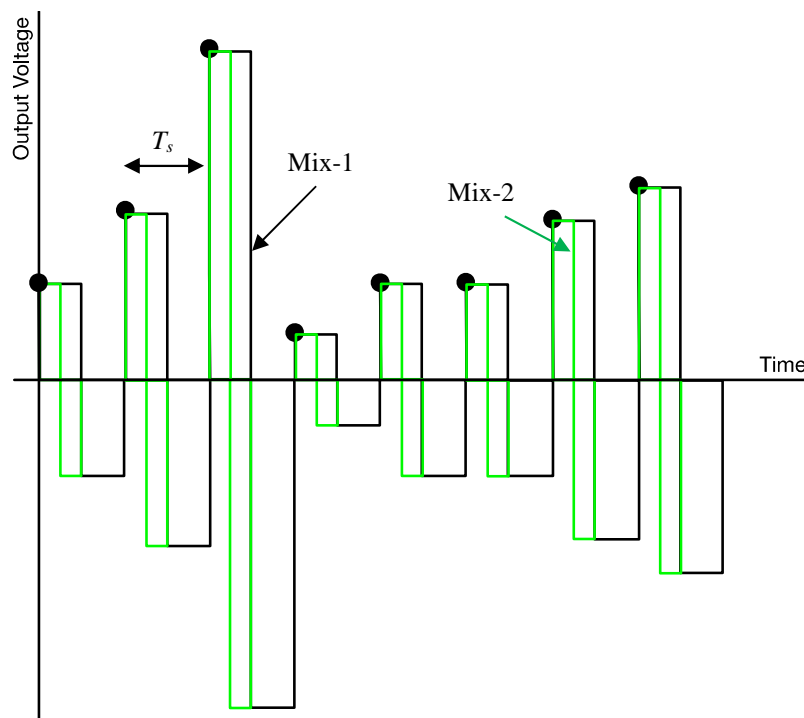


Figure 5.3-3b: DAC's operation switching modes - Two examples of mixed modes

The above fundamentals apply to DACs as well as ADCs, where for DACs the output is the analog quantity (voltage or current) and the input is the digital code. The main DAC operation is the conversion of the digital code into a stream of quantized and "held" analog pulses, which when filtered give the continuous-time and continuous-amplitude analog output signal. If the output is NRZ pulses as shown in Figure 5.3-3a in blue, the DAC output spectrum in the frequency domain will have a $\text{sinc}(f_{out}/f_s)$ response that goes to zero at frequency f_s as shown in Figure 5.3-4. This results in a reduction of the output amplitude as the frequency increases and a significant reduction in amplitude in the second and higher Nyquist zones. Alternatively, RZ pulses as shown in Figures 5.3-3a and 5.3-4 in red, goes to zero at $2f_s$, which improves the amplitude in the second Nyquist zone. Alternatively, "mixed mode" operation can be employed where the output is modulated by pulses of opposite polarity operating at f_s or higher frequencies to modulate the output and hence move some of the output energy to higher Nyquist zones. Examples are shown in Figures 5.3-3a, 5.3-3b and 5.3-4 in black and green for two different mixed modes.

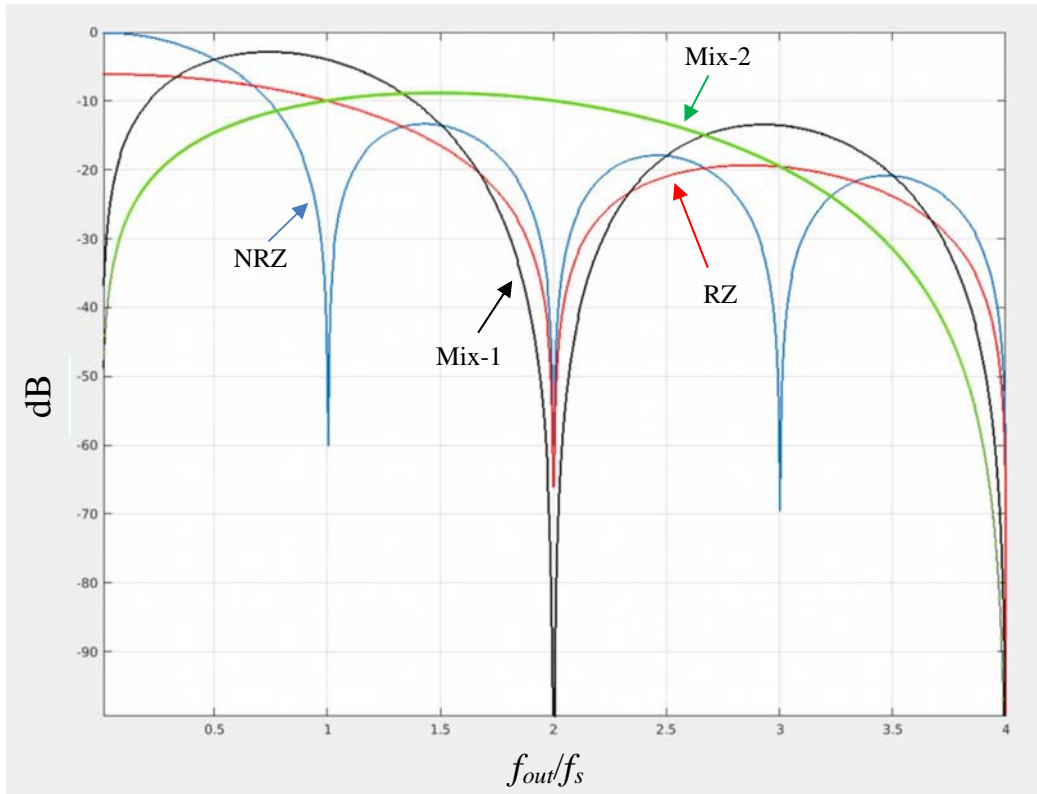


Figure 5.3-4: DAC's output spectrum in different switching modes

In practice, there are other sources of noise in addition to the quantization error. Those include thermal noise in the signal path, clock noise (jitter), coupling noise, and noise due to quantization non-idealities. These are often captured collectively by the signal-to-noise-and-distortion ratio (*SNDR* or *SINAD*), which is the ratio of the signal power (or converter full-scale power) to the total noise plus distortion power in dB or dBFS. This *SNDR* can be used to deduce the Effective Number of Bits (*ENOB*) of the converter, which is given for a sinusoidal signal by:

$$SNDR(\text{in dB}) = SINAD(\text{in dB}) = 6 \cdot ENOB + 1,76 \quad (28)$$

When including all the noise sources in the converter's Nyquist bandwidth, the *ENOB* is typically less than the resolution of the converter (*N*) because it includes all other noise and distortion contributors in addition to quantization errors.

Because of oversampling, where the band of interest is often smaller than the Nyquist bandwidth, the noise over a certain band, as opposed to the whole Nyquist bandwidth, in an ADC or a DAC is often considered. If the noise is white, the *SNDR* over a certain bandwidth *B* is given by:

$$SNDR_B(\text{in dB}) = SINAD_B(\text{in dB}) = SNDR + 10 \log\left(\frac{f_s}{2B}\right) \quad (29)$$

Similarly, the noise spectral density (*NSD*) in dB/Hz is given by:

$$NSD(\text{in dB/Hz}) = -SNDR - 10 \log\left(\frac{f_s}{2}\right) = -SNDR_B - 10 \log(B) \quad (30)$$

As shown in Figure 5.3-2b, the ADC/DAC full-scale voltage, current or power is needed to translate the *SNDR/ENOB* into noise voltage or noise power and to design the full signal chain accordingly. For the same *SNDR*, a larger full-scale implies a larger noise voltage/power.

From the above, the sampling rate of the converter f_s and the resolution *N* in bits (or the effective number of bits *ENOB* if all sources of noise and distortion are included) represent its two main metrics that are related directly to the fundamental parameters in Shannon-Hartley channel capacity formula:

$$C = B \log_2(1 + SNR) \quad (31)$$

The quantization operation is a non-linear operation that results in quantization errors that are correlated with the signal. That is: the quantization error is *not* uncorrelated additive noise but is in fact distortion. In some cases, if the thermal noise is substantially larger than the quantization noise, it tends to "dither" the non-linearity of the quantization noise and reduce the correlation between the quantization errors and the analog signal. Distortion in data converters is usually dominated by non-idealities in the sampling and quantization processes in the ADC. Similarly in the DAC, distortion tends to be dominated by non-idealities in the DAC switching circuits. However, modeling quantization error as additive uncorrelated noise can be a rough first-order and high-level useful approximation in some cases.

Distortion and coupling in data converters result in harmonics and spurs in the output spectrum. For a sinusoidal input, the distortion can be in the form of low-order harmonics, such as second- or third-order harmonics, or in the form of high-order harmonics and spurs that may or may not be related to the input frequency. This distortion is often represented by the Spurious-Free-Dynamic-Range (SFDR), which is the ratio between the signal power (or full-scale power) and the power of the highest harmonic/spur in the band of interest.

Ideal quantization results in distortion spurs at full-scale that are approximately given by the formula [i.50]:

$$SFDR(\text{in dBFS}) \sim 9N - c \quad (32)$$

Where c is a constant that ranges between 0 for low resolutions to 6 for high resolutions. However, as the signal amplitude is reduced the $SFDR$ can fluctuate and can be as bad as [i.61]

$$SFDR(\text{in dBFS}) \sim 6N \quad (33)$$

Figure 5.3-5 shows the output spectrum of a 12-bit ADC with 64 dB thermal noise, which limits the $ENOB$ to 10,4 bits. The largest spur is about -97 dB, indicating an $SFDR$ of 97 dB. Similarly, non-ideal quantization can result in spurs that are related to the magnitude of the non-ideal quantization errors. Figure 5.3-6 shows an example of an output spectrum with quantization non-idealities that limit the $SFDR$ to about 70 dB and the $SNDR$ to 56 dB, which represents a degradation of 8 dB (i.e. 1,3-bit degradation in $ENOB$) relative to the baseline.

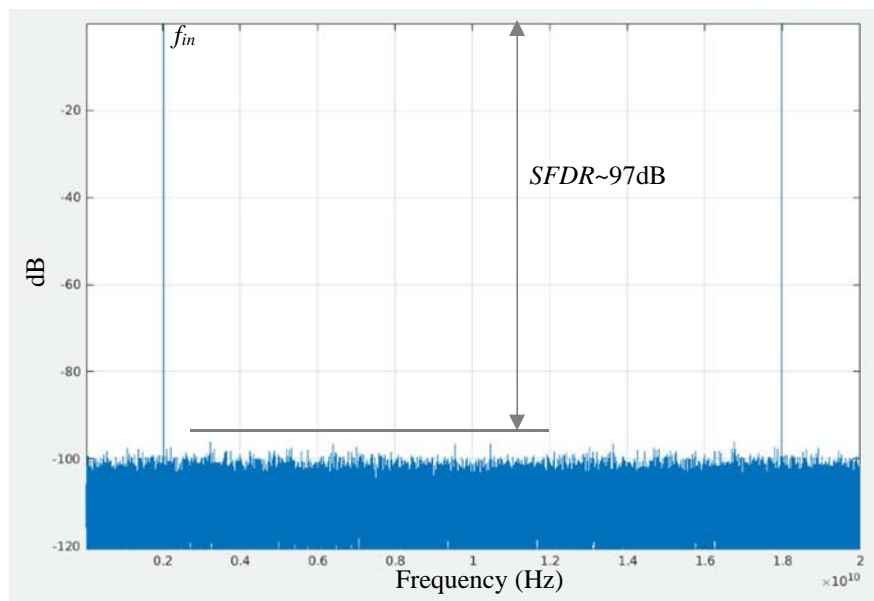
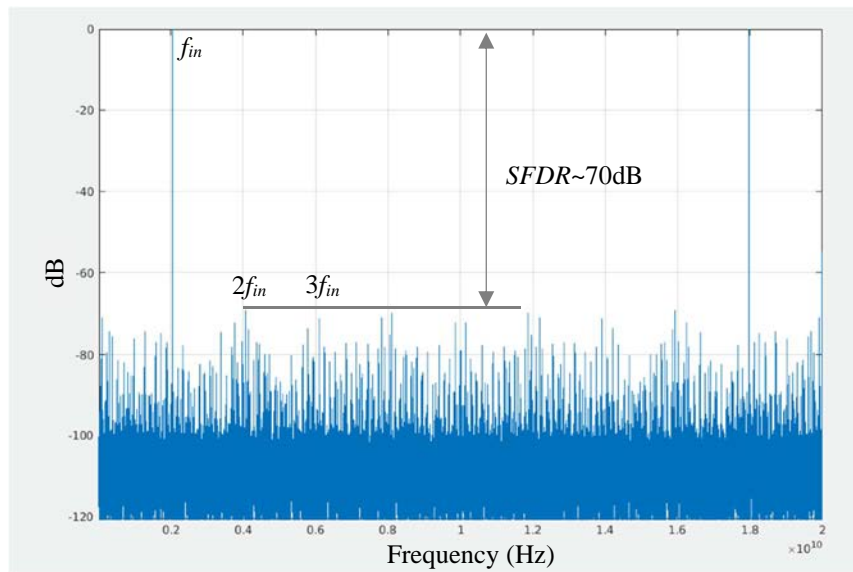


Figure 5.3-5: Output spectrum of a 12-bit ADC with 64 dB thermal noise using a single-tone input



NOTE: The *SNDR* degrades to 56 dB because of non-linear quantization non-idealities errors, which is a degradation of 1,3-bit in *ENOB*.

Figure 5.3-6: Output spectrum of a 12-bit ADC with 64 dB thermal noise and quantization non-idealities causing a large number of spurs

Figure 5.3-7 shows an example of the output spectrum that is dominated by low-order harmonics, namely second-order (HD2) and third-order (HD3) distortion at levels of about -50 dB and -60 dB, respectively. This limits the *SNDR* and *SFDR* of the ADC to about 50 dB, which is 2,3-bit degradation in *ENOB*.

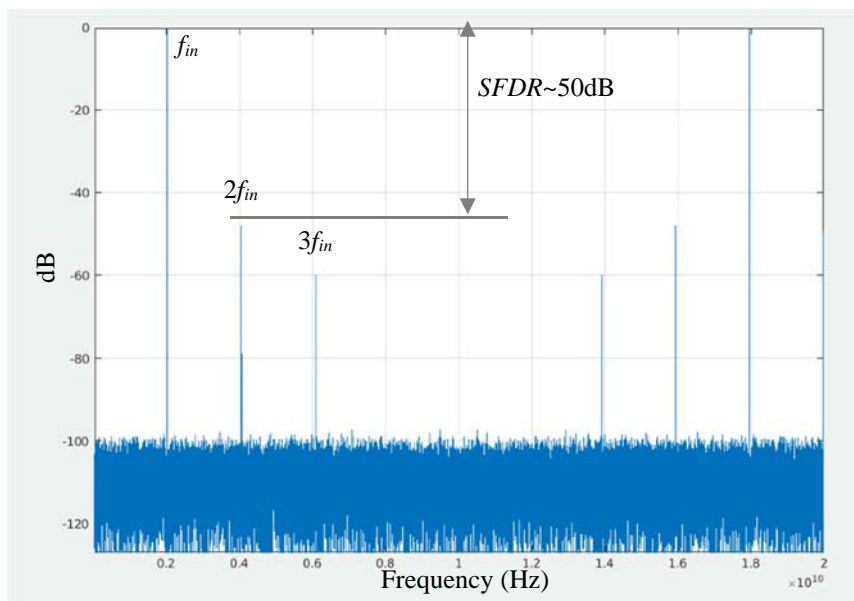


Figure 5.3-7: Output spectrum of a 12-bit ADC with 64 dB thermal noise and second- and third-order distortion

The HD2 ($2f_{in}$) and HD3 ($3f_{in}$) harmonics are shown. The *SNDR* degrades to 50 dB because of the harmonics, which is a degradation of 2,3-bit in *ENOB*.

Two-tone tests are often employed to characterize the converter's non-linearity as represented by the Inter-Modulation Distortion (IMD). These are important to characterize third order distortion as it captures the in-band distortion without the filtering limitation of the third order harmonic of single tone tests. Figure 5.3-8 shows an example output spectrum of an ADC with third-order distortion showing an $IMD3$ (or $IM3$) of about 62 dB. The third order $IMD3$ is also related to the Adjacent Channel Leakage Ratio (ACLR), which is used to characterize the effect of the adjacent channels on the desired channel. The ACLR is related to the $IMD3$ by:

$$ACLR_n = IMD3 + C_n \quad (34)$$

Where n is the number of fundamental carriers and C_n is a constant that depends on the number of carriers, which is equal to 9 dB for two carriers and 12 dB for four carriers.

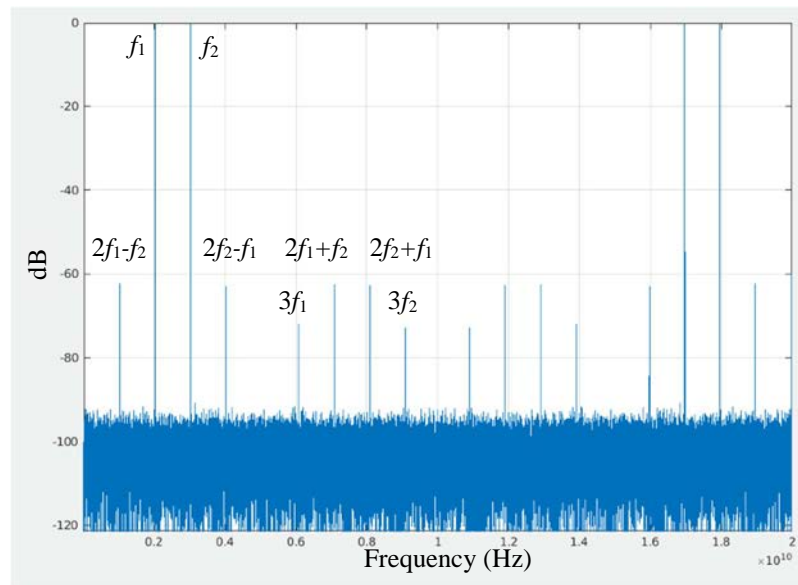


Figure 5.3-8: Output spectrum of a 12-bit ADC with 64 dB thermal noise and third-order distortion using two input tones

The $IMD3$ ($2f_1 \pm f_2$ and $2f_2 \pm f_1$) and $HD3$ ($3f_1$ and $3f_2$) components are shown.

The Nyquist-Shannon sampling theorem implies that a reliable reconstruction of a signal is possible only if the sampling rate f_s is at least two times the highest frequency of the original signal. In practice, oversampling is usually exploited to reduce quantization error, which means a sampling rate much higher than twice the signal band will be used. Specifically, oversampling and proper shaping of the quantization error spectrum can significantly reduce the power of the quantization noise in the band of interest [i.75] and [i.76]. Nevertheless, in THz communication systems, the wide transmission bandwidth leads to extremely high sampling rate, which brings challenges for data converter design. Therefore, time-interleaving scheme (e.g. as shown in Figure 5.3-9) becomes a major concern to achieve high sampling rate (tens of GS/s to hundreds of GS/s) [i.77], [i.78] and [i.79]. If the speed of the converter is higher than what is achievable using a single core, multiple cores are usually interleaved in the time domain to achieve a net sampling rate that is equal to the sampling rate of each multiplied by the number of interleaved converters. Ideally, this increase in the sampling rate is achieved without sacrificing performance. An example is shown conceptually in Figure 5.3-9 where four ADCs, each operating at $f_s/4$, are time-interleaved to obtain a faster ADC operating at a sampling rate of f_s . The simplified timing diagram of this 4-way interleaving is shown in Figure 5.3-10.

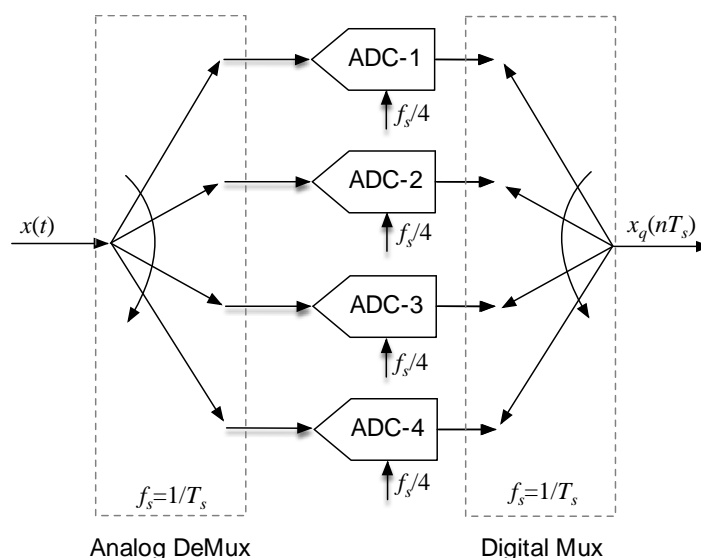


Figure 5.3-9: A representation of a 4-way interleaved ADC

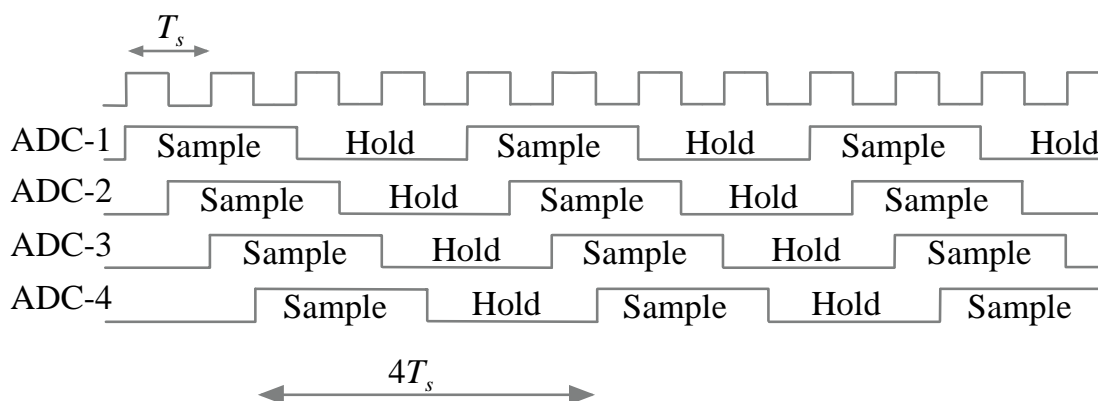


Figure 5.3-10: Simplified timing diagram of a 4-way interleaved ADC

However, in practice, the mismatch between the individual converters results in spurs that are often referred to as interleaving spurs. For example, offset mismatch results in additive spurs at fixed locations that are independent of the input signal and are located at:

$$f_{IL} = \frac{kf_s}{M} \quad (35)$$

Where k is an integer given by $1, 2, \dots, M-1$. M is the number of interleaved cores, and f_s is the interleaved sample rate. For example, interleaving 4 ADCs would result in 3 offset mismatch spurs and $f_s/4$, $f_s/2$ and $3f_s/4$. In a single side band representation, this results in two spurs and $f_s/4$ and $f_s/2$.

If there is gain, timing, or bandwidth mismatch, the spurs result from an amplitude or phase modulation of the signal, which results in spurs at frequencies of:

$$f_{IL} = \pm f_{in} + \frac{kf_s}{M} \quad (36)$$

It is interesting to note that the spur-free bandwidth is equal to $f_s/2M$. That is, the spur-free bandwidth is equal to the Nyquist band of a single non-interleaved core. Table 5.3-2 summarizes the cause, behaviour and location of the interleaving spurs and Figure 5.3-11 shows an output spectrum of a 4-way interleaved ADC with offset and gain/timing mismatch spurs.

From the above discussion, the *SNDR/ENOB* and sampling rate are the two main parameters of data converters that are required for system design at a high level. However, it is often important to understand the distortion/spur behaviour as well. Over a certain band, the *SNDR* can vary significantly depending on whether large harmonics or spurs fall in band or not. Therefore, the representation of the data converter in terms of bits and sampling rate or in terms of additive noise may not be adequate, and in some cases other parameters such as *IMD* and *SFDR* need to be included.

Table 5.3-2: Effect of mismatch in interleaved converters

Mismatch type	Impact on input	Resulting spur location in the spectrum
Offset mismatch	Additive effect, independent of input	$f_{IL} = \frac{k f_s}{M}$
Gain mismatch	Amplitude modulation	$f_{IL} = \pm f_{in} + \frac{k f_s}{M}$
Timing mismatch	Phase modulation	$f_{IL} = \pm f_{in} + \frac{k f_s}{M}$
Bandwidth mismatch	Amplitude and phase modulation	$f_{IL} = \pm f_{in} + \frac{k f_s}{M}$

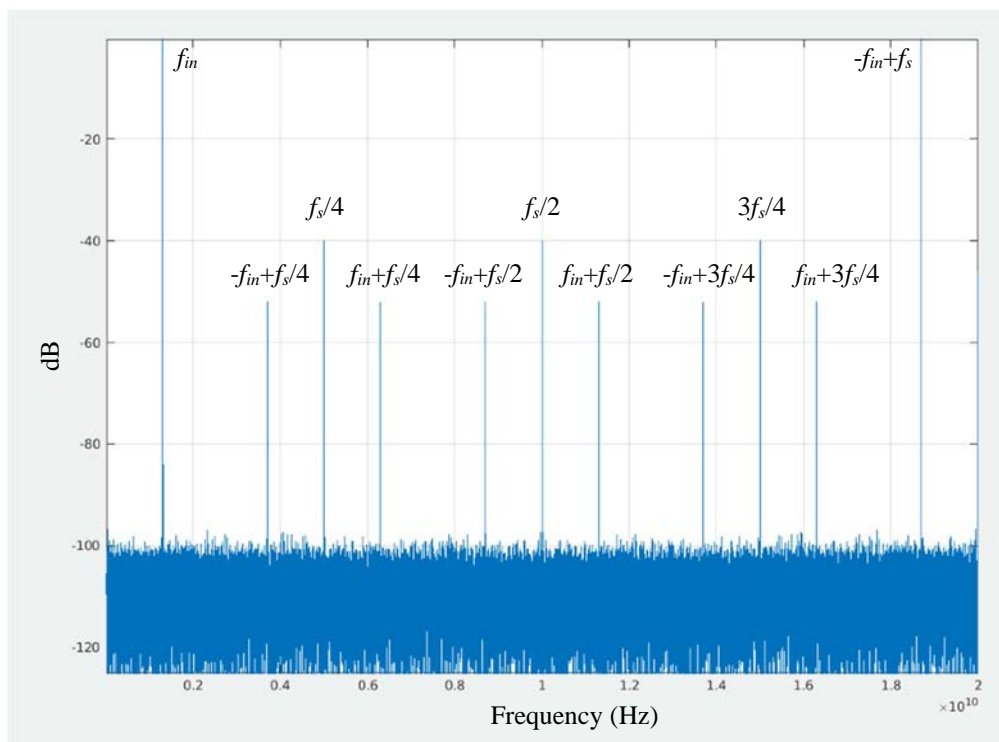


Figure 5.3-11: Output spectrum of a 4-way interleaved 12-bit ADC with 64 dB thermal noise and channel mismatch

The spectrum shows offset and gain/timing mismatch spurs. The spurs represent a degradation of 4 bits in overall ENOB. However, there is a spur-clean bandwidth of 2,5 GHz around the fundamental regardless of its location.

The above characterization parameters mostly apply to both ADCs and DACs. However, one main difference is that for DACs, it is less common to represent its performance using *ENOBs* or *SNDR* because of the analog nature of its output and the possible spreading of the noise over multiple Nyquist zones. Instead, the noise is usually represented as Noise Spectral Density (*NSD*) in dBFS/Hz within the band of interest. Similarly, analogous to the full-scale voltage of the ADC, DACs are usually characterized by their output full-scale power in dBm.

A general model that can capture the different ADC non-idealities is shown in Figure 5.3-12, which illustrates an ADC composed of M -interleaved cores, each has a non-linear function, a sampler, and a quantizer. The interleaving offset, gain and timing mismatches are incorporated in the sampler. The clock jitter can be incorporated as additive noise in the sampling clock of the sampler. The thermal noise is added to the signal before the quantizer. The quantizer can incorporate the quantization non-idealities as well, if needed. The DAC's model can be a similar model where the signal flow is from right (digital) to left (analog) as shown in Figure 5.3-13. Since the digital sequence is already quantized, the DAC's "Quantizer" block can be used to model the analog full-scale and the quantization non-idealities, if needed. The S/H (Sample-and-Hold) block models the analog pulse generation and, combined with the Analog Mux at the output, can be used to model an NRZ, RZ or any other preferred switching mode as shown before in Figures 5.3-2a and 5.3-2b.

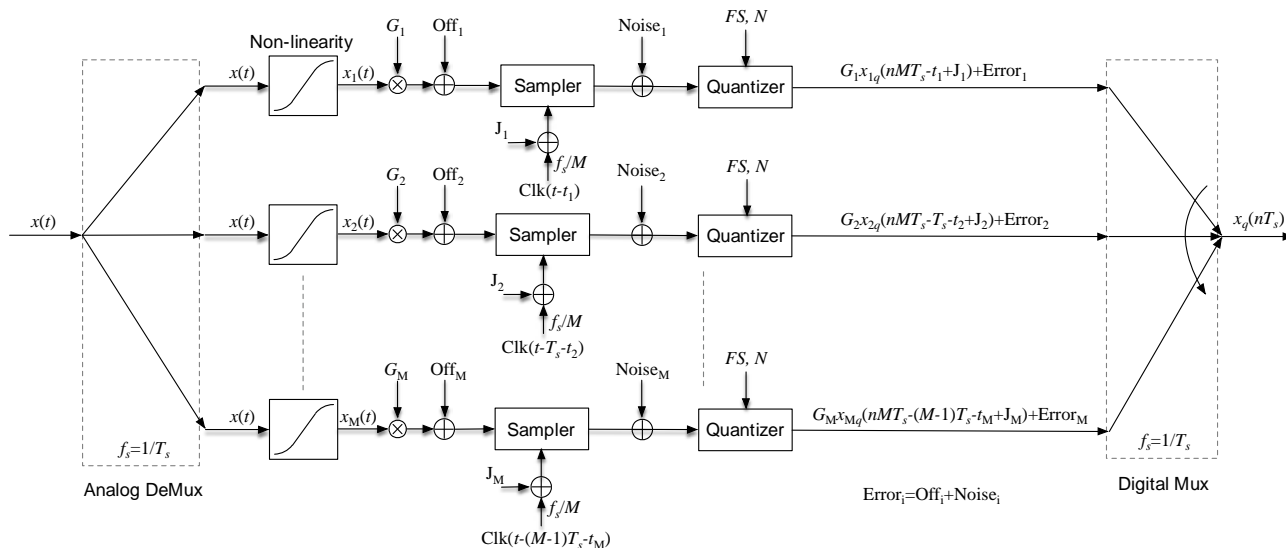


Figure 5.3-12: Simplified representation of a general model that captures the ADC's non-linearity, interleaving errors and quantization

The ADC's sampling rate is f_s and is composed of M time-interleaved channels each sampling at f_s/M . The signal x_{iq} is the quantized digital output signal of the i th ADC channel. The parameters Off_i , G_i and t_i are the offset, gain and timing errors of the i th channel, respectively. $Error_i$ is the additive error term, $Noise_i$ is the additive thermal noise, and J_i is the random jitter on the sampling clock of the i th channel. The parameters FS and N in the quantizer are the full-scale and resolution (or quantization accuracy), respectively.

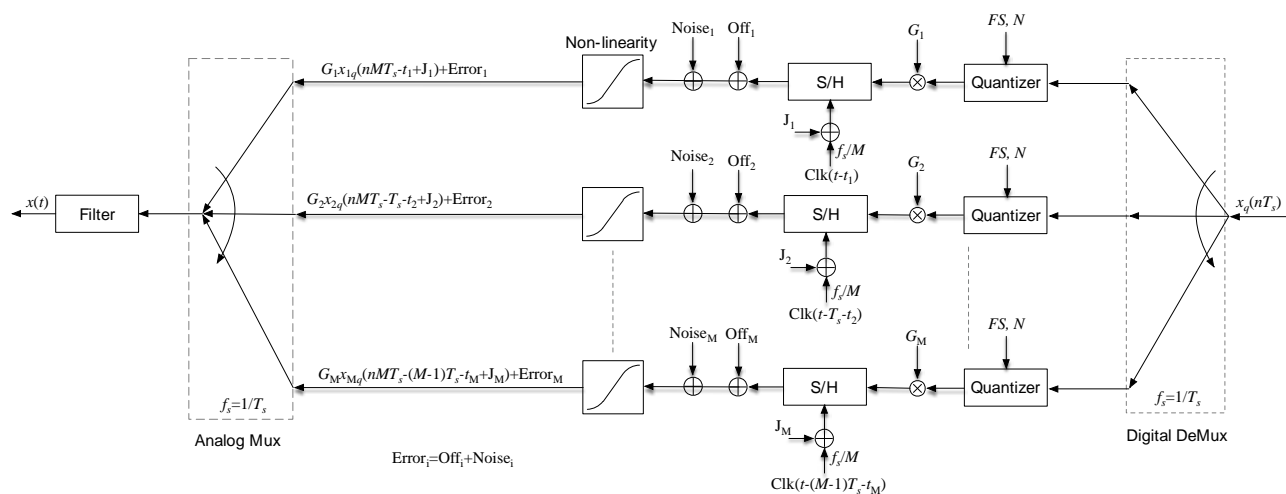


Figure 5.3-13: Simplified representation of a general model that captures the DAC's non-linearity, interleaving errors and quantization errors

The S/H is the sample-and-hold block. The DAC's sampling rate is f_s and is composed of M time-interleaved channels each sampling at f_s/M . The signal $x_{i,q-h}$ is the quantized-and-held output signal of the i th DAC channel. The parameters Off_i , G_i and t_i are the offset, gain and timing errors of the i th channel, respectively. $Error_i$ is the additive error term, $Noise_i$ is the additive thermal noise, and J_i is the random jitter on the sampling clock of the i th channel. The "Quantizer" is used to model the full-scale and quantization non-idealities, where the parameters FS and N are the full-scale and resolution (or quantization accuracy), respectively.

5.3.1.2 Performance Trends

In spite of the multi-dimensional nature of the converter performance, it is desirable to normalize that performance into a metric that represents the efficiency of the converter for its performance and captures the performance/speed/power trade-off with reasonably accuracy. This normalized performance is referred to as Figure of Merit (FOM). A commonly used FOM was first proposed by Walden in [i.51] and is given by:

$$FOM_W(\text{in J/conv. step}) = \frac{\text{Power}}{2^{ENOB} \cdot f_s} \quad (37)$$

The Walden FOM_W assumes the power increases linearly with sampling rate and exponentially with the effective number of bits. A smaller FOM_W indicates a more efficient ADC. Another FOM that is suitable for noise-limited converters was proposed by Schreier in [i.52], and is given by:

$$FOM_S(\text{in dB}) = DR + 10 \log_{10} \left(\frac{BW}{\text{Power}} \right) \quad (38)$$

Where DR is the dynamic range defined as the input range from full-scale to where the SNR reduces to 0 dB. This is typically a measure of the SNR in the absence of a signal excluding large signal effects, jitter, and non-linearity. BW is the bandwidth of the ADC where the DR holds. A larger FOM_S indicates a more efficient ADC.

A modification of the Schreier FOM was proposed by Ali in [i.53] to generalize the Schreier FOM_S to capture the distortion, jitter, high-frequency impairments and large-signal effects [i.54]. This modified Schreier FOM_{S_HF} is given by [i.53] and [i.54]:

$$FOM_{S_HF}(\text{in dB}) = SNDR + 10 \log_{10} \left(\frac{f_s/2}{\text{Power}} \right) \quad (39)$$

Where the $SNDR$ is the high frequency $SNDR$ that captures large signal, distortion and jitter effects. The parameter f_s represents sampling rate in Nyquist converters. For Delta-Sigma and other noise-shaped converters, f_s is the effective sampling rate, which is double the bandwidth over which the $SNDR$ holds [i.53]. A larger FOM_{S_HF} indicates a more efficient ADC.

The Walden and the modified Schreier FOM 's described in equations (37) and (39) are widely used to compare the efficiency and performance of data converters in [i.54] and [i.55]. From the figures shown in the Murmann survey [i.55] some trends are observed:

- As the sampling rate increases, converters tend to be less efficient. That is: the FOM is not fixed and tends to degrade with increasing the speed for sampling rates above 100 MHz. This is an important consideration when attempting to extrapolate power and performance at different sampling rates. This speed penalty is in the order of 10 dB/decade in the modified Schreier FOM_{S_HF} . For the Walden FOM_W , the trend is similar although the slope is less than 10 dB/decade. It indicates that the power of the converter at high speeds increases in a super-linear fashion with sampling rate, and the rate of increase tends to be to the power of 1.5 - 2x of the sampling rate. This is partially because of jitter and partially due to the technology limits of pushing the speed higher.
- The Walden FOM_W is more appropriate to use at the high speeds and relatively low resolutions, where the converters' efficiency tend to be less noise-limited and more speed-limited. The modified Schreier FOM_{S_HF} is more appropriate with relatively high-resolution converters at both low and high speeds.
- In 2015, the FOM in the high-speed region was reported to improve by a factor of approximately 2 every about 2 years. That is: the state-of-the-art high-speed front moves to the right by an octave every about 2 years [i.54]. The more recent trend shows about 10x-30x improvement over the 10 years from 2012 to 2022 [i.55]. This trend may slow down in the future because of the slowing-down of Moore's law.

- Data converters with resolutions in the order of 4 bits to 6 bits and sampling rates in the 10 GS/s to 50 GS/s range consume power in the order of 50 mW to 100 mW with a Walden FOM_W of 40 fJ/step to 60 fJ/step [i.56], [i.57], [i.58], [i.59] and [i.60] and a modified Schreier $FOM_{S_{HF}}$ of 146 dB to 148 dB. Higher resolutions are achieved in the 10 GS/s to 24 GS/s range for higher power. For example, 7 bit to 8 bit of performance consumes power in the range of 0,6 W to 1,5 W with a Walden FOM_W of about 180 fJ/step to 350 fJ/step and a Schreier $FOM_{S_{HF}}$ of 146 dB to 148,5 dB [i.61], [i.62] and [i.63].
- It is interesting to note the substantial degradation in efficiency according to the Walden FOM_W with increasing resolution/accuracy at the same sampling rate. The modified Schreier $FOM_{S_{HF}}$ does not show such degradation because of its better accuracy in capturing the efficiency of noise-limited converters. This is another indicator of the risk of extrapolating power estimates from one data point to another at a different resolution or sampling rate using one FOM .
- In practical applications, power dissipation of data converters is equally (or often more) important as the sampling rate and resolution. With the state-of-the-art Integrated Circuits (ICs) fabrication techniques, it is difficult for data converters to support high precision, high sampling rate and low power consumption simultaneously [i.73] and [i.74].

Unlike ADCs, there is no FOM that is agreed upon to compare the efficiency of DACs. In addition to sampling rate and noise, the $IMD3$ and $SFDR$ are the most important parameters used to characterize DACs as well. A survey of DAC performance is given in [i.64] up to 2020. Some data points after 2020 are given in [i.65], [i.66] and [i.68]. Examples of the state-of-the-art of high-speed DACs in the 10 GHz to 20 GHz range with resolutions in the 12 bits to 14 bits are given in [i.65], [i.66] and [i.67] whose power consumption is in the range of 170 mW to 550 mW. The performance is often limited by distortion components that tend to be in the 9 bit to 11-bit range. For lower resolutions, performance in the 4-6-bit range could be achieved for power consumption in the range of 40 mW to 100 mW [i.57], [i.68], [i.69] and [i.70].

5.4 Beam Squint

5.4.1 Beam Squinting Effect at THz bands

Large antenna array and wide channel bandwidth are two characteristics of the communications over THz. Consider a practical and low-cost analog beamforming architecture with one Radio Frequency (RF) chain and a phased array employing phase shifters, as shown in Figure 5.4-1.

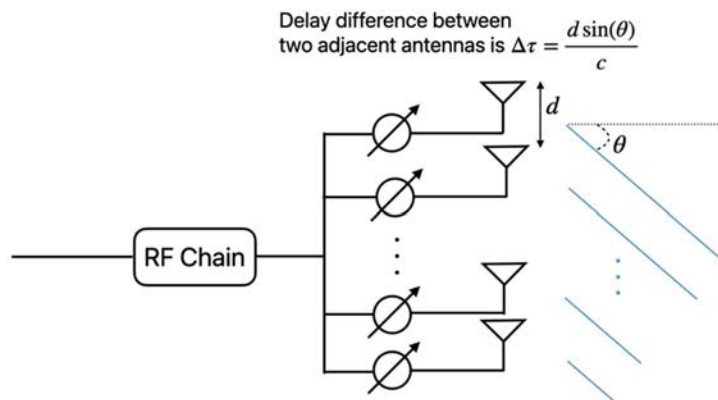


Figure 5.4-1: Analog beamforming architecture with phase shifters

The relative channel response of the n -th antenna with respect to the first antenna is:

$$s_n = e^{-j2\pi d(n-1)\frac{\sin\theta}{\lambda}}, \quad (40)$$

where θ is the angle of the transmitted signal, d is antenna spacing, and λ is the wavelength corresponding to frequency f .

In phase shifter based analog beamforming architecture, the phase shifter designed for carrier frequency f_c is configured as:

$$\varphi_n = 2\pi d(n-1) \frac{\sin \theta}{\lambda_c} \quad (41)$$

for n -th antenna where λ_c is the wavelength corresponding to carrier frequency f_c .

This works well for narrowband signals. For wideband signal, however, it may become problematic. More specifically, the set of phase shifters $\{\varphi_n\}$ designed based on f_c cannot completely compensate for the phase difference at another frequency f where $f \neq f_c$. This leads to the beam squinting phenomenon, as illustrated in Figure 5.4-2.

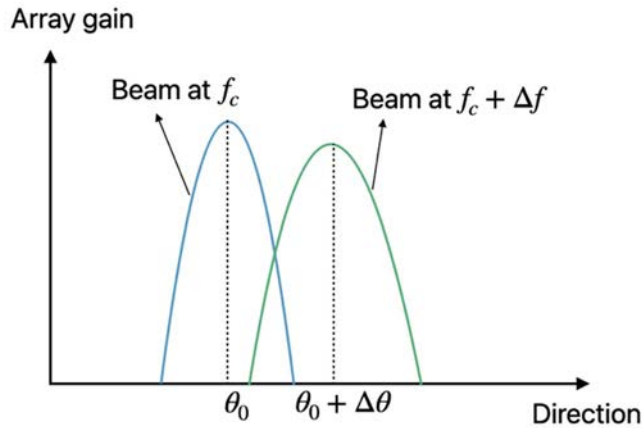


Figure 5.4-2: Illustration of beam squinting

5.4.2 Theoretical Analysis of Beam Squinting

In the following, the beam squinting effects of a Uniform Planar Array (UPA) are theoretically analysed. As shown in Figure 5.4-3, a UPA is deployed at x - z plane and assumed to have $N_h \times N_v$ antennas, where N_h is the number of antennas in the horizontal direction and N_v is the number of antennas in the vertical direction. The distance between two adjacent antennas in horizontal/vertical direction is d . Also, ϕ and θ are used to denote the azimuth Angle of Departure (AoD) and elevation AoD, respectively.

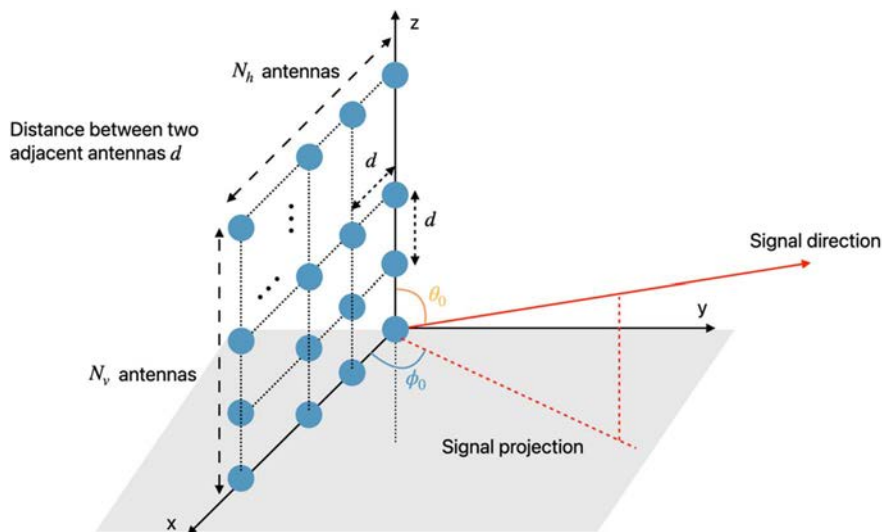


Figure 5.4-3: UPA modeling

Assume:

- line-of-sight transmitter to receiver link;

- far field channel modeling;
- individual antenna element response $u(\phi, \theta)$ is independent of frequency and is the same for all the $N_h \times N_v$ antennas;
- antenna efficiency β is independent of frequency and is the same for all the $N_h \times N_v$ antennas.

Then the channel response $h(f)$ at frequency f for AoD $\{\phi, \theta\}$ is expressed as:

$$h(f) = \gamma(f) e^{-j2\pi f \tau} \frac{1}{\sqrt{N_h N_v}} \sum_{n=1}^{N_h} \sum_{m=1}^{N_v} e^{j\varphi_{m,n}} e^{-j2\pi f \left(\frac{d}{c}\right) \{(n-1) \cos \phi \sin \theta + (m-1) \cos \theta\}} \quad (42)$$

where:

- γ represents path loss α , combined with antenna element response u and antenna efficiency β , i.e. $\gamma(f) = \alpha(f)u\beta$.
- τ is the transmission delay from the first antenna element.
- $\varphi_{m,n}$ is the phase shifter of the (m, n) -th antenna element.

To maximize $|h(f)|^2$ for a targeting AoD $\{\phi_0, \theta_0\}$ and center frequency f_c , the phase shifter $\varphi_{m,n}$ should be configured as:

$$\varphi_{m,n} = 2\pi f_c \left(\frac{d}{c}\right) \{(n-1) \cos \phi_0 \sin \theta_0 + (m-1) \cos \theta_0\} \quad (43)$$

Then the channel response $h(f)$ at frequency f for an arbitrary AoD $\{\phi, \theta\}$ becomes:

$$h(f) = \gamma(f) e^{-j2\pi f \tau} \frac{1}{\sqrt{N_h N_v}} \sum_{n=1}^{N_h} \sum_{m=1}^{N_v} e^{j2\pi f_c \left(\frac{d}{c}\right) \{(n-1) \cos \phi_0 \sin \theta_0 + (m-1) \cos \theta_0\}} e^{-j2\pi f \left(\frac{d}{c}\right) \{(n-1) \cos \phi \sin \theta + (m-1) \cos \theta\}} \quad (44)$$

By defining array gain as $|h(f)|^2$ with $\gamma(f) = 1$, i.e. isotropic antenna element with no efficiency loss, and assuming $d = 0,5\lambda_c$:

$$\begin{aligned} |h(f)|^2 &= \frac{1}{N_h N_v} \left| \sum_{n=1}^{N_h} e^{j\pi(n-1) \left(\cos \phi_0 \sin \theta_0 - \frac{f}{f_c} \cos \phi \sin \theta\right)} \sum_{m=1}^{N_v} e^{j\pi(m-1) \left(\cos \theta_0 - \frac{f}{f_c} \cos \theta\right)} \right|^2 \\ &= \left| \frac{\sin\left(\frac{N_h \pi x}{2}\right)}{\sqrt{N_h} \sin\left(\frac{\pi x}{2}\right)} e^{j\frac{(N_h-1)\pi x}{2}} \right|^2 \times \left| \frac{\sin\left(\frac{N_v \pi y}{2}\right)}{\sqrt{N_v} \sin\left(\frac{\pi y}{2}\right)} e^{j\frac{(N_v-1)\pi y}{2}} \right|^2 \\ &= \left| \sqrt{N_h N_v} \times \frac{\sin\left(\frac{N_h \pi x}{2}\right)}{N_h \sin\left(\frac{\pi x}{2}\right)} \times \frac{\sin\left(\frac{N_v \pi y}{2}\right)}{N_v \sin\left(\frac{\pi y}{2}\right)} \right|^2 \end{aligned} \quad (45)$$

where $x = \cos \phi_0 \sin \theta_0 - \frac{f}{f_c} \cos \phi \sin \theta$ and $y = \cos \theta_0 - \frac{f}{f_c} \cos \theta$, i.e. $|h(f)|$ is the multiplication of two periodic sinc functions (also called Dirichlet function) and a factor $\sqrt{N_h N_v}$. Then, for a given frequency f , by maximizing $|h(f)|^2$ the $\{\hat{\phi}(f), \hat{\theta}(f)\}$ that yield the largest array gain can be obtained.

Beam squinting phenomenon is verified by equation (45), i.e.:

- the beams can be steered to different directions for different frequencies, which deviate from the target direction;
- from the perspective of a target direction, the array gain varies across frequencies.

Next, numerical evaluations of beam squinting are provided.

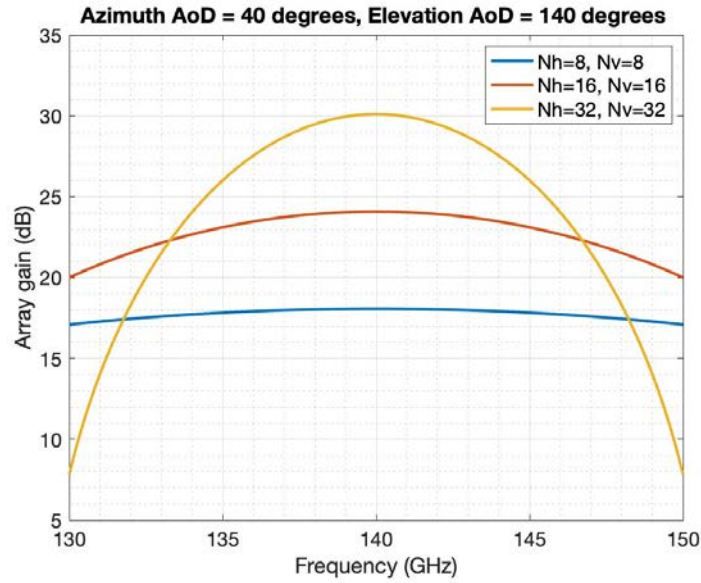
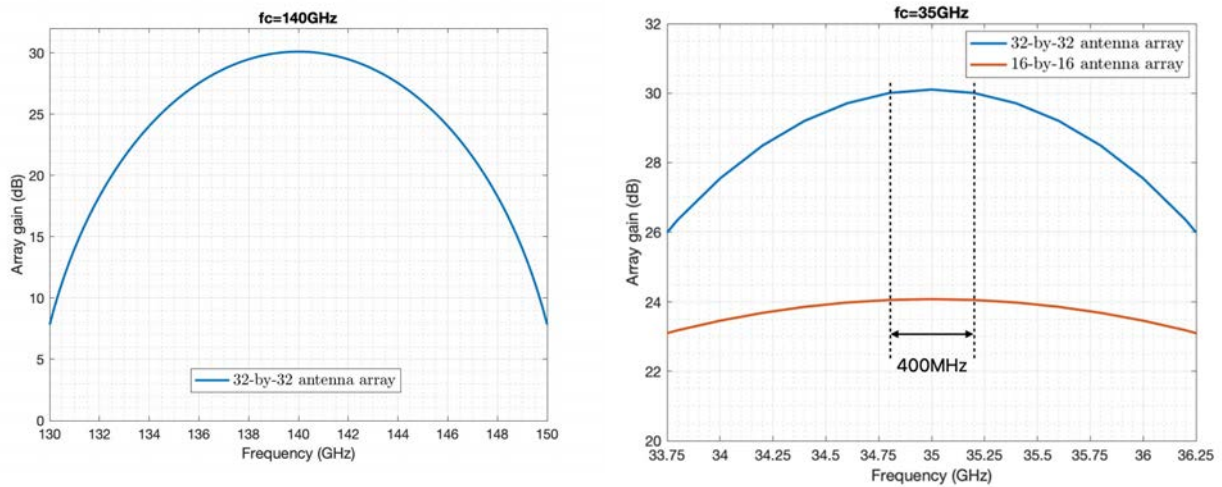


Figure 5.4-4: Array gain comparison of different antenna array sizes

Figure 5.4-4 shows the array gain variation over frequencies for different antenna array sizes, which assumes the target AoD $\{\phi_0 = 40, \theta_0 = 140\}$ and carrier frequency $f_c = 140$ GHz. Due to beam squinting, the array gain varies over the frequency ranges [130 GHz, 150 GHz], where the peak is achieved at 140 GHz. As shown, a large array leads to more severe beam squinting, e.g. significant gain degradation across frequencies.



(a): $f_c = 140$ GHz

(b): $f_c = 35$ GHz

Figure 5.4-5: Comparison of array gain variation for different carrier frequencies and antenna sizes

Figure 5.4-5 shows array gain variation across frequencies for different carrier frequencies and antenna sizes, assuming the target AoD $\{\phi_0 = 40, \theta_0 = 140\}$ and the considered AoD $\{\phi = 40, \theta = 140\}$. There are several observations from Figure 5.4-5:

- First, for a considered antenna dimension, e.g. 32-by-32 array, the array gain drops roughly by 4 dB (30 dB to 26 dB) from centre frequency 140 GHz to frequency $140 + 5 = 145$ GHz for $f_c = 140$ GHz; and by 4 dB from centre frequency 35 GHz to frequency $35 + 1,25 = 36,25$ GHz for $f_c = 35$ GHz. Here 1,25 GHz is considered from fractional bandwidth perspective. Hence, for a fixed antenna dimension and the same fractional frequency offset from centre frequency, beam squinting is comparable between lower carrier frequency and higher frequency.

- Nevertheless, the available bandwidth is typically different for higher and lower frequencies. For example, for 35 GHz which belongs to FR2, the NR available channel bandwidth is up to 400 MHz.; while for THz 140 GHz the bandwidth can be much larger, e.g. 12,5 GHz [i.80]. For a bandwidth of 400 MHz in Figure 5.4-5(b) with $f_c = 35$ GHz, the array gain drop is almost negligible from 35 GHz to $35 \pm 0,2$ GHz for both 32-by-32 and 16-by-16 antenna arrays.
- Moreover, due to different wavelength of different frequency, the actual physical array size is different for the same antenna dimension. From practical perspective, it is more reasonable to compare different frequencies when fixing the physical antenna size. More specifically, a 32-by-32 antenna array at $f_c = 140$ GHz with 16-by-16 antenna array at $f_c = 35$ GHz is compared, as they have the same physical size when assuming the half wavelength antenna distance. Due to the smaller dimension, the beam squinting effect for 16-by-16 antenna array at $f_c = 35$ GHz is even more negligible for a bandwidth of 400 MHz as illustrated in Figure 5.4-5(b).

Therefore, if practical channel bandwidth and antenna array size are considered, the effects of beam squinting are more significant for higher carrier frequency compared to lower carrier frequency.

Figures 5.4-6 to 5.4-10 illustrate the array gain variation over frequencies and azimuth/elevation AoDs for different target AoDs, assuming a 32-by-32 antenna array and $f_c = 140$ GHz. As shown, how array gain is spread over azimuth/elevation AoDs and how the gain varies across frequencies for a given azimuth/elevation AoD largely depends on the target AoD. For example, it is seen that the array gain variation over frequencies is much smaller in Figure 5.4-7(a) compared to Figure 5.4-8(a).

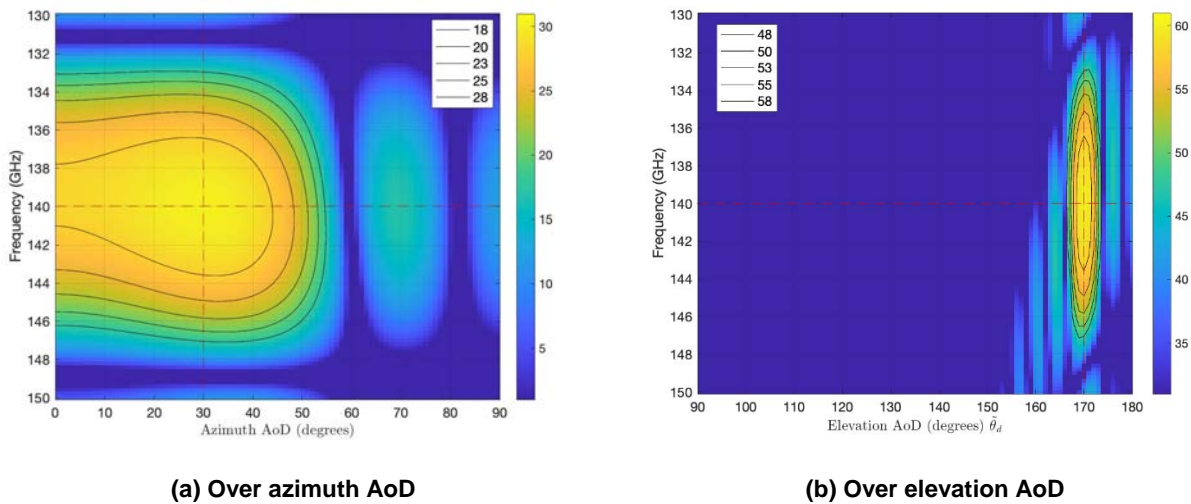


Figure 5.4-6: Array gain variation for target AoD $\{\phi_0 = 30, \theta_0 = 170\}$

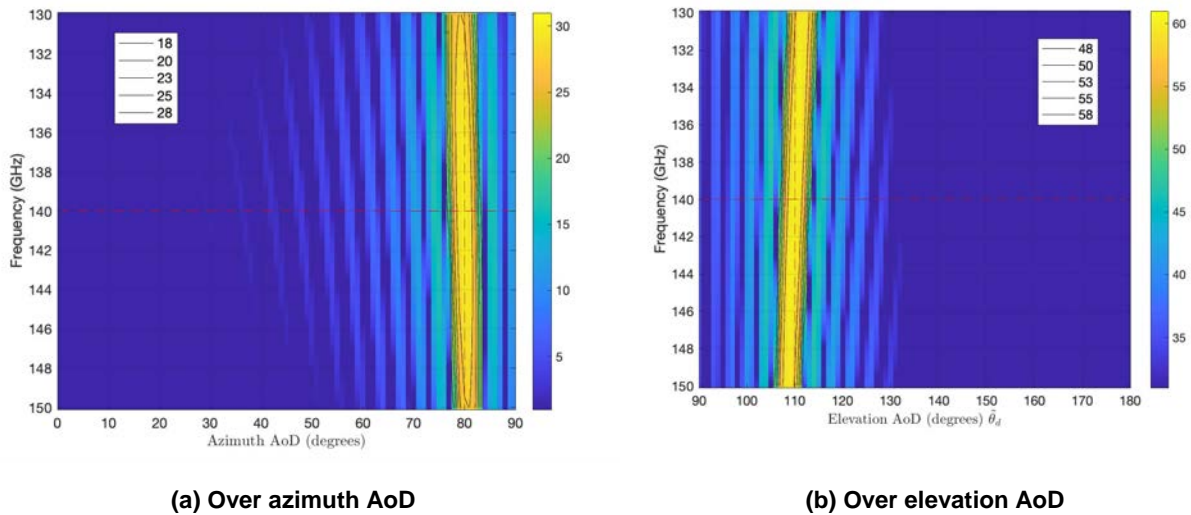


Figure 5.4-7: Array gain variation for target AoD $\{\phi_0 = 80, \theta_0 = 110\}$

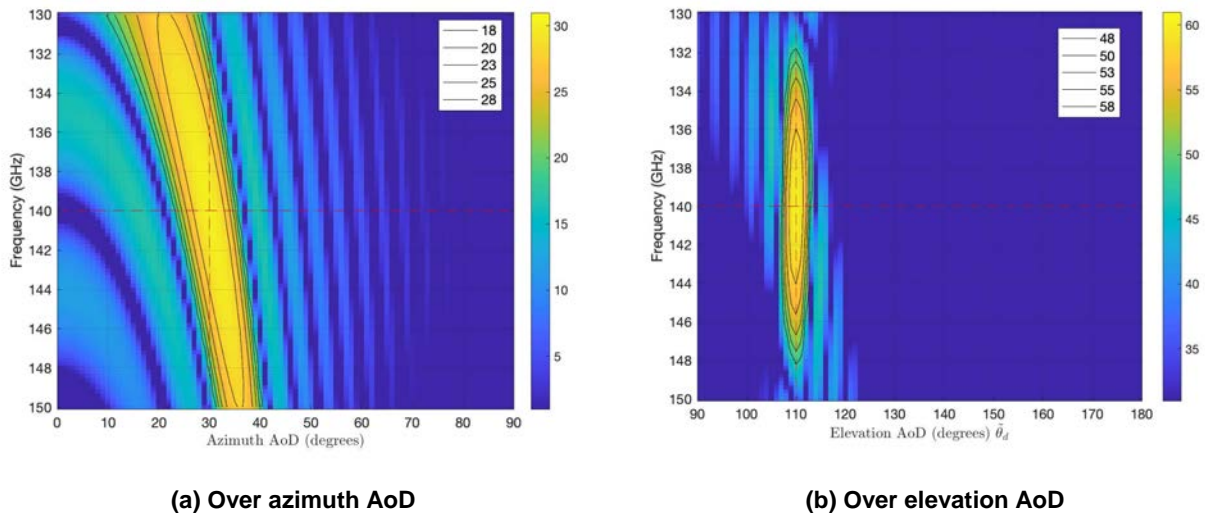


Figure 5.4-8: Array gain variation for target AoD $\{\phi_0 = 30, \theta_0 = 110\}$

Based on the above analysis, the beam squinting effects can be quite detrimental in some scenarios, especially for THz communication which potentially has large antenna array and wide channel bandwidth. Hence, practical beam squinting elimination or reduction techniques should be studied for THz.

5.4.3 Beam Squinting Handling

To eliminate beam squinting, True Time Delay (TTD) has been proposed [i.81] and [i.82]. The underlying principle of TTD is that, instead of the approximate compensation of delay difference across antennas using phase shifters, TTD can directly compensate for the delay difference itself, and thus has no problem for either narrowband or wideband signal.

In general, TTD can be implemented in analog domain, digital domain, passband, baseband, or a combination of them. Figures 5.4-9, 5.4-10 and 5.4-11 provide some implementation architecture examples, which are from the receiver perspective.

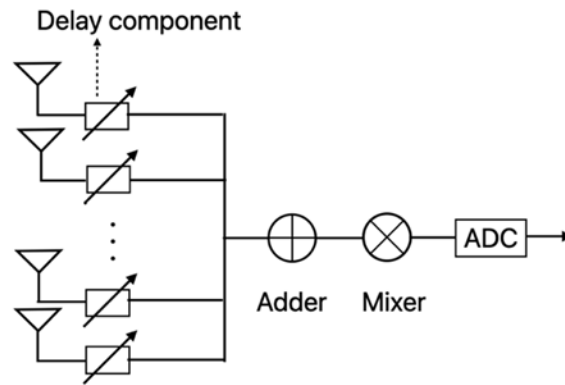


Figure 5.4-9: TTD implementation in RF

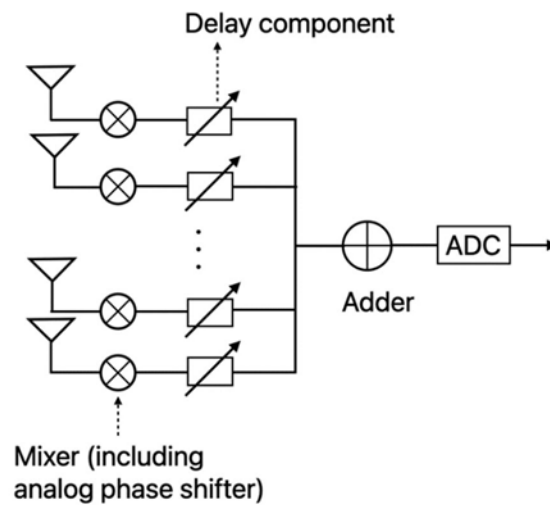


Figure 5.4-10: TTD implementation in analog baseband

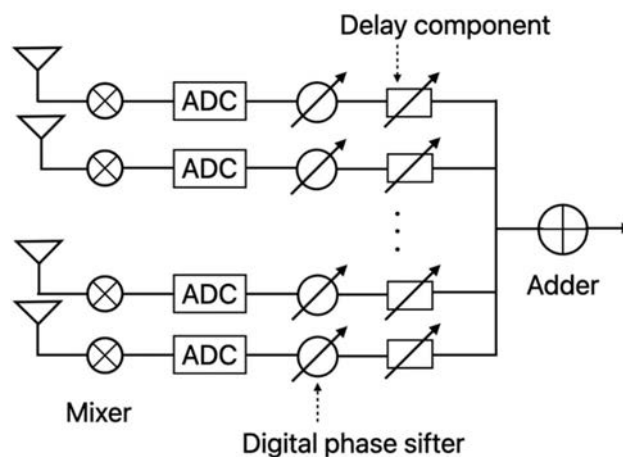


Figure 5.4-11: TTD implementation in digital baseband

Each architecture option has its disadvantages and limitations:

- TTD implementation in RF (Figure 5.4-9) is prone to process-voltage-temperature variation and delay variation, and has high power consumption. It is not a solution in practice.
- For TTD implementation in analog baseband (Figure 5.4-10), it has delay range limitation.

EXAMPLE: The state-of-art delay TTD delay range is in the order of 15 ns [i.83].

- TTD implementation in digital baseband (Figure 5.4-11) requires pure digital beamforming architecture and is fairly costly for large antenna arrays.
- TTD implementation in digital baseband using bandpass sampling is proposed in [i.81]. It obtains the I/Q samples by directly sampling the bandpass signal. Effectively, the TTD is implemented in digital baseband. However, the mechanism is very sensitive to ADC errors and can have quite high power consumption.

Therefore, the conventional TTD may not be a practical solution. On the other hand, as analysed above the beam squinting effects can be quite detrimental in some scenarios, especially for THz communication which potentially has large antenna array and wide channel bandwidth. Hence, practical beam squinting elimination or reduction techniques should be further studied for THz system design.

5.5 Impact of RF Impairments on THz Links

In order to show the impact of RF impairments on THz links, this clause provides results from a simulation-based study for a point-to-point link in a data center environment at 300 GHz based on [i.84] and [i.85]. The investigations comprise the impact of linear and non-linear distortion of the Power Amplifier (PA), Phase Noise (PN) and I/Q-imbalance on the Error Vector Magnitude (EVM) and Bit Error Rate (BER) via Link Level Simulations (LLSs) with the Simulator for Mobile Networks (SiMoNe) [i.86].

In the following a brief description of the four RF impairments models used in this study is provided. A more detailed description can be found in [i.84] and [i.85]:

- *Linear distortion* is modelled by a Finite Impulse Response (FIR) filter with a given transfer function. The corresponding PA characteristics are taken from [i.87] and the conversion gain of mixer is taken from [i.88]. Two filters are implemented dealing separately with the I/Q components to take into account, that the mixer acts separately on the I and Q components.
- *Non-linear Distortion* is modelled by an Amplitude Modulation (AM) with an (AM)-AM characteristic and an AM-Phase Modulation (PM) characteristic. A memoryless polynomial model given by a truncated power series of order K is applied [i.89] and the realistic coefficients are extracted from [i.99].
- *In-phase and quadrature Imbalance* is modelled by the signal model from [i.90] assuming frequency independent impairments and realistic characteristics from [i.91].
- *Phase Noise* is modelled using a realistic PN power density spectrum from an optoelectronic phase-locked loop measured in [i.92].

The Schematic view of RF hardware models in the simulation of the communication channel together with the signal vector diagrams for originating from the various RF impairments are shown in Figure 5.5-1. The characteristic used for the modeling of the propagation channel have been derived from an extensive measurement campaign described in [i.93]. Concrete, the channel impulse responses ToR P2P DL2 setup from [i.93] are applied here. The simulation parameters used in this study are listed in Table 5.5-1. The investigated modulation and coding schemes are those defined in IEEE 802.15.3d-2017 [i.94].

Table 5.5-1: Simulation Parameter
(Source: [i.84] Copyright 2024 Shaker Verlag, reproduced with permission)

Parameter	Value
Transmit pulse	RRC with roll-off factor 0,3
Modulation scheme	QPSK, 8-PSK, 8-APSK, 16-QAM, 64-QAM
Coding scheme	No coding, (255,239)-Reed-Solomon, 11/15-LDPC
Max. number of bits	100 Mbit
Radio channel gain	-58,4 dB
Transmit power	12 dBm
PA model	Two-box model of PA from [i.87]
Mixer	Frequency-dependent conversion gain from [i.88]
I/Q amplitude imbalance	1 dB
I/Q phase imbalance	4°
Noise figure	10 dB
Noise temperature	290 K

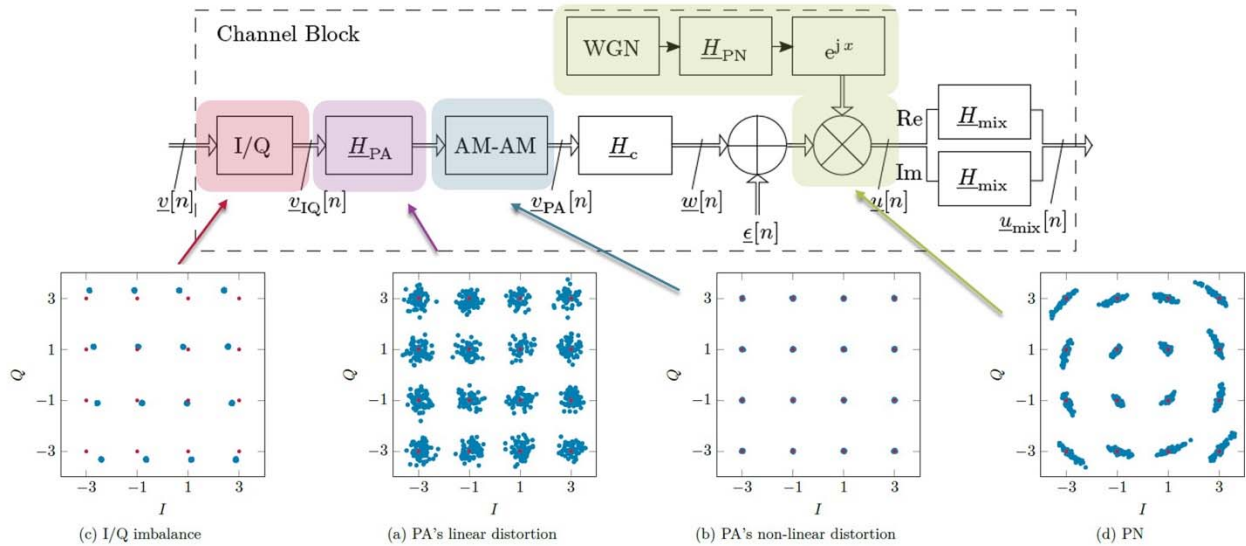


Figure 5.5-1: Schematic view of RF hardware models in the simulation of the communication channel

In order to quantitatively show the impact of various RF impairments including combinations of them Table 5.5-2 shows the Error Vector Magnitude (EVM) for these configurations. From these results it is obvious that the impact of the non-linear PA can be neglected when compared to the impact of the linear PA distortions, the PN and the I/Q imbalance. For a subset of these three dominant effects Figure 5.5-2 shows the BER with and without channel coding by a (255,239)-Reed-Solomon code. The BER increases with increasing symbol rates. The coding has a significant effect only for the more robust modulation schemes QPSK and 8-APSK, where coding improves the BER by one order of magnitude.

Table 5.5-2: Impact of RF Impairments on EVM in dB
(Source: [i.84], Copyright 2024 Shaker Verlag, reproduced with permission)

Impairment configuration	QPSK	8-PSK	8-APSK	16-QAM	64-QAM
Without	-47,0	-47,0	-48,7	-48,5	-50,4
AWGN	-42,3	-42,3	-43,5	-45,0	-45,5
PA linear	-19,2	-19,3	-21,4	-22,0	-23,7
PA non-linear	-47,2	-47,2	-47,0	-49,0	-49,9
Mixer	-35,5	-35,4	-37,6	-38,1	-39,2
I/Q	-18,2	-18,0	-20,2	-20,4	-22,3
PN	-16,0	-19,7	-19,6	-25,6	-26,9
All	-11,1	-14,4	-17,3	-17,4	-21,1

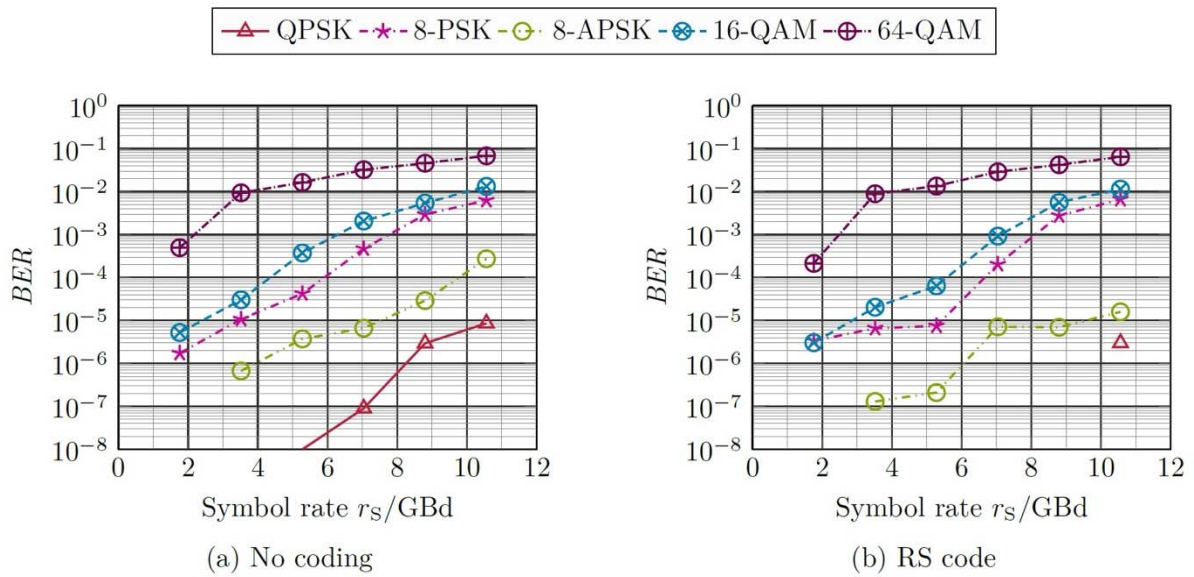


Figure 5.5-2: Impact of RF Impairments (PA, mixer, PN) on BER
(Source: [i.84], Copyright 2024 Shaker Verlag, reproduced with permission)

Using the same simulator, a multi carrier approach using aggregated channels with the various bandwidths defined in [i.94] has been simulated validating the approach taken in [i.95], where a bandwidth of 8,96 GHz has been realized by aggregating 4 channel with a bandwidth of 2,16 GHz relaxing the requirements of RF circuit design.

6 Practical Implementation Aspects

6.1 Packaging and Antenna Technologies

6.1.1 Impact of Packaging Technology

The feasibility of (sub-)THz electronics has been demonstrated in a variety of semiconductor and electro-optical materials up to several hundred GHz. These devices can become viable in consumer electronics only if they can facilitate low cost. There are two main cost factors in the sub-THz frequency range: semiconductor die and packaging. The former is well understood and follows the same trade-offs as other electronic devices (e.g. < 6 GHz RFICs), especially in CMOS. Smaller die size and older, widely available semiconductor processes lead to lower cost. Engineers strive to reduce the size of their Integrated Circuits (ICs) and it is not uncommon to find RF and mm-wave circuits designed in several process nodes older than their advanced digital counterparts.

There different many different packaging options discussed in the literature. Performance is a crucial aspect as illustrated in Figure 6.1-1. Connecting from the output of the transmitter and input of the receiver to their respective antennas introduces additional losses L_{pt} and L_{pr} , reducing the link margin by equal amounts. L_{pt} and L_{pr} are determined by the distance between the interfaces and the antennas as well as the package technology, materials and thickness.

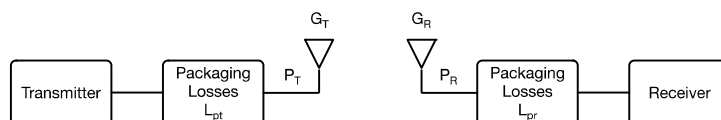


Figure 6.1-1: Package Losses in a typical radio transceiver

Packaging cost depends on a variety of factors, that also affect performance: materials, complexity (manufacturing technology, number of layers, etc.) and size. The following sections will touch upon these factors and present the different performance-cost trade-offs.

6.1.2 Antenna-In-Package vs Antenna-on-Die

6.1.2.0 Introduction

Communication systems in the (sub-)THz range will employ antenna arrays to compensate for the increased free space path loss. The physical antenna size is inversely proportional to the frequency of operation, while the same is not necessarily true for the overall die size. This has led several researchers to consider implementing the antenna [i.97] and [i.98] or the antenna feed [i.99] as part on the integrated circuit die. One such example is found in [i.99].

Integrated antennas significantly reduce the packaging complexity by allowing the use of simple and cheap flip-chip processing or even wire-bonding. The packaged die can then be directly soldered on a low frequency FR-4 Printed Circuit Board (PCB). The downside of this approach is that typically the die size needs to increase to accommodate the antennas. Depending on the IC cost per mm², the overall cost typically ends up being higher for frequencies below 200 GHz. This tradeoff will change at very high frequencies where transitioning from the IC to an external antenna might not even be feasible due to very high L_{pt} and L_{pr} .

A second approach, which has been widely adopted for mm-wave systems < 100 GHz is to use Antenna-in-Package (AiP). Typical AiP configurations found in [i.100] at 60 GHz and [i.101] at 140 GHz. The sub-THz die is flip-chip processed with small bump size and placed on the back side of a multi-layer PCB. Vias are used to connect the high frequency signals to the antennas which typically reside on the top layer. Bigger bumps are grown on the package PCB, which facilitate soldering it on a standard, lower-cost PCB along with other ICs for power management, digital processing etc. to form a complete system.

Obviously the AiP PCB number of layers, overall thickness and dielectric materials along with its size will determine its overall cost. AiPs have been demonstrated using relatively low-cost processes at 140 GHz [i.101] and [i.103] and up to 170 GHz [i.105].

6.1.2.1 Dielectric Materials

The routing loss and antenna radiation efficiency in standard PCB based AiPs largely depends on the type of type of dielectric used in the stack-up. Routing loss and antenna efficiency will be set by the thickness of the metals and dielectrics and importantly, by the dielectric loss tangent, $\tan\delta$. It should be emphasized that $\tan\delta$ has strong dependence on frequency.

References [i.101] and [i.102] have demonstrated that standard laminated dielectrics are a good choice for the lower sub-THz region (< 150 GHz). Higher frequencies might require lower loss materials such as Liquid Crystal Polymers (LCP) [i.104] or glass [i.105] along with a combination of the previous technologies. Higher performing dielectrics are expected to introduce additional cost, especially if they require a special manufacturing technology such as LTCC.

6.2 Semiconductor Technologies

Different options exist for generating and detecting THz waves. Specifically, for the sub-THz frequency range, below 300 GHz, semiconductor MMICs (Microwave Monolithic Integrated Circuits) are a compelling candidate due to their performance, smaller size and lower cost than alternative options.

There are two board categories of semiconductor materials used for electronics:

- Silicon; and
- III-V semiconductors.

III-V semiconductors (GaAs, InP, GaN) can achieve higher speed and output power but suffer from limited integration and high cost. Silicon, especially CMOS, has dominated RFICs in the past two decades. Its RF performance is generally lower than III-V, but it facilitates high integration and lower cost.

Gallium arsenide (GaAs)

GaAs has been used at very high frequency and high power applications in high volume (e.g. cell phone power amplifiers) for decades. Different devices are available:

- pseudomorphic High Electron Mobility Transistors (pHEMTs) which demonstrate very low noise;

- Heterojunction Bipolar Transistors (HBTs) which are typically used in high power applications; and
- Schottky diodes that operate as mixers and downconverters up to several THz.

The main disadvantage of GaAs is the relatively higher wafer cost (compared to silicon) and low integration. However, due to its existing high volume application in commercial electronics and optoelectronics, GaAs wafer cost is decreasing.

Indium Phosphide (InP)

InP has the highest electron mobility and saturation velocity. InP HBTs achieve the highest cut-off frequencies of any semiconductor electronic device and have been demonstrated in circuits operating in excess of 0,5 THz [i.106] and [i.108]. InP High Electron Mobility Transistors (HEMTs) achieve the lowest noise and are typically used in THz radio astronomy applications, many times while being cryogenically cooled.

InP suffers from extremely high wafer cost, higher than GaAs, and low integration. Fabrication is typically done by government or military contractors and InP devices are currently used only in low volume, high performance applications. Due to these limitations, there is little chance that InP can be used for high volume products in the 6G timeframe.

Gallium Nitride (GaN)

GaN is typically used in high power applications due to its very wide bandgap and breakdown field. This allows GaN transistors to operate under high bias voltages and thus deliver high output power. Most often GaN devices are combined with silicon carbide substrates to improve their heat dissipation.

GaN power amplifiers find application in cellular base stations, power converters and power supplies. However, due to the limited mobility of GaN, its mm-wave applications have been limited. As a result, the probability of GaN becoming a mature mass-market technology for sub-THz in the 6G timeframe is limited.

CMOS and Silicon Germanium (SiGe) HBT

CMOS is a widely available technology with applications that span every aspect of modern life. It has dominated RFIC design over the past 20 years. Highly integrated silicon RFICs at 140 GHz have been demonstrated [i.107] and [i.108] with good performance, albeit at higher power dissipation. SiGe HBTs are used in automotive radars and have also been demonstrated in the lower sub-THz region, e.g. in [i.108] and [i.109] at 160 GHz. SiGe HBTs can be integrated along with CMOS transistors in a BiCMOS process that allows both high speed and high integration.

Both CMOS and SiGe BiCMOS are expected to play a crucial role in 6G, especially in potential D-band deployments. However, it should be emphasized that their performance degrades rapidly beyond the D-band. Other technologies such as GaAs or photonic based will be needed at higher frequency.

[i.96] summarizes the different electronic technologies available for (sub-)THz.

6.3 Photonic Technologies

6.3.1 Transmitter and Receiver Architecture for sub-THz Communication Systems based on Photonics

In general, it is known that there are three methods to provide a sub-THz transmitter and a sub-THz receiver required for configuring the sub-THz communication systems. Figure 6.3-1 shows a sub-THz transmitter including the external optical modulator based on intensity modulation and a sub-THz receiver including the diode detector based on envelope detection [i.110] and [i.111]. In this configuration, a photonics-based sub-THz transmitter mainly consists of a data modulation part and THz wave generation part. The data modulation part is composed of two light sources like Laser Diode (LD), an external optical modulator, a data encoder, an optical amplifier and an optical bandpass filter. Two light sources are employed for optical heterodyne mixing procedure. One of them is employed for optical Local Oscillator (LO) and the other is utilized for optical intensity modulation. Based on optical heterodyne mixing principle, the frequency difference between 2 light sources is converted to the output frequency of photomixer [i.111]. The two light sources can be configured with commonly used semiconductor LDs. For special applications, fibre lasers or external cavity lasers can also be used. In addition to these single laser modules, optical comb generator with multi-wavelength output can be utilized for light sources. In this contribution, the sub-THz transmitter using an optical comb generator was intentionally excluded. This is because multi-wavelength light sources do not affect the functionality of a sub-THz transmitter, except for the structure of the light source itself in optical heterodyne mixing [i.112]. The external optical modulator plays the role of modulating the digital signal generated by the data encoder on the CW optical carrier, typically using either a Mach-Zehnder Modulator (MZM) or an Electro-Absorption Modulator (EAM). An optical amplifier such as Erbium Doped Fiber Amplifier (EDFA) or Semiconductor Optical Amplifier (SOA) primarily serves to compensate losses in an external optical modulator or to produce an optical signal with adequate input power for effective operation of a Uni-Traveling Carrier Photodiode (UTC-PD), a type of photomixer. An optical bandpass filter (OBPF) is employed to minimize Signal to Noise Ratio (SNR) degradations in optical carrier caused by Amplified Spontaneous Emission (ASE) noise produced when operating an optical amplifier [i.112]. The THz wave generation part is mainly composed of photomixer and Variable Optical Attenuator (VOA). Photomixer like UTC-PD or Positive-Intrinsic-Negative Photodiode (PIN-PD) performs the role of generating sub-THz electromagnetic waves based on the optical heterodyne mixing principle using the two lights generated from the data modulation part. The output of photomixer is typically comprised of various kinds of rectangular waveguide coupled devices (for example antenna or amplifier, etc.). The VOA adjusts the optical power level injected into the photomixer to enable it to operate under appropriate operating conditions.

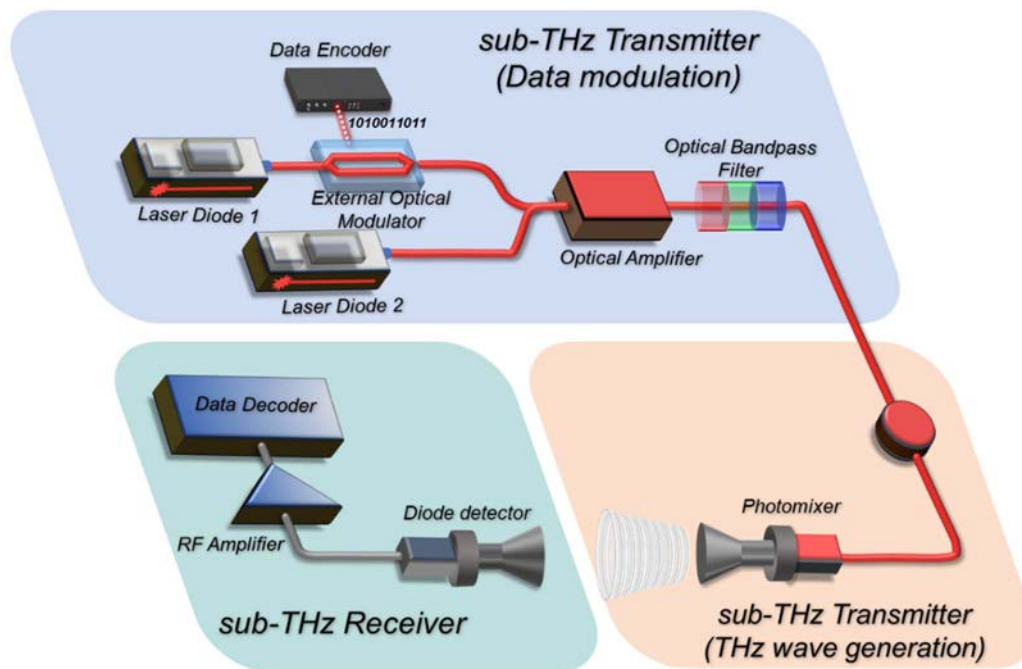


Figure 6.3-1: A sub-THz transmitter including the external optical modulator based on intensity modulation and a sub-THz receiver including the diode detector based on envelope detection

The structure of a sub-THz receiver is generally the same as that used in RF electronics [i.110] and [i.111]. As illustrated in Figure 6.3-1, a sub-THz receiver includes the diode detector, RF amplifier, and data decoder. The diode detector can be configured with the most widely used Schottky Barrier Diode (SBD) or Fermi-Level Managed Barrier Diode (FMBD). The RF amplifier can be typically used with appropriate bandwidth and gain considering the speed of the transmitted signal. An error detector can be served as a data decoder that is compatible with the envelope detection scheme to measure bit error rates for Non-Return-to-Zero On-Off-Keying (NRZ-OOK) signal.

In particular, this configuration has an advantage that the implementation cost of the sub-THz transmitter/receiver is relatively low and the structure is very simple. However, providing a transmission speed higher than the modulation bandwidth of the optical modulator is challenging. In general, the modulation speed of optical intensity modulators using electro-optic effects is known to support up to 40 Gbps. Additionally, using a commercially available SBD or FMBD, the receiver sensitivity is relatively higher than mixer, and the maximum allowable bandwidth is limited to ≤ 40 GHz or 10 GHz, respectively.

Figure 6.3-2 shows a sub-THz transmitter and a sub-THz receiver architecture using direct modulation and envelope detection. This transmitter/receiver architecture is almost similar to the configuration shown in Figure 6.3-1. Instead of using external optical modulator, a directly modulated LD like Distributed Feedback LD (DFB-LD) is employed for a light source and a data modulator simultaneously. By adopting this configuration, the cost-effectiveness of a sub-THz transmitter can be improved due to the utilization of cost-effective DFB-LD. However, the modulation bandwidth of the directly modulated LD limits the data transmission speed. Currently, when using commercial directly modulated DFB-LD, the maximum transmission speed based on OOK modulation format is known to be limited to 25 Gbps. Thus, it can be implemented economically in applications with low data throughput requirements (below 25 Gbps) or the initial deployment status of a sub-THz communication systems.

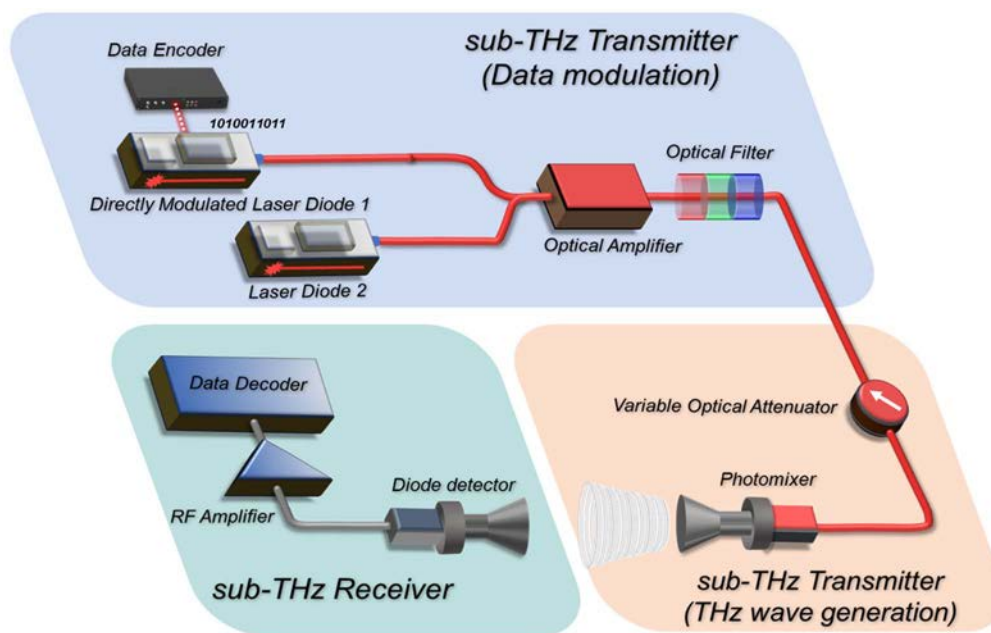


Figure 6.3-2: A sub-THz transmitter and a sub-THz receiver architecture using direct modulation and envelope detection

Figure 6.3-3 shows a sub-THz transmitter including the optical IQ modulator based on field modulation and a sub-THz receiver including the mixer based on coherent detection scheme. This structure has the same configuration as depicted in Figure 6.3-1, but instead of using an optical intensity modulator for data modulation, it uses an optical IQ modulator, which modulates both intensity and phase simultaneously. Currently, commercial optical IQ modulators support rates up to 40 Gbaud, typically utilizing LiNbO₃-based electro-optic modulators. For data encoding, a Digital Signal Processor (DSP) is generally utilized which is shown in Figure 6.3-4. Moreover, real-time operation, the bandwidth and bit resolution of the data converter are very important.

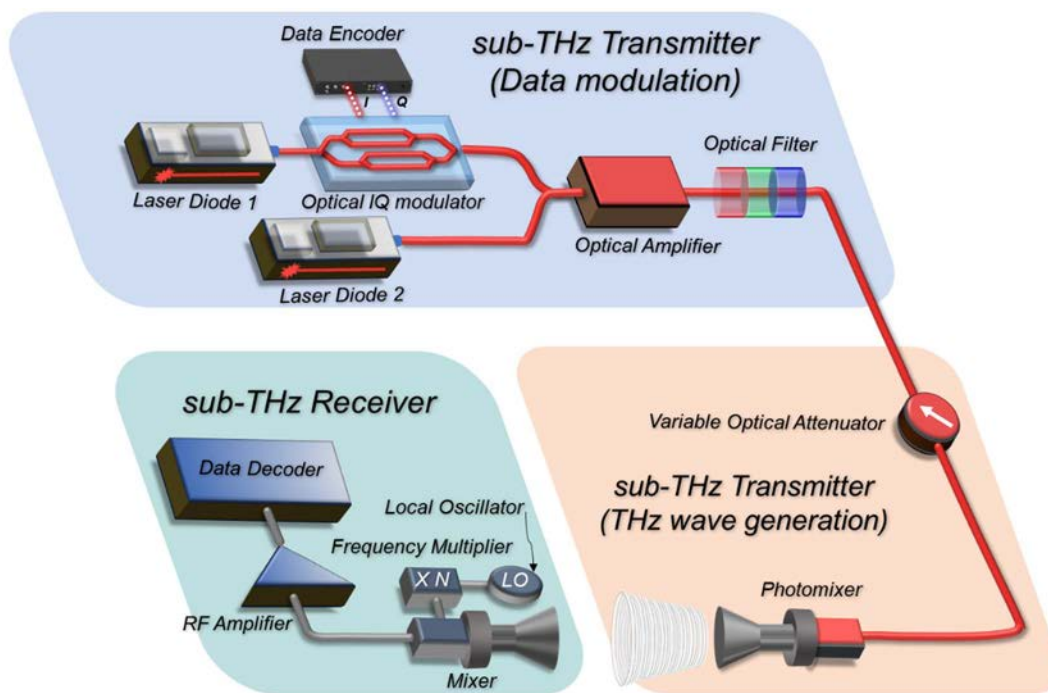


Figure 6.3-3: A sub-THz transmitter including the optical IQ modulator based on field modulation and a sub-THz receiver including the mixer based on coherent detection

The structure of a sub-THz receiver is also the same as that used in RF electronics. This receiver structure employs a coherent detection scheme and primarily comprises a mixer, frequency multiplier, and Local Oscillator (LO). Typically, fundamental or harmonic mixers can be employed. Mixers operating in the currently commercialized sub-THz band can support an output Intermediate Frequency (IF) range of up to 40 GHz. The frequency multiplier should be chosen based on the target sub-THz frequency regime and the available LO frequency. An RF amplifier can be utilized with appropriate bandwidth and gain taking into account the baud rate of the data signal generated from a sub-THz transmitter. The data decoder is basically composed of a DSP suitable for recovering the signal used in the data encoder on the transmitter side, and can accommodate both single carrier signals and multi-carrier signals such as OFDM signal. As explained earlier, the bandwidth and bit resolution of the data converter in the front-end of data decoder are also very crucial. For better understanding, an example of DSP architecture for single carrier is shown in Figure 6.3-4.

In particular, this configuration has a disadvantage in that the implementation cost of a sub-THz transmitter and a sub-THz receiver is relatively high. Also, the configuration is relatively complicated because the DSP for data encoding and decoding and a mixer with multi components are required. However, when using this structure of transmitter/receiver, it is possible to transmit a signal capable of multi-level and multi-phase modulation/demodulation with high spectral efficiency. As a result, this enabled the provision of a transmission speed of 100 Gb/s or higher. It also provides the advantage of having a wide dynamic range for received signals due to the coherent detection.

Figure 6.3-4 shows an example structure of the DSP used in the sub-THz transmitter/receiver and the data frame format. The generated Pseudo Random Binary Sequence (PRBS) data are mapped into a Gray mapped m-QAM signal. Following that, a preamble is inserted, and the signal is oversampled. Then, it is filtered using a square-root-raised-cosine filter with a proper roll-off factor, as shown in Figure 6.3-4(a). Figure 6.3-4(b) shows a detailed example structure of DSP for a receiver. The received signal within the pass-band is then post-emphasized, and the frequency is down-converted back to a baseband signal. After passing through the low-pass filter, the baseband signal is resampled twice at the baud rate. Then, the timing error recovery block estimates and compensates for the initial timing offset by finding a value that minimizes the metric using a square time algorithm to follow the sampled phase offset quickly [i.113]. A timing error recovery block with a feedback structure consisting of a phase detector, square time algorithm, and an interpolator for a second-order loop filter operates [i.112] and [i.113]. After the timing retrieval process, the preamble for Carrier Frequency Offset (CFO) estimation is examined to find a time index that maximizes auto-correlation among the recovered timing signals. The CFO recovered signal is post-equalized with pre-measured equalizer filter coefficients. The phase rotation is estimated from the equalized signal using phase search, phase detection, and a phase estimation algorithm [i.113], [i.114] and [i.115]. The phase recovered signal is de-mapped back into a bit stream. The frame starts from the preamble to provide a relatively accurate CFO estimation function over a wide range. After the preamble is inserted, training sequences are attached to learn channel equalization in the receiver DSP. After the training symbol, a payload data sequence is provided, shown in Figure 6.3-4(c) [i.113].

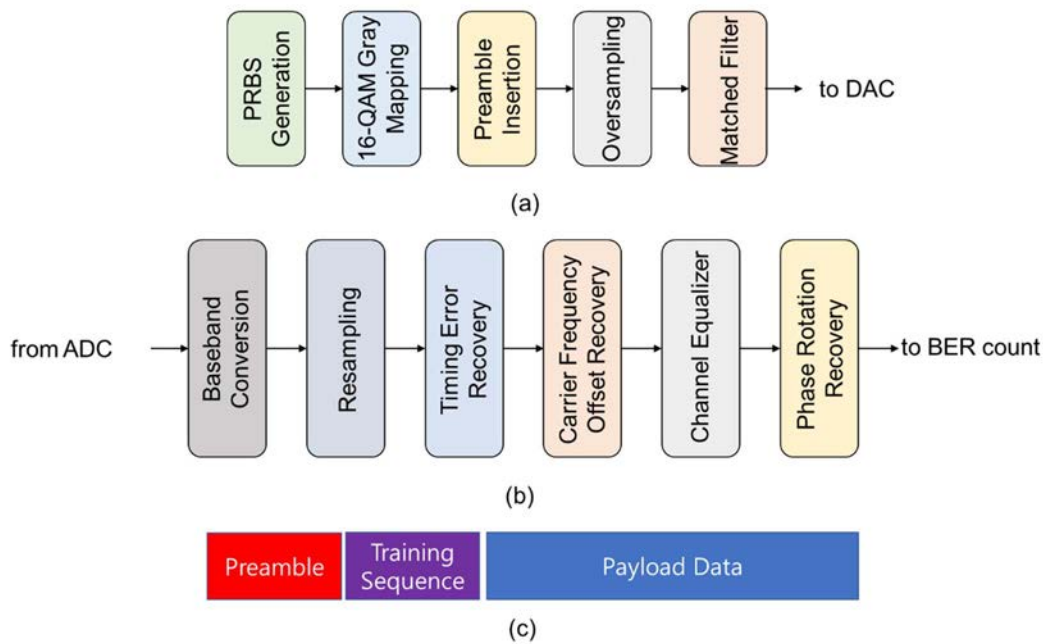


Figure 6.3-4: An example structure of the DSP used in a sub-THz transmitter/receiver and the data frame format (a) DSP for transmitter, (b) DSP for receiver and (c) data frame format

The characteristics of each configuration including complexity, cost-effectiveness, and application areas are briefly summarized in Table 6.3-1.

Table 6.3-1: The characteristics of each transmitter and receiver configuration based on photonics

No.	Transmitter and Receiver Architecture	Complexity	Cost-effectiveness	Applications area
1	Intensity modulation and envelope detection	Simple	Medium-cost	<ul style="list-style-type: none"> • Intermediate deployment stage • Up to 40 Gb/s data rate • Short-range communications
2	Direct modulation and envelope detection	Simple	High-cost	<ul style="list-style-type: none"> • Initial deployment stage • Up to 25 Gb/s data rate • Very short-range communications
3	Field modulation and coherent detection	Complex	Low-cost	<ul style="list-style-type: none"> • Initial deployment stage • Above 100 Gb/s data rate • Long-range communications

6.3.2 Key Components for sub-THz Communication Systems based on Photonics

There are two main types of UTC-PD modules commercialized so far. The first is rectangular waveguide coupled UTC-PD module and the second is lens collimated UTC-PD module (or antenna integrated UTC-PD module). The available frequency band utilized by the rectangular waveguide coupled type is determined by the standard of the coupled waveguide, whereas the antenna integrated type can be employed across a significantly wider range of frequency bands. (100 GHz ~ 1 000 GHz). For the rectangular waveguide type, operating within a specific frequency band results in comparatively higher output power than that of the lens collimated type. Although it is feasible to integrate the waveguide with different types of antennas or other sub-THz components, a notable challenge arises due to its relatively large physical size. On the other hand, the lens collimated type has a relatively small form factor, which has the advantage of miniaturizing the transmitter and receiver, but has the disadvantage of making it difficult to practicalize it in a real communication system because the output power is very small.

Figure 6.3-5 shows the measured output power characteristics of a commercially available rectangular waveguide coupled type UTC-PD module combined with a horn antenna with WR3.4 waveguide specifications [i.116]. Figure 6.3-5(a) shows the measured output power from the UTC-PD module within the frequency range corresponding to the WR3.4 band [i.117]. The output power value is the best when the frequency is near 300 GHz. Inset of Figure 6.3-5(a) shows the photograph of rectangular waveguide coupled UTC-PD module combined with a horn antenna. Figure 6.3-5(b) shows the measured output power by varying the photocurrent into the UTC-PD module [i.117]. The output power is increased proportionally as increasing the photocurrent into the UTC-PD module. The maximum photocurrent was limited to 7,5 mA to avoid damage to the UTC-PD module [i.116] and [i.117].

The measured sub-THz output power from the lens collimated UTC-PD module is shown in Figure 6.3-6. Two modules purchased from different vendors were measured for comparison. Figure 6.3-6(a) shows the measured output power from the lens-collimated UTC-PD module within the frequency range from 200 GHz to 900 GHz. To measure the output power, the injected current was fixed at 6 mA. As shown in the inset of Figure 6.3-6(a), the physical size of lens collimated UTC-PD module is relatively small compared to the photograph shown in inset of Figure 6.3-5(a). The measured output power values at 300 GHz were 6,08 μW , 14,59 μW , and 26,9 μW for photocurrents of 4 mA, 6 mA, and 8 mA, which is also depicted in Figure 6.3-6(b).

When developing sub-THz communication systems based on photonics, there are a few issues that need to serious consideration. The first thing is low output power of the photomixer due to its low responsivity. The second thing is the relatively large form factor of photomixer module compared to RF electronics. For successful deployment for sub-THz communication systems, a photomixer module with high output power and miniaturization/integration of various photonic devices like UTC-PD should be required. To compensate for these shortcomings, various technological developments are being actively underway, but no notable achievements have been reported yet. However, in order to improve the UTC-PD output, It is expected that significant outcomes will soon be delivered by improving performances using a SiC platform and Silicon photonics integration [i.118] and [i.119].

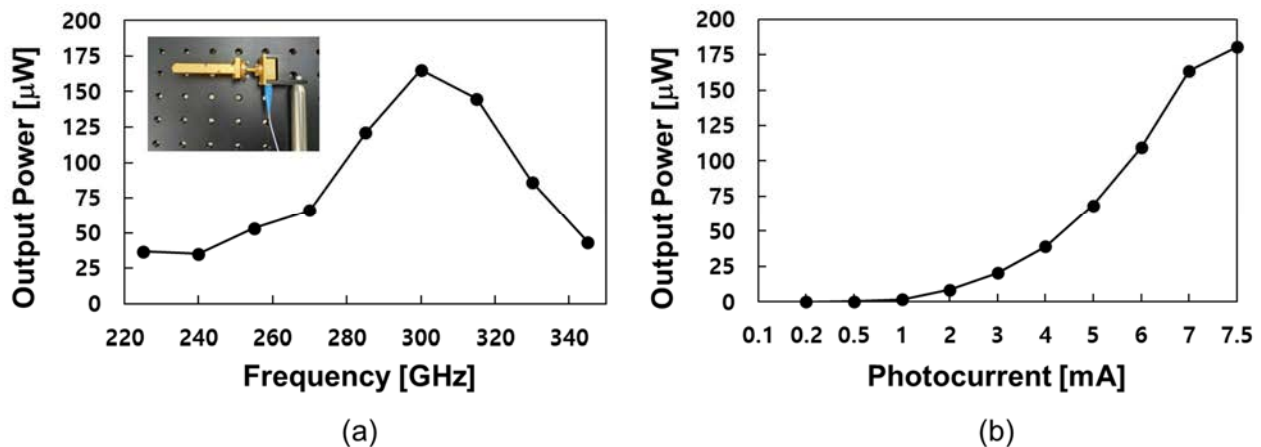


Figure 6.3-5: The measured output power characteristics of a rectangular waveguide coupled type UTC-PD module

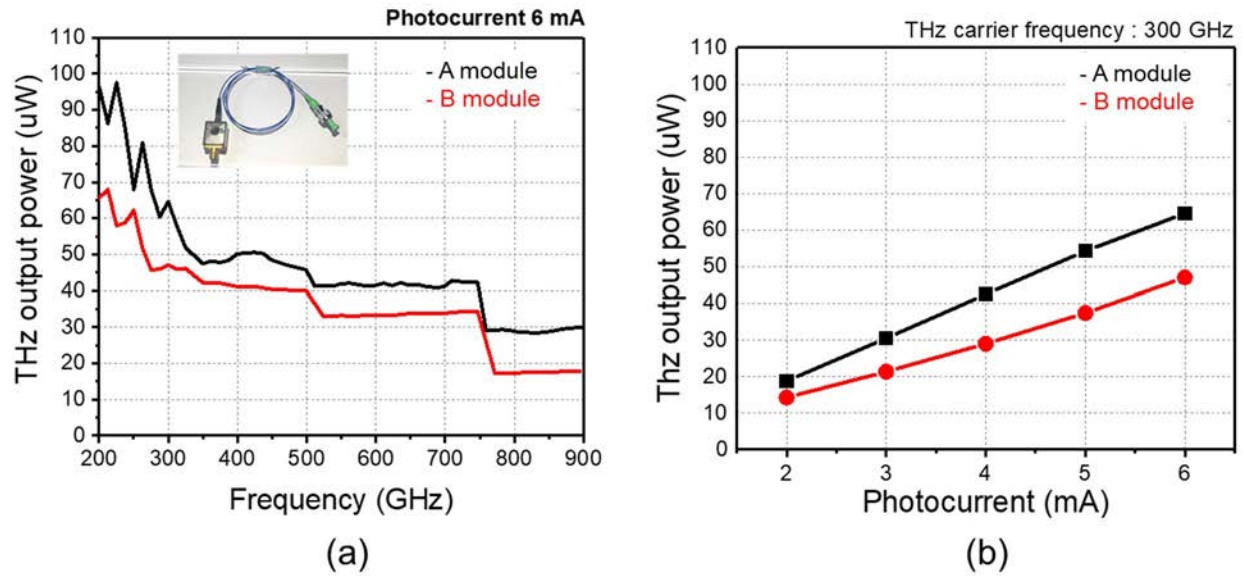


Figure 6.3-6: The measured sub-THz output power from the lens collimated UTC-PD module

6.3.3 Results of State-of-the-art sub-THz Transmission Experiments based on Photonics

In Table 6.3-2, the results of state-of-the-art sub-THz transmission experiments based on photonics are summarized. All experimental results with carrier frequency near 300 GHz were chosen and summarized based on single carrier (channel) transmission experiment to investigate the relevance of sub-THz transmitter/receiver configuration.

Table 6.3-2: Results of state-of-the-art sub-THz transmission experiments based on photonics

No	Technology (transmitter receiver architecture)	Carrier Frequency [GHz]	Bit Rate [Gbps]	Wireless Transmission Distance [m]	Modulation Format	Use case defined in GR-001	References
1	Waveguide integrated InP-based PIN photodiode (filed modulation/coherent detection)	300	128	0,5	16-QAM	<ul style="list-style-type: none"> intra-device communications 	[i.120]
2	Probabilistic constellation shaping (filed modulation/coherent detection)	450	132	1,8	64-QAM	<ul style="list-style-type: none"> intra-device communications 	[i.121]
3	Dual DFB laser diode integration (filed modulation/coherent detection)	408	131	10,7	16-QAM (OFDM)	<ul style="list-style-type: none"> in-airplane or train cabin entertainment wireless data centers ultra-high throughput for indoor users 	[i.122]
4	Si Photonics based optical intensity modulator (intensity modulation/envelop detection)	300	40	1,4	NRZ-OOK	<ul style="list-style-type: none"> intra-device communications 	[i.119]

No	Technology (transmitter receiver architecture)	Carrier Frequency [GHz]	Bit Rate [Gbps]	Wireless Transmission Distance [m]	Modulation Format	Use case defined in GR-001	References
5	PAM-N modulation (intensity modulation/envelop detection)	300	90	1,4	PAM-8	<ul style="list-style-type: none"> intra-device communications 	[i.123]
6	Adiabatic chirp management of directly modulated DFB-LD (direct modulation/envelop detection)	290	25	2,2	NRZ-OOK	<ul style="list-style-type: none"> in-airplane or train cabin entertainment ultra-high throughput for indoor users 	[i.124]
7	Probabilistic shaping & 2 × 50 dBi high gain antenna (filed modulation/coherent detection)	350	119,1	26,8	16-QAM (OFDM)	<ul style="list-style-type: none"> fixed point to point wireless applications mobile wireless X-haul transport 	[i.125]
8	Generalized K-K receiver with THz amplifier (filed modulation/coherent detection)	300	132	110	16-QAM	<ul style="list-style-type: none"> fixed point to point wireless applications mobile wireless X-haul transport grand events with ultra-high throughput 	[i.126]
9	Indoor network applications with up/down link configurations. (filed modulation/coherent detection)	300	120	2,5	16-QAM	<ul style="list-style-type: none"> in-airplane or train cabin entertainment wireless data centers ultra-high throughput for indoor users 	[i.117]
10	Probabilistic shaping (filed modulation/coherent detection)	339	124,8	104	256-QAM	<ul style="list-style-type: none"> fixed point to point wireless applications mobile wireless X-haul transport grand events with ultra-high throughput 	[i.127]
11	Single carrier modulation with high gain antenna and THz amplifier (filed modulation/coherent detection)	300	120	2,5	16-QAM	<ul style="list-style-type: none"> in-airplane or train cabin entertainment wireless data centers ultra-high throughput for indoor users 	[i.128]
12	Specially designed Plan-Convex lens with horn antenna (filed modulation/coherent detection)	320	50	850	16-QAM	<ul style="list-style-type: none"> fixed point to point wireless applications mobile wireless X-haul transport grand events with ultra-high throughput 	[i.129]

6.3.4 Phase noise in Microwave photonics transceivers

Phase noise in microwave photonics or indirect RF signal generation through heterodyning of optical modes on a fast photodiode is a critical aspect that affects the performance of the communication systems. As it is mentioned, heterodyning involves mixing two optical signals at different frequencies to generate an RF signal. In this process, any phase noise present in the optical signals is translated to the RF domain. The fast photodiode used in this setup converts the optical signals to electrical signals with high speed, enabling the generation of RF signals. However, the phase noise introduced by various sources such as laser linewidth, optical components, and environmental factors such as temperature fluctuation and vibrations can degrade the performance of the RF signal. Therefore, understanding and mitigating phase noise in microwave photonics systems is essential for achieving high-quality RF signal generation.

The primary method for producing RF signals with low phase noise in microwave photonics systems involves converting highly stable optical references into the RF domain using a frequency comb [i.133]. This method is known as Optical Frequency Division (OFD). At the core of the division process lies an optical frequency comb, pivotal for transferring the fractional stability of stable references at optical frequencies to the comb repetition rate at radio frequency. During frequency division, the output signal's phase noise is attenuated by the square of the division ratio compared to that of the input signal. Notably, a phase noise reduction factor of up to 86 dB has been documented. Nevertheless, the most stable microwaves obtained from Optical Frequency Division (OFD) predominantly hinge on bulk or fibre-based optical references, constraining advancements in applications requiring exceptionally low microwave phase noise. Recently many publications demonstrated the integrated version of OFD techniques at different sub-THz and millimetre-wave frequencies [i.134]. As an example, a miniaturized optical frequency division system that can potentially transfer the approach to a complementary metal-oxide-semiconductor-compatible integrated photonic platform is demonstrated in [i.134]. Phase stability is ensured through a spacious mode volume, planar-waveguide-based optical reference coil cavity. This stability is then down-converted from optical to RF frequency-utilizing soliton microcombs generated in a waveguide-coupled micro-resonator. In addition to achieving unprecedentedly low phase noise levels for integrated photonic sub-THz oscillators, these devices offer the possibility of heterogeneous integration with semiconductor lasers, amplifiers, and photodiodes. This integration potential holds promise for large-scale, cost-effective manufacturing suitable for widespread commercial applications.

6.3.5 Noise Figure of Microwave Photonic Receivers for coherent detection

The Noise Figure (NF) of microwave photonic receivers is a crucial parameter that characterizes the performance of these systems. Microwave photonic receivers convert microwave signals to optical signals, process them using optical components, and then convert them back to microwave signals for detection. During this process, various noise sources, such as shot noise, thermal noise, Relative Intensity Noise (RIN) of lasers and optical amplifier noise, can degrade the Signal-to-Noise Ratio (SNR) of the received signal. Careful design and optimization of the receiver's components and parameters are necessary to minimize noise and enhance system performance.

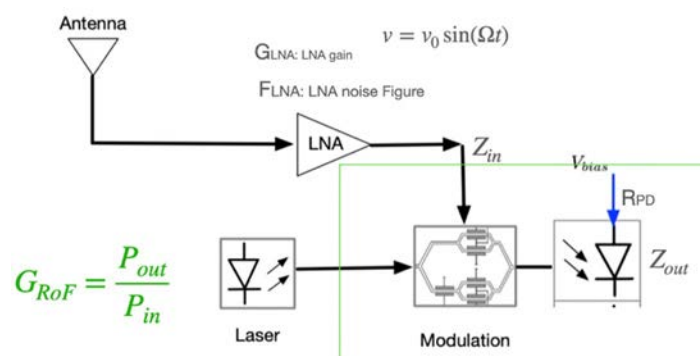


Figure 6.3-7: Microwave photonic receiver

A microwave photonics receiver schematic is presented in Figure 6.3-7. These receivers are converting the received RF signal to an optical signal using an electro-optical modulator (e.g. Mach-Zehnder Modulator (MZM)). The RF signal can be amplified using an LNA Low Noise Amplifier (LNA) in order to reduce the overall noise figure of the receiver. However, in certain publications [i.130], employing plasmonic technology, authors assert that the MZM modulator alone can yield sufficient gain. The optical signal that contains the received data is later demodulated back to electrical domain using a photodiode.

The first step in calculation of the noise figure of the microwave photonics receivers is to obtain the conversion gain from received RF signal to optics and again from optics to output of the photodiode. Let this gain be G_{RoF} . This gain can be calculated as follow and is shown in green box in Figure 6.3-7.

$$G_{RoF} = \frac{P_{out}}{P_{in}} \quad (46)$$

Where P_{out} is the output power at the output of the photodiode (Z_{out}) and P_{in} is the input RF power to the RF input port of the MZM (Z_{in}). Following some calculations and assuming that the MZM is biased at the quadrature point, and that the amplitude of the RF voltage (v_0) is small enough to make the MZM work linearly, one can obtain following [i.131]:

$$G_{RoF} = \frac{P_{out}}{P_{in}} = \left(\frac{\pi^2 Z_{in} Z_{out}}{V_{\pi}^2} \right) \left(\frac{R_{PD}}{\alpha} P_{opt} \right)^2 \quad (47)$$

Z_{in} and Z_{out} = Input impedance of the MZM and Output impedance of the photodiode, respectively.

R_{PD} = Photodiode responsivity (A/W).

α = Total optical insertion loss

V_{π} = Half wave voltage bias (voltage required to achieve a phase shift of π (180 degrees) in a MZM).

P_{opt} = Optical laser power.

The gain equation is written as follows:

$$G_{RoF} = \frac{P_{out}}{P_{in}} = \gamma (I_{DC})^2 \quad (48)$$

Where I_{DC} is the DC current at the output of the photodiode, and define:

$$\gamma = \frac{\pi^2 Z_{in} Z_{out}}{V_{\pi}^2} \quad (49)$$

Inspecting equation (46), one can see that MZMs with higher V_{π} values create more gain for the receiver.

During the second step of noise figure calculation, it is necessary to assess the noise contributions originating from both the electrical and optical domains. This involves considering the thermal noise generated at the output of the photodiode load, as well as the thermal noise introduced by the antenna (and LNA in case it is used) and entering the system through the MZM RF input port. The photonics noise spectral density is written as follows:

$$N_{Photonics} = k_B T + k_B T G_{RoF} + N_{RIN} + N_{shot} \quad (50)$$

$k_B T$ = Output thermal noise. k_B is Boltzmann's constant, T is the standard temperature.

$k_B T G_{RoF}$ = Amplified input thermal noise.

N_{RIN} = Relative intensity noise (laser intensity fluctuations) spectral density.

N_{shot} = shot noise spectral density = $2qZ_{out}I_{DC}$ where q is the electron charge.

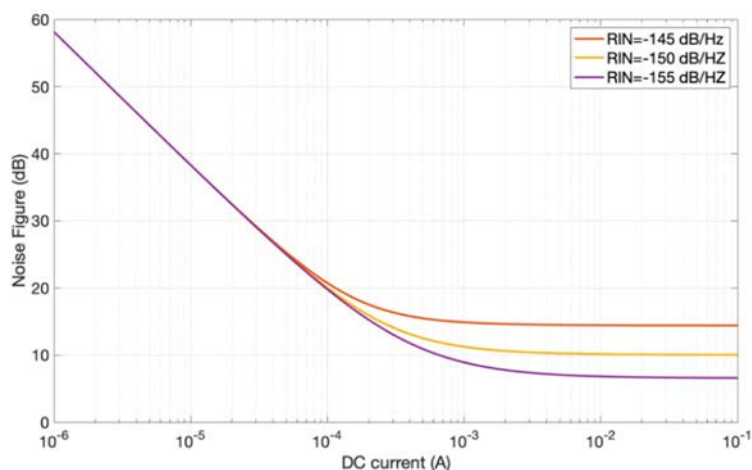
With the noise spectral density available, one can proceed to calculate the noise factor for the green box depicted in Figure 6.3-7:

$$F_{RoF} = \frac{N_{Photonics}}{k_B T G_{RoF}} = 1 + \frac{k_B T}{k_B T G_{RoF}} + \frac{N_{RIN}}{k_B T G_{RoF}} + \frac{N_{shot}}{k_B T G_{RoF}} \quad (51)$$

To consider the noise figure of the LNA, one can utilize the cascade formula for calculating the overall noise figure.

$$F_{Total} = F_{LNA} + \frac{F_{RoF}-1}{G_{LNA}} = F_{LNA} + \frac{1}{\gamma G_{LNA}} \left(\frac{1}{I_{DC}^2} + \left(\frac{2qZ_{out}}{k_B T} \right) \frac{1}{I_{DC}} + \left(\frac{Z_{out}}{k_B T} \right) N_{RIN} \right) \quad (52)$$

Figure 6.3-8 illustrates the Noise Figure (NF) values for various DC currents and different Relative Intensity Noise (RIN) levels. It is evident from the figure that increasing the received DC current leads to a reduction in the overall system NF. However, this decrease reaches a saturation point due to the presence of RIN noise. Consequently, to minimize the overall NF of the microwave receivers, it is necessary to both augment the received DC current and diminish the RIN noise of the laser source.



NOTE: LNA Noise Figure = 3 dB, LNA gain = 30 dB, $Z_{in} = Z_{out} = 50 \Omega$, half wave voltage = 4 V.

Figure 6.3-8: NF versus DC current

6.3.6 Microwave Photonics Phased Arrays

Microwave Photonics Phased Arrays represent a cutting-edge technology that integrates microwave and photonic components to create versatile, high-performance phased array systems. These arrays utilize optical phase modulation techniques to control the phase of microwave signals, offering advantages such as wide bandwidth, low loss, and immunity to electromagnetic interference. By leveraging the properties of optical waveguides and modulators, Microwave Photonics Phase Arrays can achieve precise and rapid phase control over a wide range of frequencies. This capability enables applications such as beamforming, radar, and wireless communication systems to dynamically steer and shape antenna beams with unprecedented flexibility and accuracy. However, challenges such as phase noise, optical losses, and complexity in system integration should be carefully addressed to fully exploit the potential of Microwave Photonics Phase Arrays in real-world applications. Despite these challenges, the ongoing advancements in optical and microwave technologies hold great promise for further enhancing the performance and versatility of Microwave Photonics Phase Arrays in the future.

Unlike traditional electronic phase shifters, which can introduce frequency-dependent phase errors, true time delay systems in microwave photonics ensure that signals are delayed by a constant time, irrespective of their frequency. This characteristic significantly enhances the performance of phased arrays by eliminating beam squint, where the direction of the main lobe changes with frequency. For example, in reference [i.132], the research emphasizes the use of Lithium Niobate On Insulator (LNOI) waveguides for true time delay lines. This approach showcases their wideband capability, low power consumption, and strong resistance to electromagnetic interference, all of which are essential attributes for high-performance microwave photonics applications.

Annex A: Bibliography

- A. Bhutani, B. Göttel, A. Lipp and T. Zwick: "Packaging Solution Based on Low-Temperature Cofired Ceramic Technology for Frequencies Beyond 100 GHz", in IEEE™ Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 5, pp. 945-954, May 2019.
- Xiao, Jun & Li, Xiuping & Qi, Zihang & Zhu, Hua. (2019): "140-GHz TE340-Mode Substrate Integrated Cavities-Fed Slot Antenna Array in LTCC". IEEE™ Access. pp. 1-1. 10.1109.
- W. Heinrich et al.: "Connecting Chips With More Than 100 GHz Bandwidth", in IEEE™ Journal of Microwaves, vol. 1, no. 1, pp. 364-373, January 2021.
- K. K. Samanta: "Ceramics for the Future: Advanced Millimeter-Wave Multilayer Multichip Module Integration and Packaging", in IEEE™ Microwave Magazine, vol. 19, no. 1, pp. 22-35, January-February 2018.
- "Fundamentals of THz Technology for 6G", T. Eichler, R. Ziegel, Rohde & Schwarz White Paper.
- "Cutting-edge terahertz technology", M. Tonouchi, Nature Photonics, vol. 1, p. 97 to 105, February 2007.
- F. Roccaforte and M. Leszczynski: "Nitride Semiconductor Technology: Power Electronics and Optoelectronic", Devices, Wiley-VCH Verlag GmbH & Co. KGaA, 2020.

History

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