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Surface Mount Technology (SMT); Requirements for Embedded Communication Modules For Machine To Machine Communications

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Contents

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Foreword

This Group Specification (GS) has been produced by ETSI Industry Specification Group (ISG) Surface Mount Technique (SMT).

Modal verbs terminology

In the present document "**shall**", "**shall not**", "**should**", "**should not**", "**may**", "**need not**", "**will**", "**will not**", "**can**" and "**cannot**" are to be interpreted as described in clause 3.2 of the ETSI Drafting Rules (Verbal forms for the expression of provisions).

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Introduction

The goal of the present document is to specify a form factor for Surface Mount Technology (SMT) based communication modules for devices supporting services across multiple vertical markets and not one specific market segment.

The present document reflects the current state for M2M and connected device design and attempts to address future needs.

1 Scope

This present document proposes mechanical and electrical requirements for wireless module implementations. This includes the SMT pad layout and common interface assignments for essential pads including some general electrical characteristics. Certain aspects such as z-height, shielding geometry and weight are not defined by the present document.

The SMT module pad configurations defined in the present document are primarily intended to allocate specific pad functionalities that need to be routed on the host device to the respective pads on the SMT module. Although many interfaces may be defined in the various pad configurations, it does not necessarily imply that all interfaces need to be supported at the same time. The assigned allocations are intended to enable the module supplier and host device integrator to design compatible circuits with aligned pad assignments as specified.

2 References

2.1 Normative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

Referenced documents which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

NOTE: While any hyperlinks included in this clause were valid at the time of publication, ETSI cannot guarantee their long term validity.

The following referenced documents are necessary for the application of the present document.

[1] ISO/IEC 7816-3: "Identification cards -- Integrated circuit cards -- Part 3: Cards with contacts -- Electrical interface and transmission protocols".

[2] ETSI TS 102 221: "Smart Cards; UICC-Terminal interface; Physical and logical characteristics".

[3] USB 2.0 Specification (April 2000): "Universal Serial Bus Specification, Revision 2.0".

NOTE: Available from http://www.usb.org/developers/docs/usb20_docs.

[4] USB 2.0 Specification: "HSIC - High-Speed Inter-Chip USB Electrical Specification", Version 1.0 (September 23, 2007), plus HSIC ECN Disconnect Supplement to High-Speed Inter-Chip Specification Revision 0.94 (September 20, 2012).

[5] USB 3.1 Specification (July 2013): "Universal Serial Bus 3.1 Specification".

NOTE: Available from http://www.usb.org/developers/docs/.

[6] PCI-SIG: "PCI Express M.2 Specification", Revision 1.0, December 12, 2013.

NOTE: Available from https://www.pcisig.com/specifications/pciexpress/M.2_Specification/.

[7] mipi alliance: "M-PHY® Specification", version 2.0, April 4, 2012.

NOTE: Available from http://mipi.org/specifications/physical-layer.

[8] ETSI TS 124 008: "Digital cellular telecommunications system (Phase 2+); Universal Mobile Telecommunications System (UMTS); LTE; Mobile radio interface Layer 3 specification; Core network protocols; Stage 3 (3GPP TS 24.008 Release 12)".

[9] mipi alliance: "Serial Low-power Inter-chip Media Bus (SLIMbus®) Specification".

NOTE: Available from http://mipi.org/specifications/serial-low-power-inter-chip-media-bus-slimbussm-specification.

[10] IEEE 1149.1: "IEEE Standard for Test Access Port and Boundary-Scan Architecture". (Joint Test Action Group, or JTAG).

[11] SD Card Association: "SD Specifications Part 1 - Physical Layer - Simplified Specification" Version 3.01, 2010.

[12] SD Card Association: "SD Specifications Part 1 - Physical Layer - Simplified Specification" Version 4.10, 2013.

[13] ISO 11898-1:2003: "Road vehicles -- Controller area network (CAN) -- Part 1: Data link layer and physical signalling".

NOTE: Available from http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=33422.

[14] C-PHY® Specification, version 1.0, October 2014.

NOTE: Available from http://mipi.org/specifications/physical-layer.

2.2 Informative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

NOTE: While any hyperlinks included in this clause were valid at the time of publication, ETSI cannot guarantee their long term validity.

The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

Not applicable.

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

AT command: command language with a series of short text strings which combine together to output complete commands for different operations such as hanging up, dialling and changing connection parameters for modems

C-PHY: specification which provides high throughput performance over bandwidth limited channels for connecting to peripherals, including displays and cameras

General Purpose I/O (GPIO): digital interface that can be set to electrical "0" or "1" by the module (output) or the host (input) with a use not defined by the present document

General Purpose Pad (GPP): pad on the physical form factor that is not assigned a specific function

NOTE: Module manufacturers have the choice of assigning an I/O interface to a general purpose pad, or support additional General Purpose I/O on a general purpose pad, or leave a general purpose pad unconnected.

ground slug pad: pad dedicated to electrical ground for the module

host device: any device that embeds a M2M module

M2M Device: physical equipment with communication capabilities that does not necessarily have a Human-Machine interface

Machine-to-Machine communications: transfer of information between M2M Devices

MIPI: alliance of companies which establishes standards for hardware and software interfaces in mobile devices

module: complete WWAN radio devices that for the purposes of the present document connect to the integrated device through a surface mount soldered connection

NOTE: A module may or may not include an integral antenna system or SIM/USIM interface.

M-PHY: specification which provides a serial interface technology with high bandwidth capabilities particularly developed for mobile applications to obtain low pin count combined with very good power efficiency

pad: physical contact on the module or host

pad layout: 2 dimensional configuration of the mechanical pad placement

pitch: distance between common points on two adjacent pads on a common row

shielding geometry: implementation of material to shield or isolate a portion or portions of the module

Surface Mount Technology (SMT): method for manufacturing electronic circuits in which the components are mounted directly onto the surface of printed circuit boards

z-height: height of the module in a 3 dimensional realm

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ADCI	A/D Converter input
API	Application Programming Interface
AT	Attention
CAN	Controller Area Network
CANBUS	Controller Area Network Bus
CLK	Clock
CSI	Camera Serial Interface
CTS	Clear To Send
DACO	D/A Converter output
DCD	Data Carrier Detect
DIN	Data Input
DOUT	Data Output
DPR	Dynamic Power Reduction
DSI	Display Serial Interfac
DSR	Data Set Ready
DTR	Data Terminal Ready
ETSI	European Telecommunication Standards Institute
GND	Ground (electrical)
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPP	General Purpose Pad
GPS	Global Positioning System
GS	Group Specification
HSIC	High-Speed Inter-Chip
I2C	Inter Integrated Circuit (interface)
I2S	Inter-IC Sound
IOH	High Output Current
IOL	Low Output Current
ISG	Industry Specification Group
JTAG	Joint Test Action Group

NOTE: IEEE 1149.1 [10].

LED	Light Emitting Diode
LGA	Land Grid Array
LLI	Low Latency Interface (MIPI)
LTE	Long Term Evolution
M2M	Machine to Machine Communications
MBIM	Mobile Broadband Interface Model

NFC	Near Field Communications
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect - express
PCM	Pulse Code Modulation
PHY	shortened form of the word PHYSICAL

NOTE: In the case of the present document this refers to the Physical Layer of the Open Systems Interconnection model (OSI Model).

PWM	Pulse Width Modulation
RF	Radio Frequency
RF_AUX	Antenna for auxiliary
RFU	Reserved for Future Use
RST	shortened form of the word RESET
RTC	Real Time Clock
RTS	Ready To Send
RX	Receive
SAR	Specific Absorption Rates
SDIO	Secure Digital Input Output
SIM	Subscriber Identity Module
SMT	Surface Mount Technology
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPU	Standard or Proprietary Use
SSIC	SuperSpeed Inter-Chip
TX	Transmit
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
UIM	User Identity Module
USB	Universal Serial Bus
VCC	Voltage Common Collector
VIH	High Input Voltage
VIL	Low Input Voltage
VOH	High Output Voltage
VOL	Low Output Voltage
VREF	Voltage Reference
WAN	Wide Area Network
WLAN	Wireless Local Area Network
WS	Word Select
WWAN	Wireless Wide Area Network
VBUS	Voltage of the Universal Serial Bus

4 Physical Form Factor Specifications

4.0 Physical Form Factor introduction

This clause defines the multiple physical form factors in terms of dimensions and pad assignments. Every design is complimentary to each other and can exist in a common footprint environment. All footprints share the same RF pad placement to optimize the reuse of designs. The naming convention SMTwwhh (ww=width, hh=height both in millimetres) provides the mapping to the specific physical layouts.

The SMT modules defined by the present document are LGA designs with all components mounted on a single side, and LGA pads mounted on the opposite side.

For any module design the recommendation is for all interface pads of a module to be soldered to the host PCB regardless of whether the pad is intended to be used electrically in the integrated design. The present document is based on the LGA methods, however, this does not explicitly exclude the use of other methods.

4.1 SMT Module Layouts

4.1.0 SMT Layout Family and Common Properties

This clause covers all modules defined in the present document for mechanical pad placement and association with specific electrical interfaces defined in clause 5. Figure 1 shows the overview of the family of modules included in the present document.

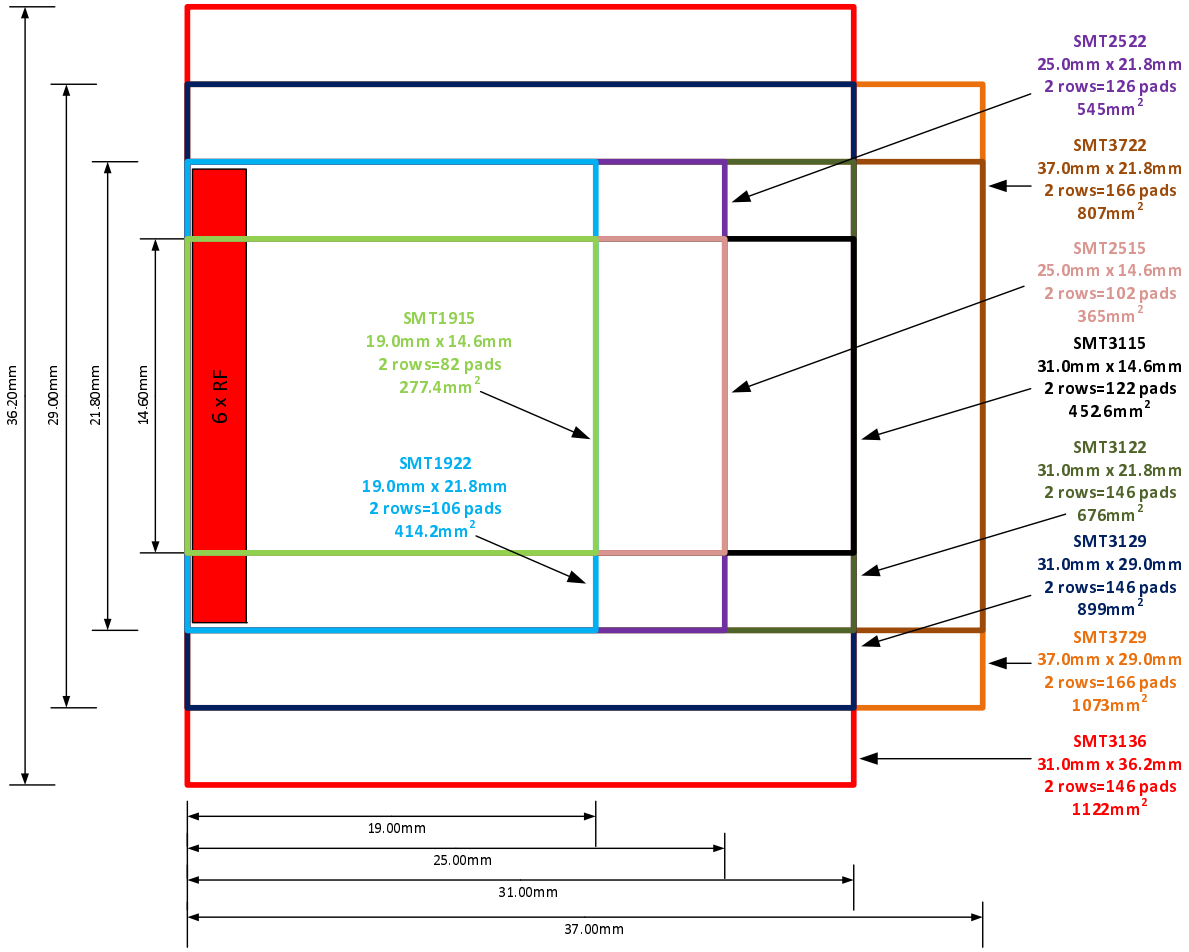

Figure 1: 10 SMT modules are shown with a common RF edge and horizontal centerline

The mechanical drawings for the module layout are as viewed from the top of the module down through the module also known as an X-Ray view. The host PCB layouts are a direct view of the PCB. The overhang at the edges of the module is stated below.

Each module in the present document shares the common properties of signal pads with a size of 1 mm × 0,7 mm spaced on a 1,2 mm pitch. The size of ground slug pads is defined in the mechanical drawings for each module. The mechanical tolerances for module pad placement allow for a variance of +/- 0,02 mm from the dimensions defined. The present document indicates a minimum 0,35 mm overhang from any outside pad to the outer edge of the module. Host PCB designs should take into consideration any overhang variance.

4.1.1 SMT3136 Module Mechanical Properties

Figures 2, 3 and 4 specify the overall dimensions of the SMT3136 module form factor in millimetres. The form factor provides 146 pads which are numbered 1 through 146.

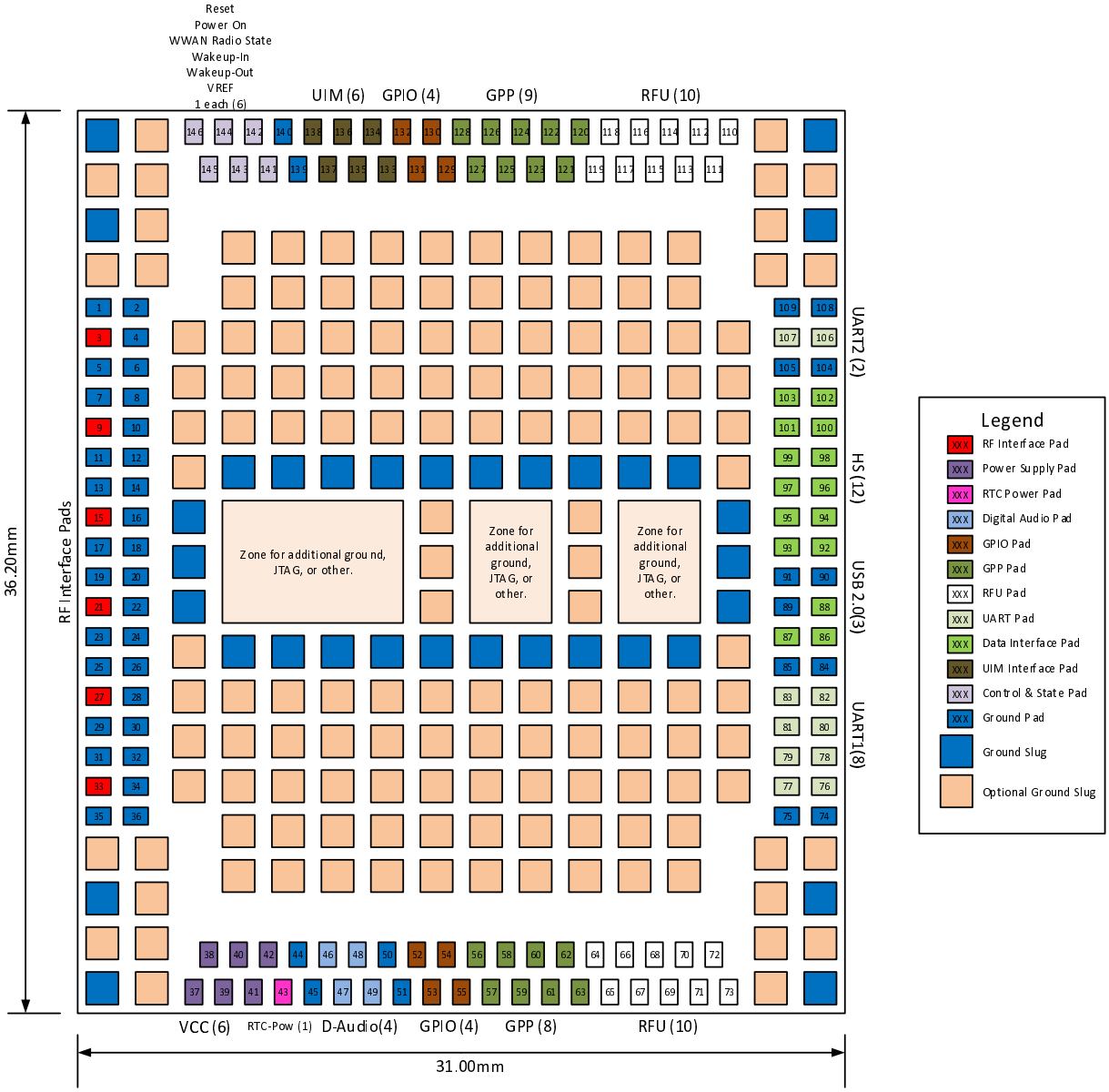

Figure 2: SMT3136 physical form factor (1 122 mm^2), dimensions, pad numbering and placement

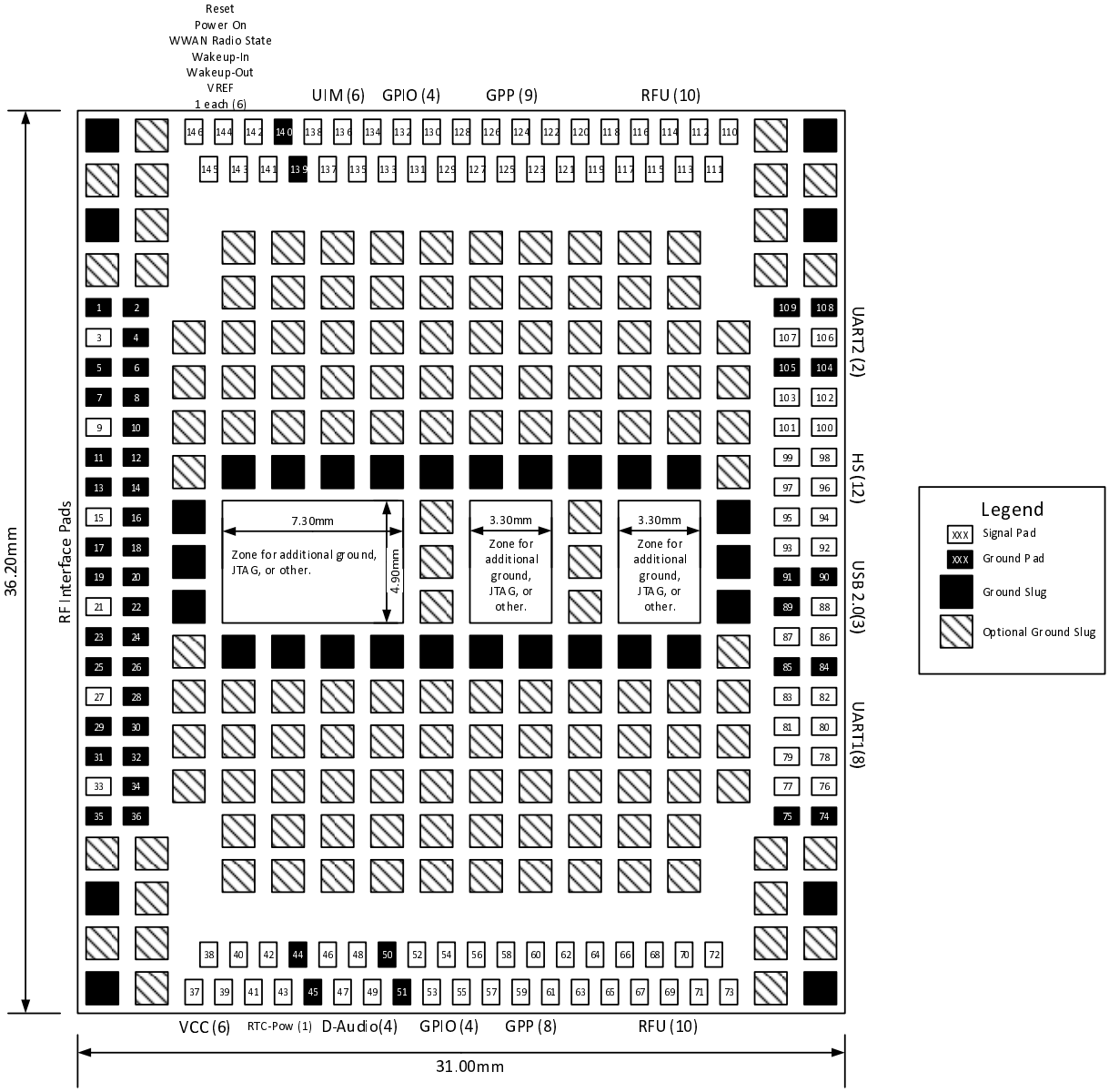

Figure 3: SMT3136 black and white physical form factor (1 122 mm^2), dimensions, pad numbering and placement

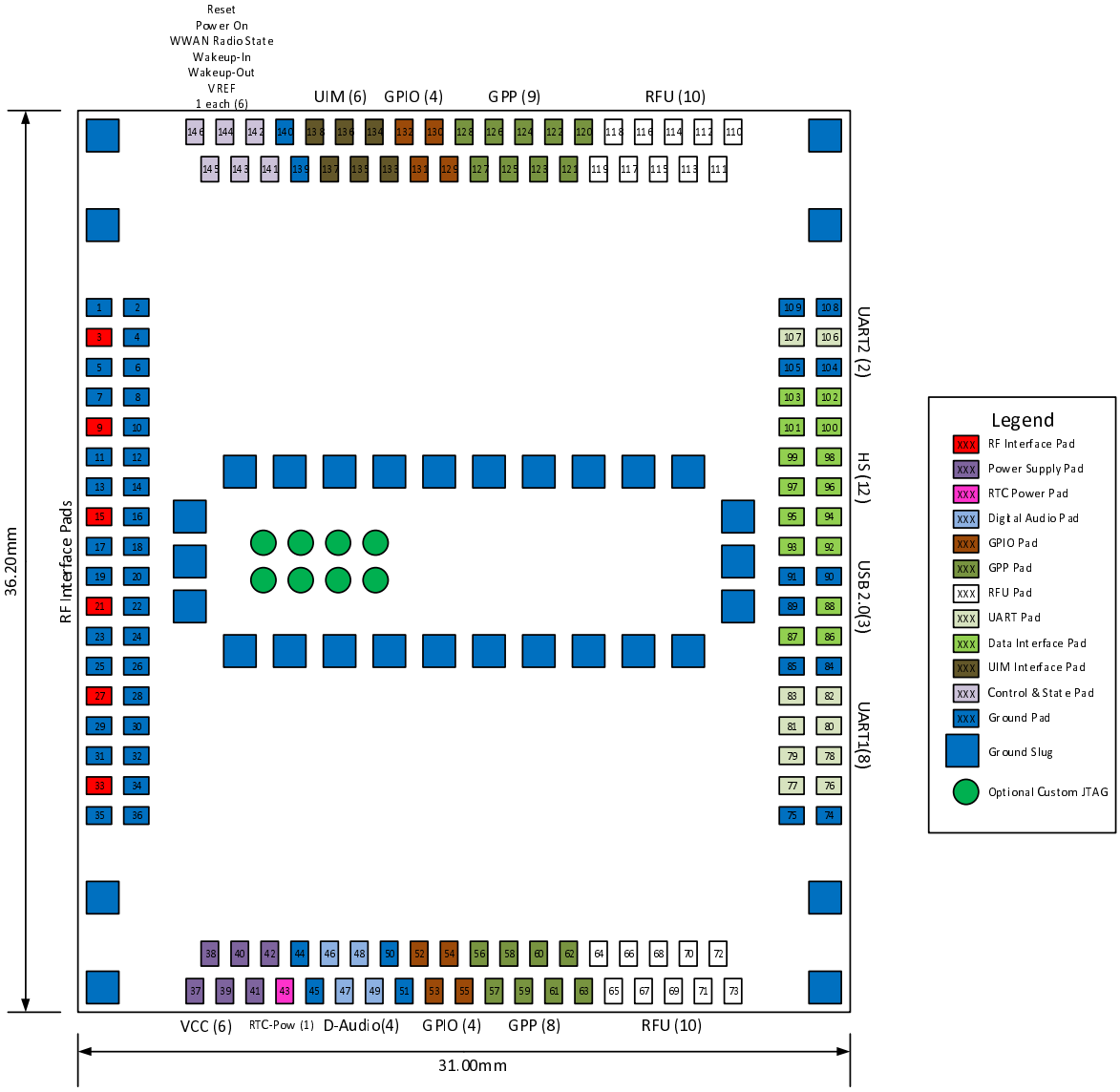

Figure 4: SMT3136 typical physical implementation (1 122 mm^2), dimensions, pad numbering and placement

4.1.2 SMT3129 Module Mechanical properties

Figures 5, 6 and 7 specify the overall dimensions of the SMT3129 module form factor in millimetres. The form factor provides 146 pads which are numbered 1 through 146.

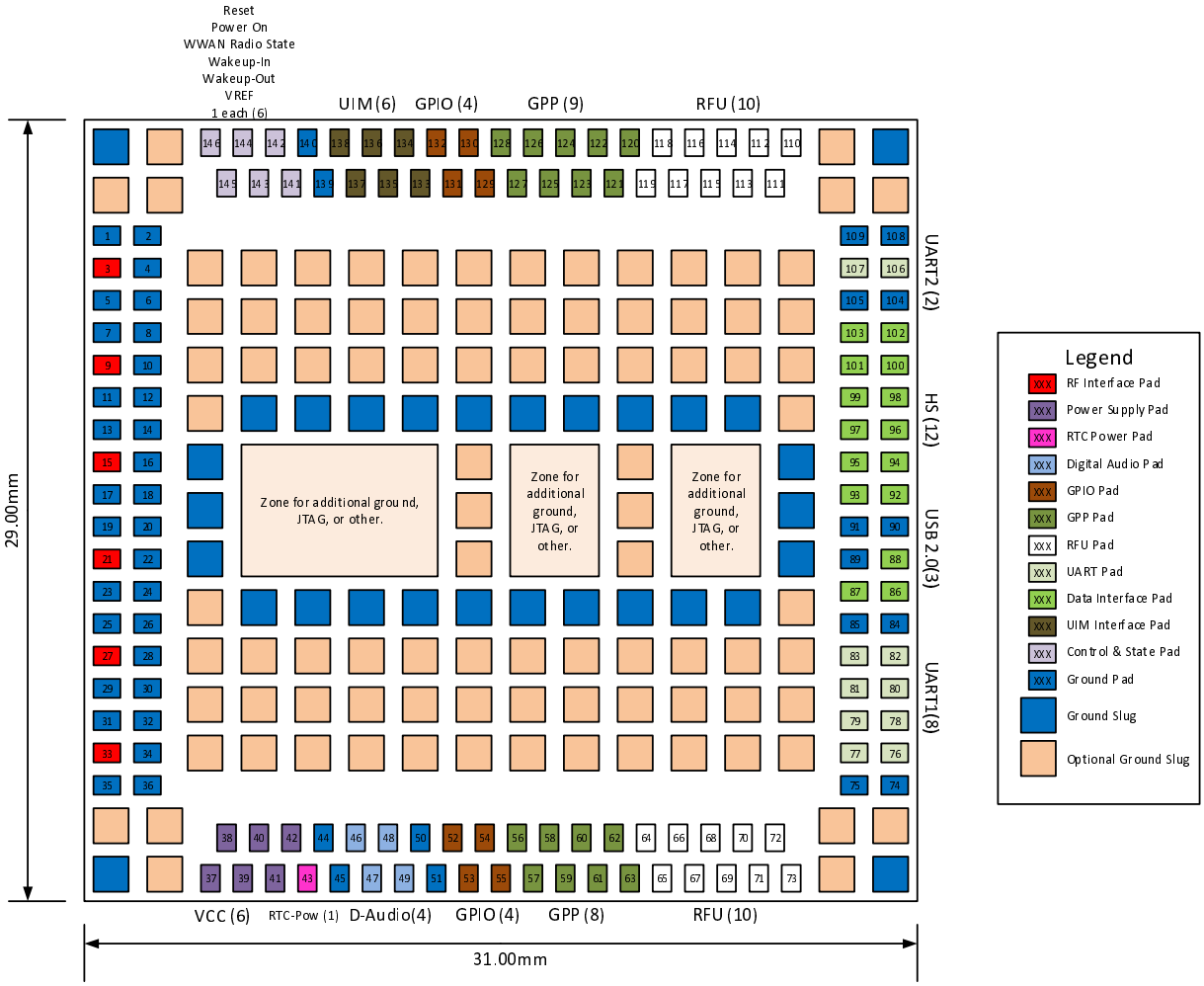

Figure 5: SMT3129 physical form factor (899 mm^2), dimensions, pad numbering and placement

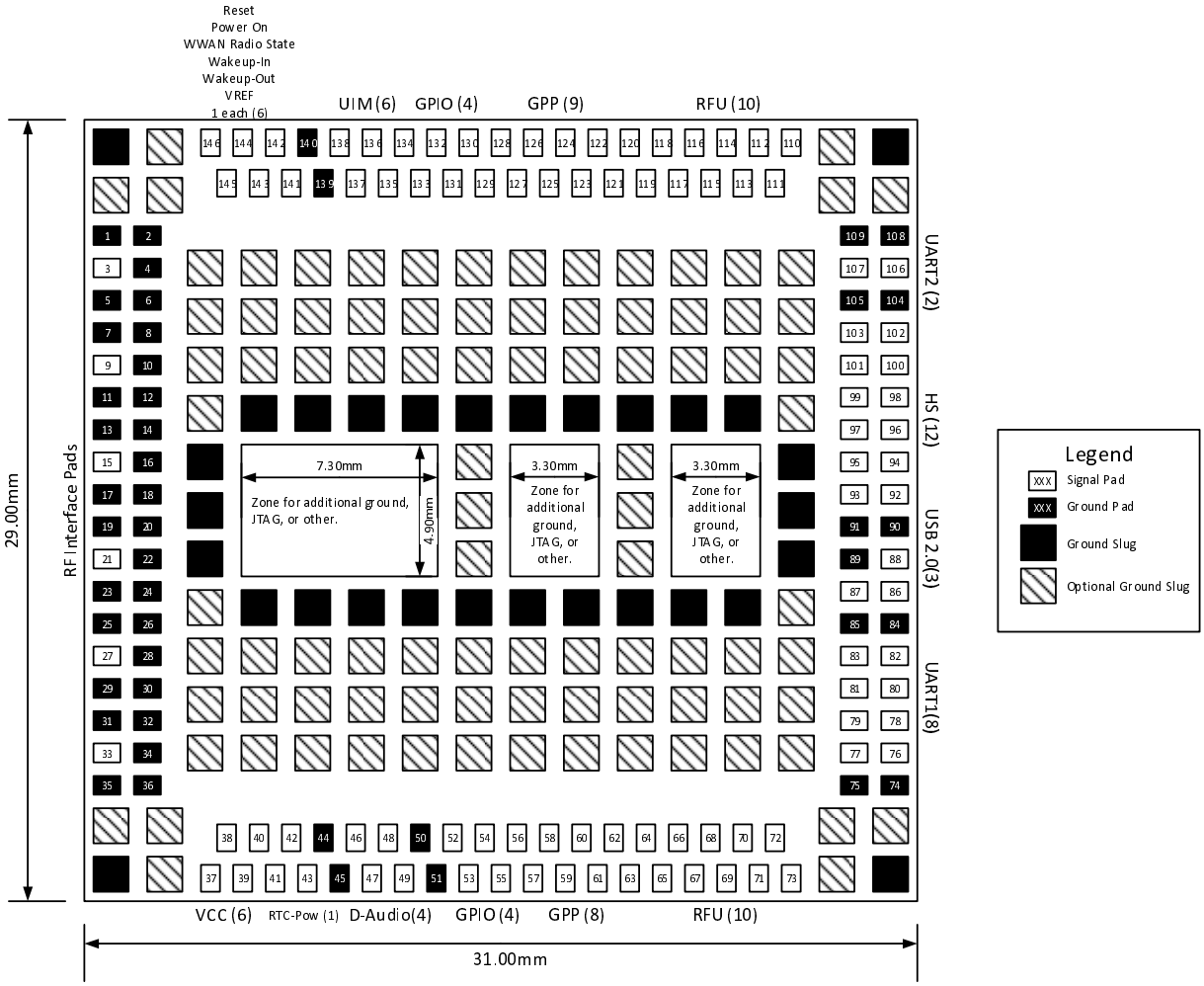

Figure 6: SMT3129 black and white physical form factor (899 mm^2), dimensions, pad numbering and placement

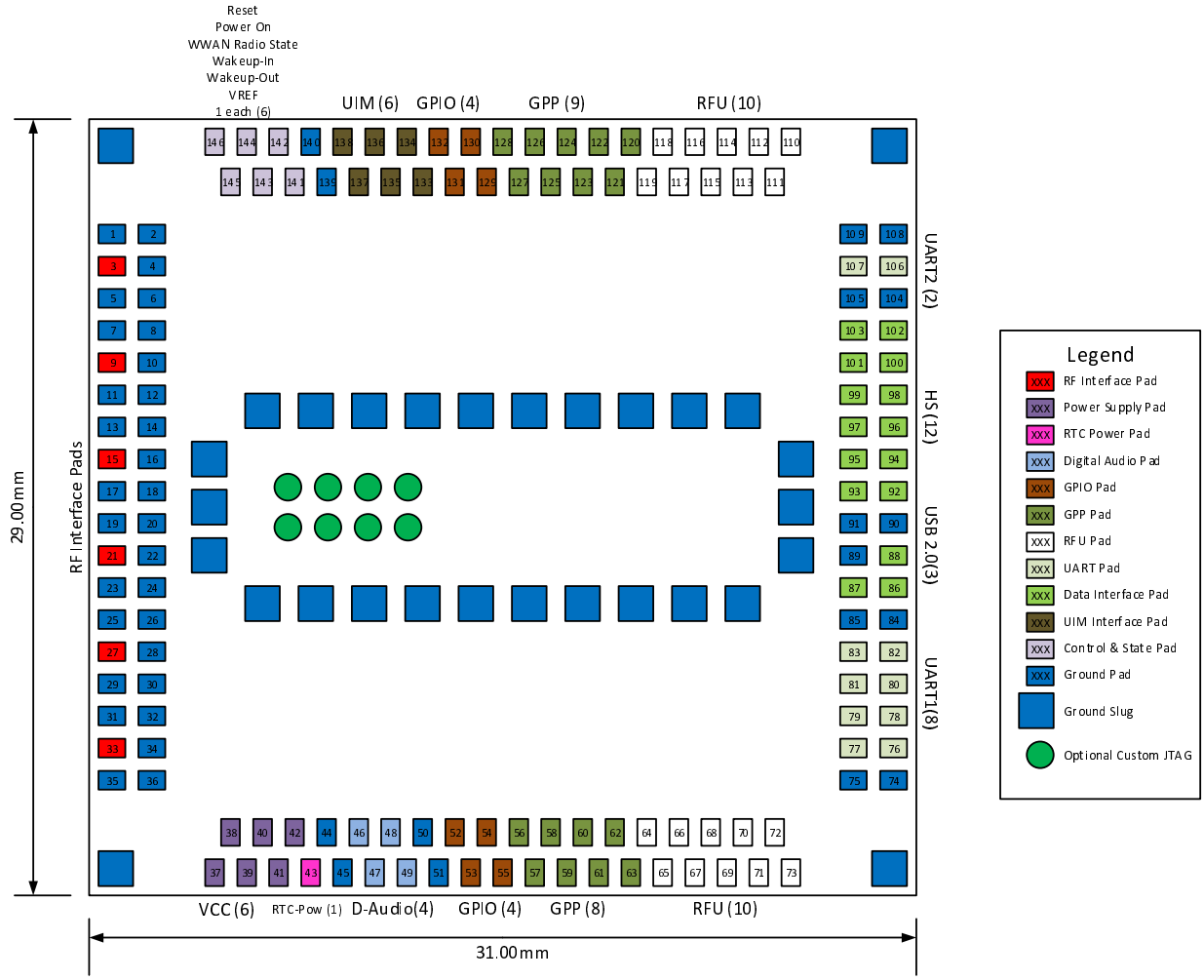

Figure 7: SMT3129 typical physical implementation (899 mm^2), dimensions, pad numbering and placement

4.1.3 SMT3122 Module Mechanical properties

Figures 8, 9 and 10 specify the overall dimensions of the SMT3122 module form factor in millimetres. The form factor provides 146 pads which are numbered 1 through 146.

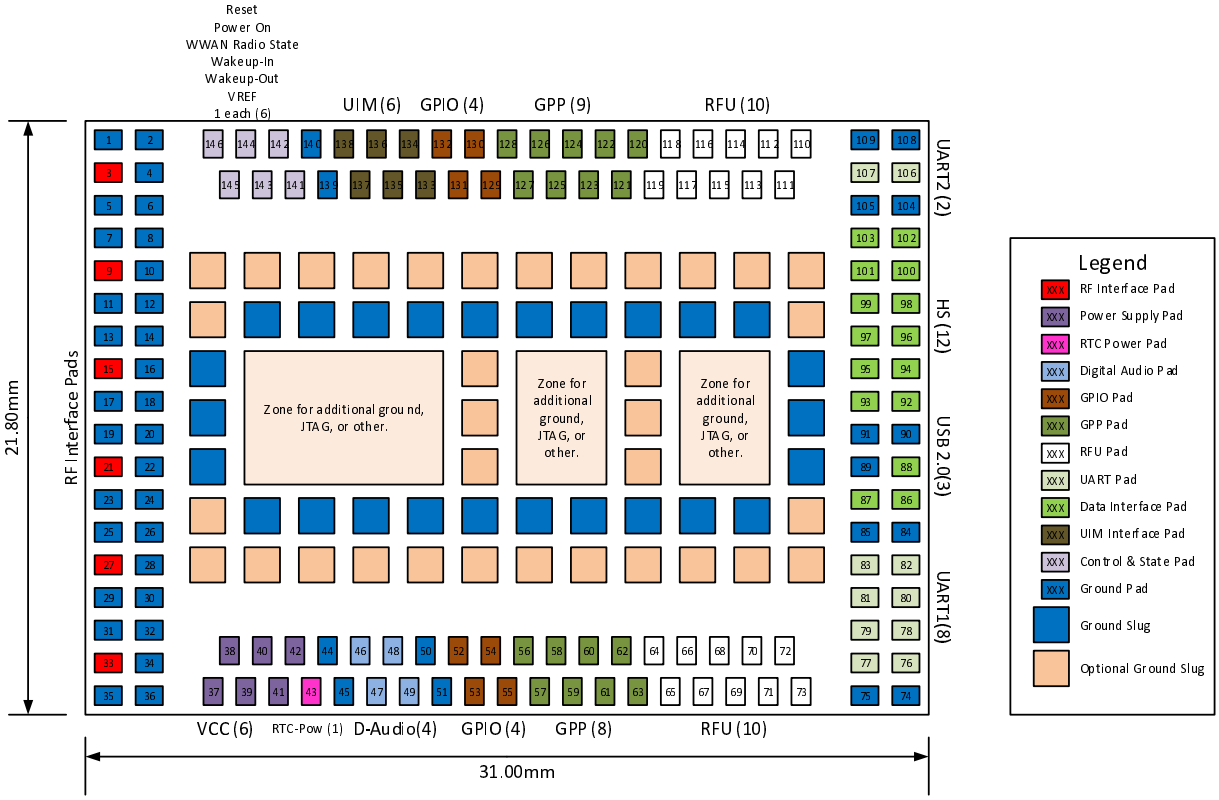

Figure 8: SMT3122 physical form factor (676 mm^2), dimensions, pad numbering and placement

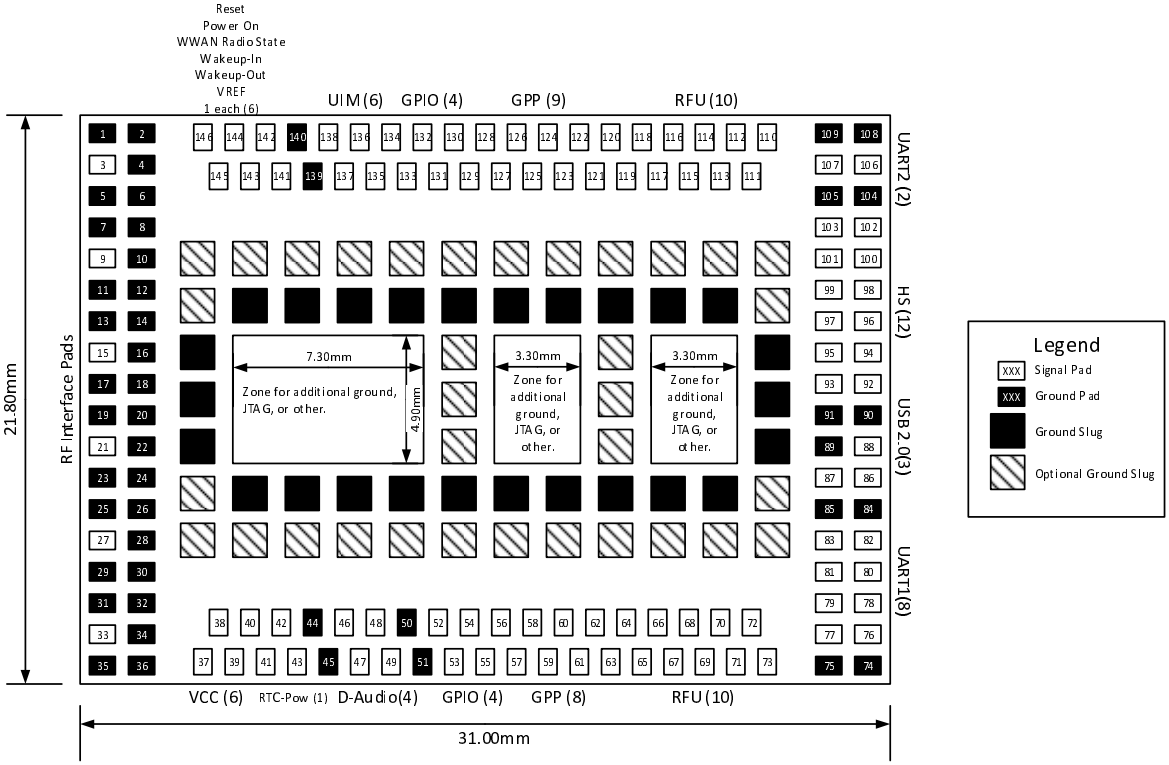

Figure 9: SMT3122 black and white physical form factor (676 mm^2), dimensions, pad numbering and placement

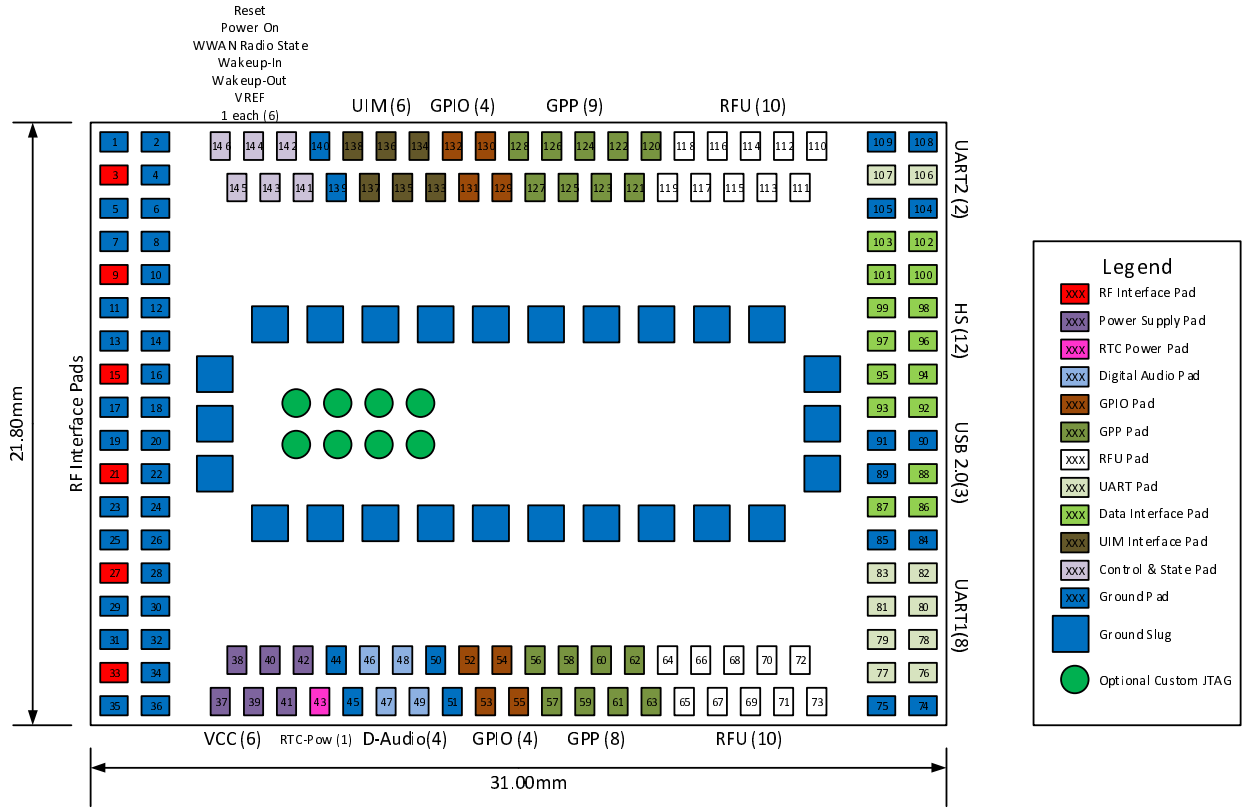

Figure 10: SMT3122 typical physical implementation (676 mm^2), dimensions, pad numbering and placement

4.1.4 SMT3115 Module Mechanical properties

Figures 11, 12, and 13 specify the overall dimensions of the SMT3115 module form factor in millimetres. The form factor provides 122 pads which are numbered 1 through 73, 80 through 103 and 110 through 146.

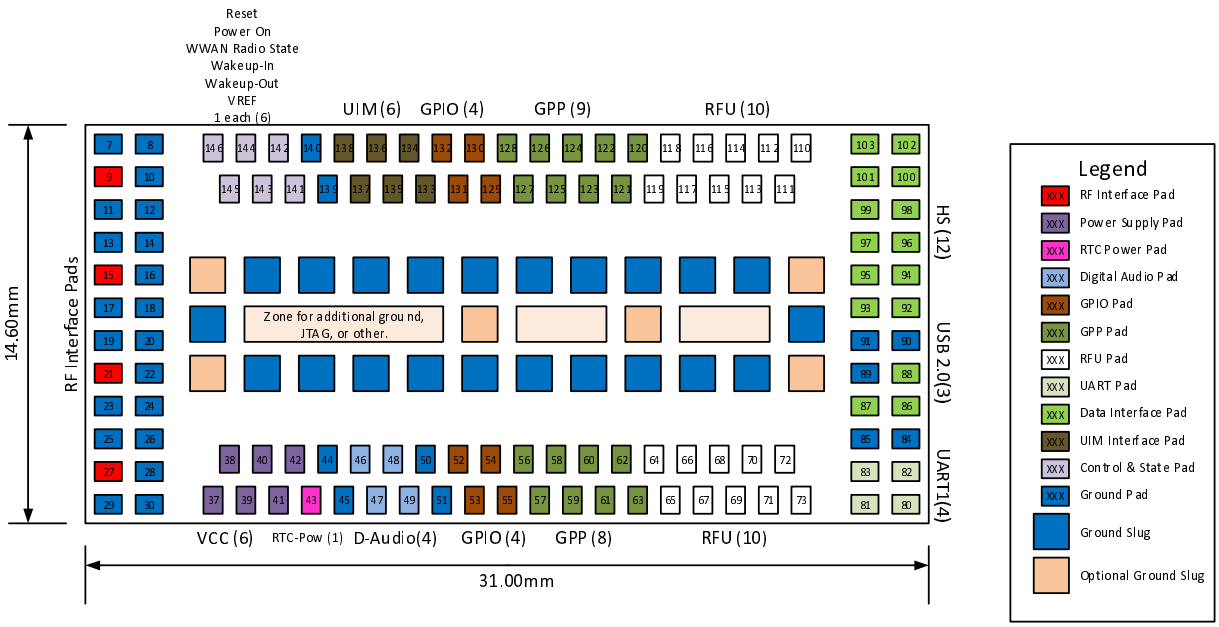

Figure 11: SMT3115 physical form factor (452 mm^2), dimensions, pad numbering and placement

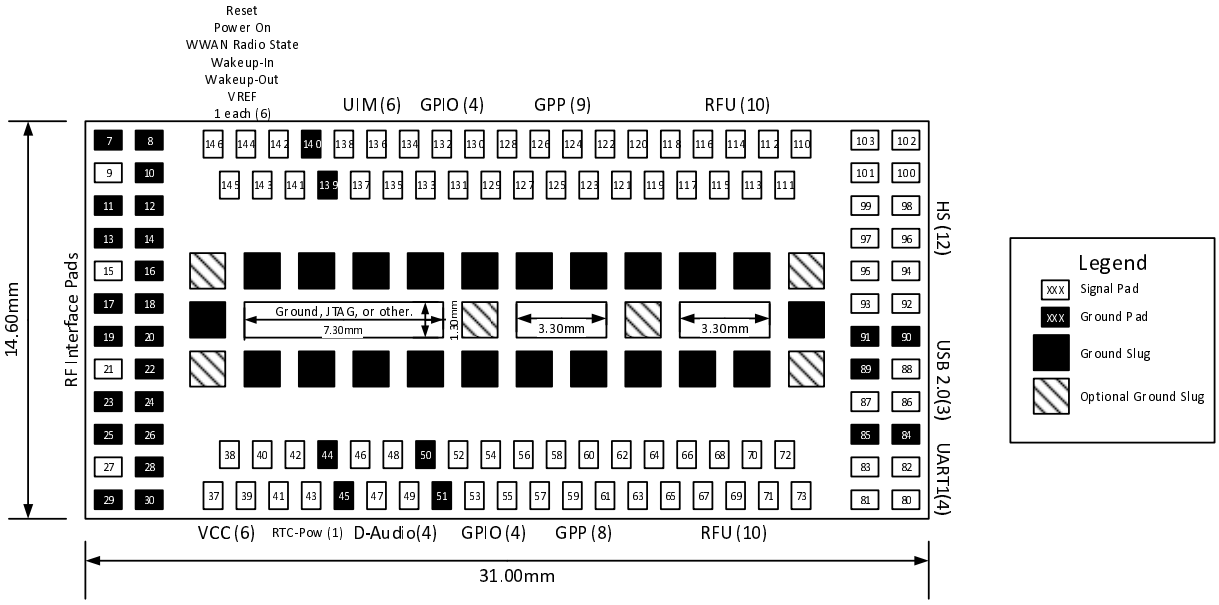

Figure 12: SMT3115 black and white physical form factor (452 mm^2), dimensions, pad numbering and placement

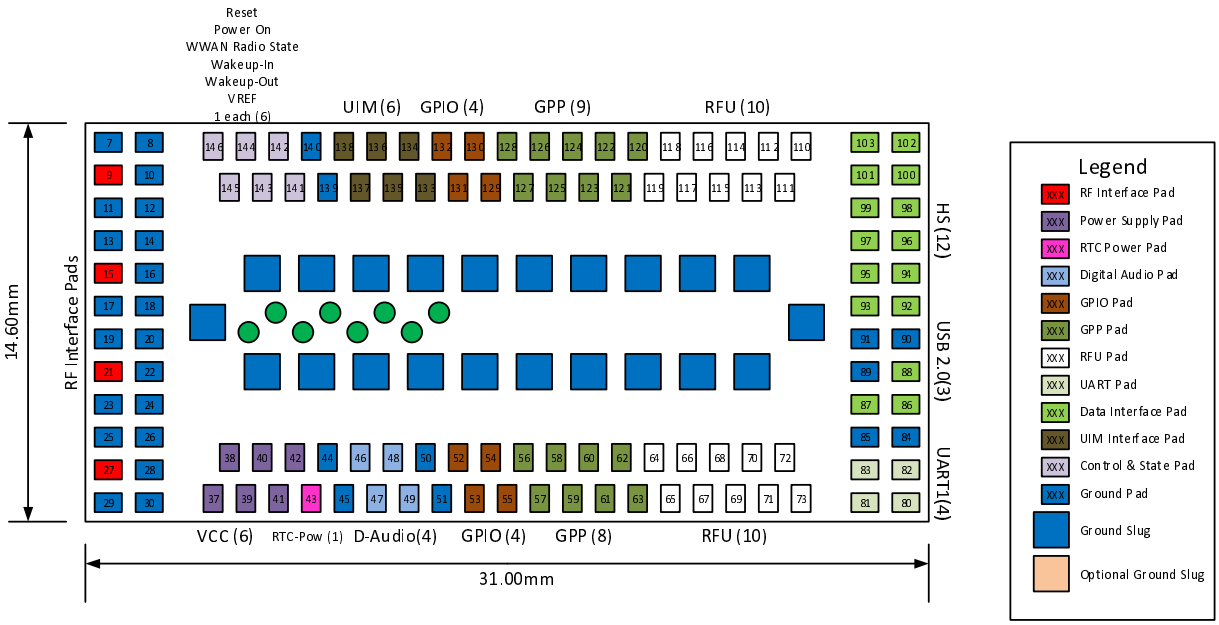

Figure 13: SMT3115 typical physical implementation (452 mm^2), dimensions, pad numbering and placement

4.1.5 SMT3729 Module Mechanical properties

Figures 14, 15 and 16 specify the overall dimensions of the SMT3729 module form factor in millimetres. The form factor provides 166 pads which are numbered 1 through 166.

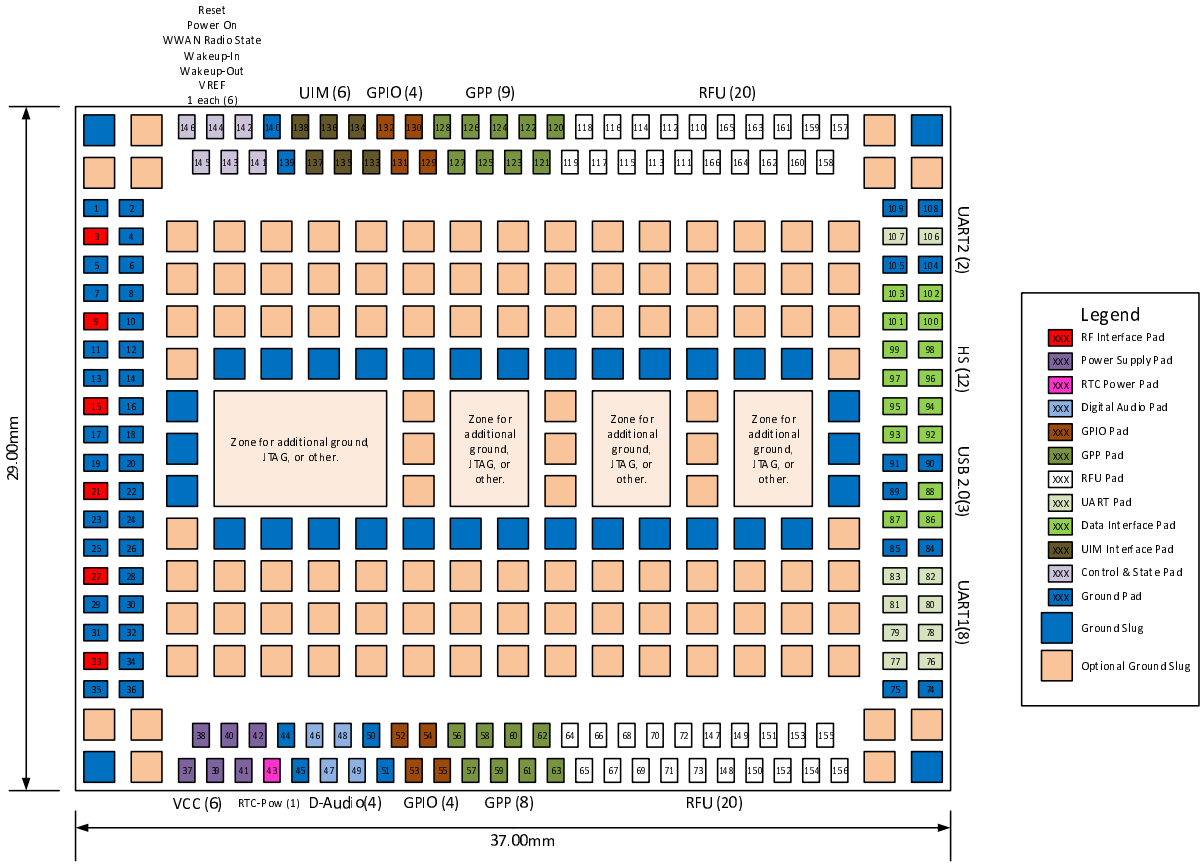

Figure 14: SMT3729 physical form factor (1 073 mm^2), dimensions, pad numbering and placement

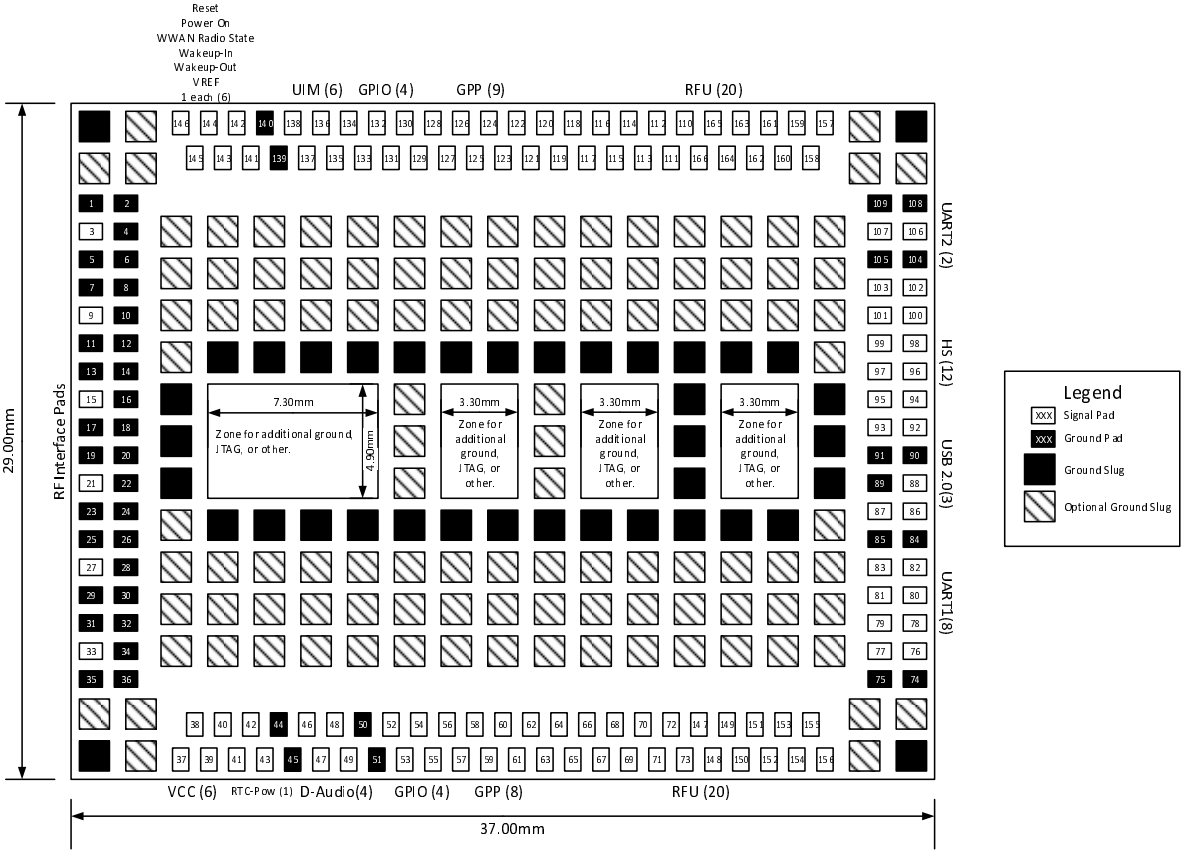

Figure 15: SMT3729 black and white physical form factor (1 073 mm^2), dimensions, pad numbering and placement

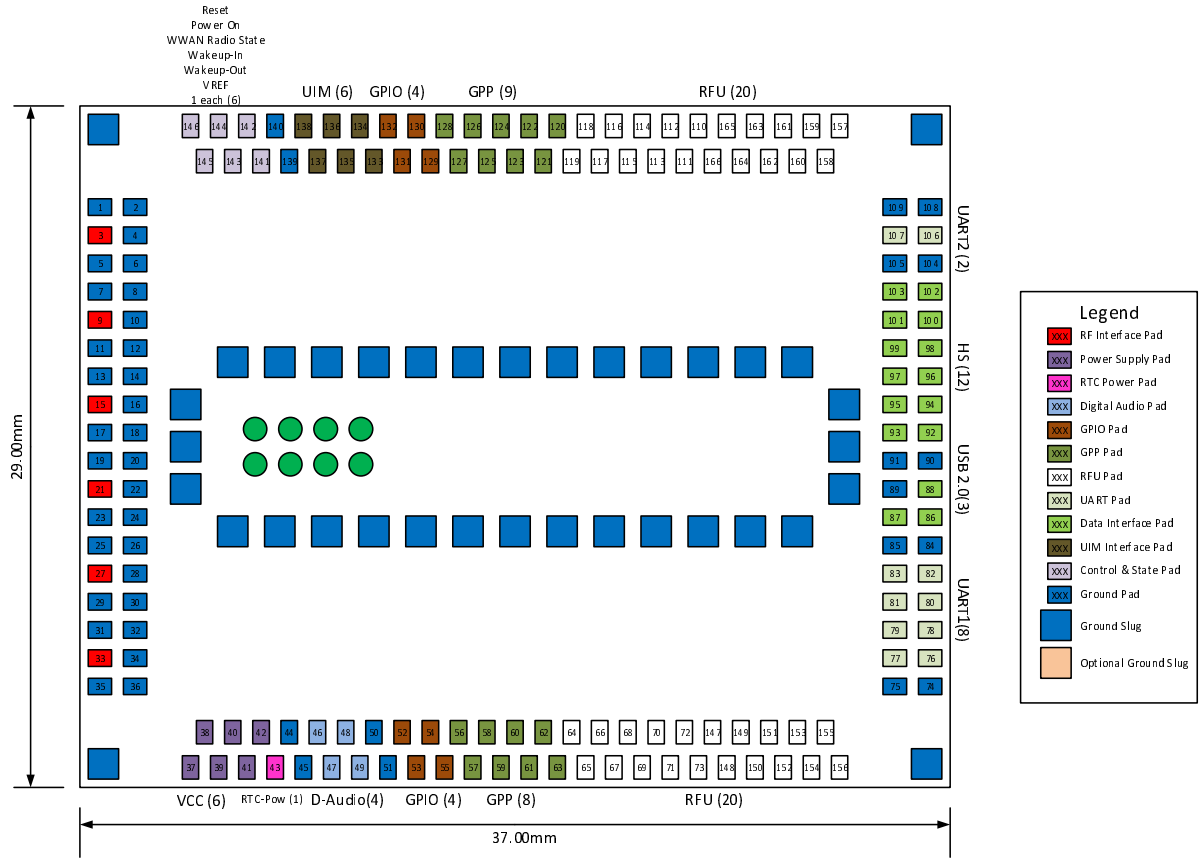

Figure 16: SMT3729 typical physical implementation (1 073 mm^2), dimensions, pad numbering and placement

4.1.6 SMT3722 Module Mechanical properties

Figures 17, 18 and 19 specify the overall dimensions of the SMT3722 module form factor in millimetres. The form factor provides 166 pads which are numbered 1 through 166.

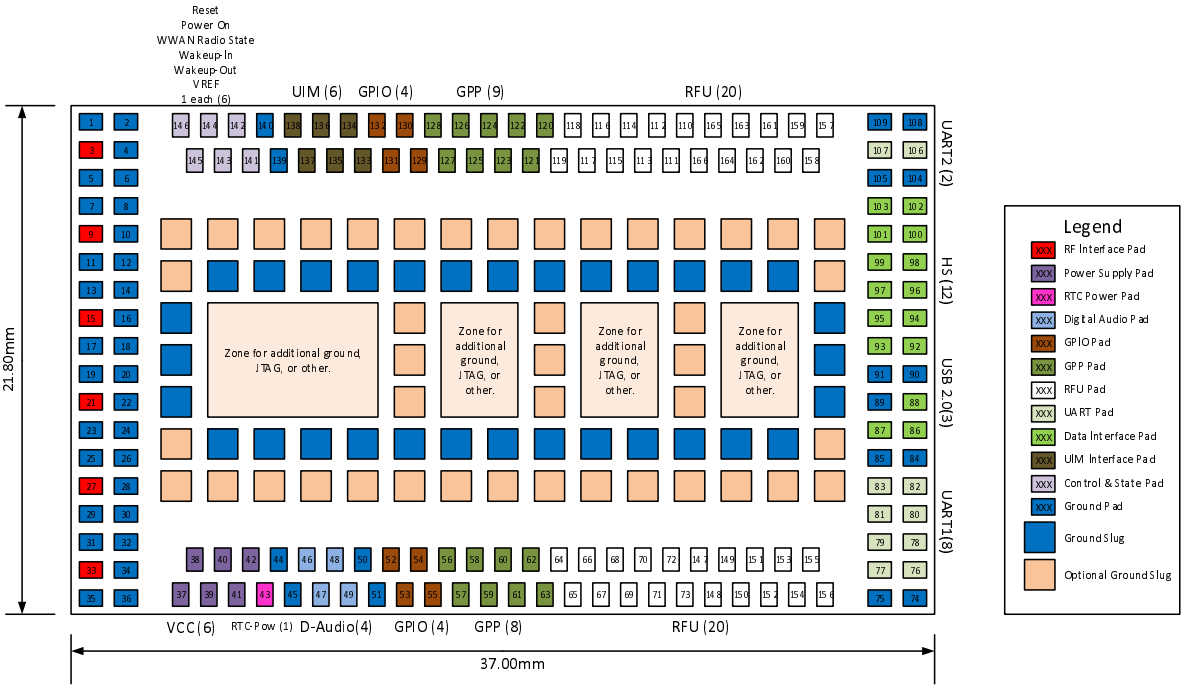

Figure 17: SMT3722 physical form factor (807 mm^2), dimensions, pad numbering and placement

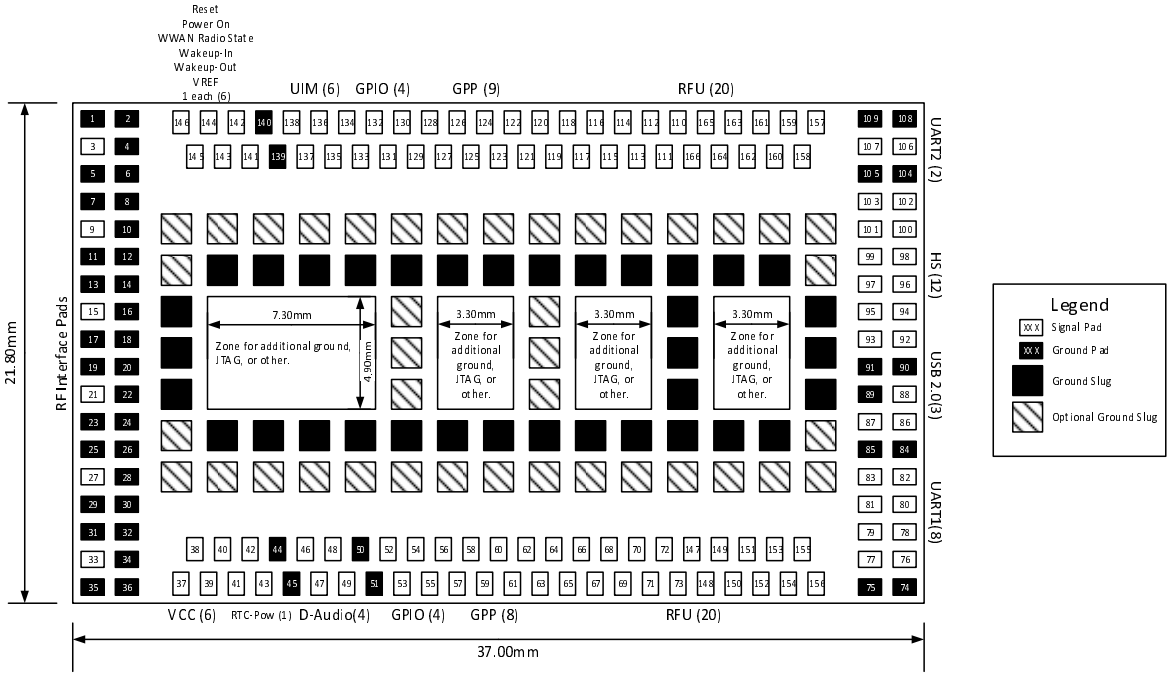

Figure 18: SMT3722 black and white physical form factor (807 mm^2), dimensions, pad numbering and placement

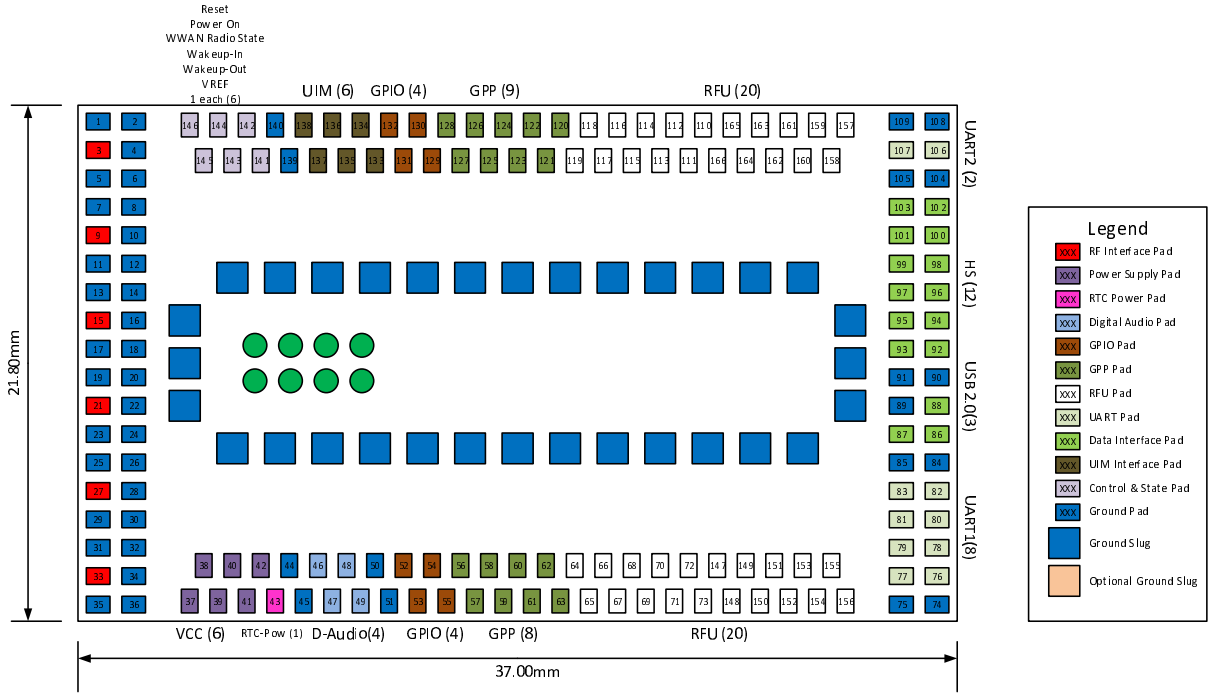

Figure 19: SMT3722 typical physical implementation (807 mm^2), dimensions, pad numbering and placement

4.1.7 SMT2522 Module Mechanical properties

Figures 20, 21, 22 and 23 specify the overall dimensions of the SMT2522 module form factor in millimetres. The form factor provides 126 pads which are numbered 1 through 63, 74 through 109 and 120 through 146.

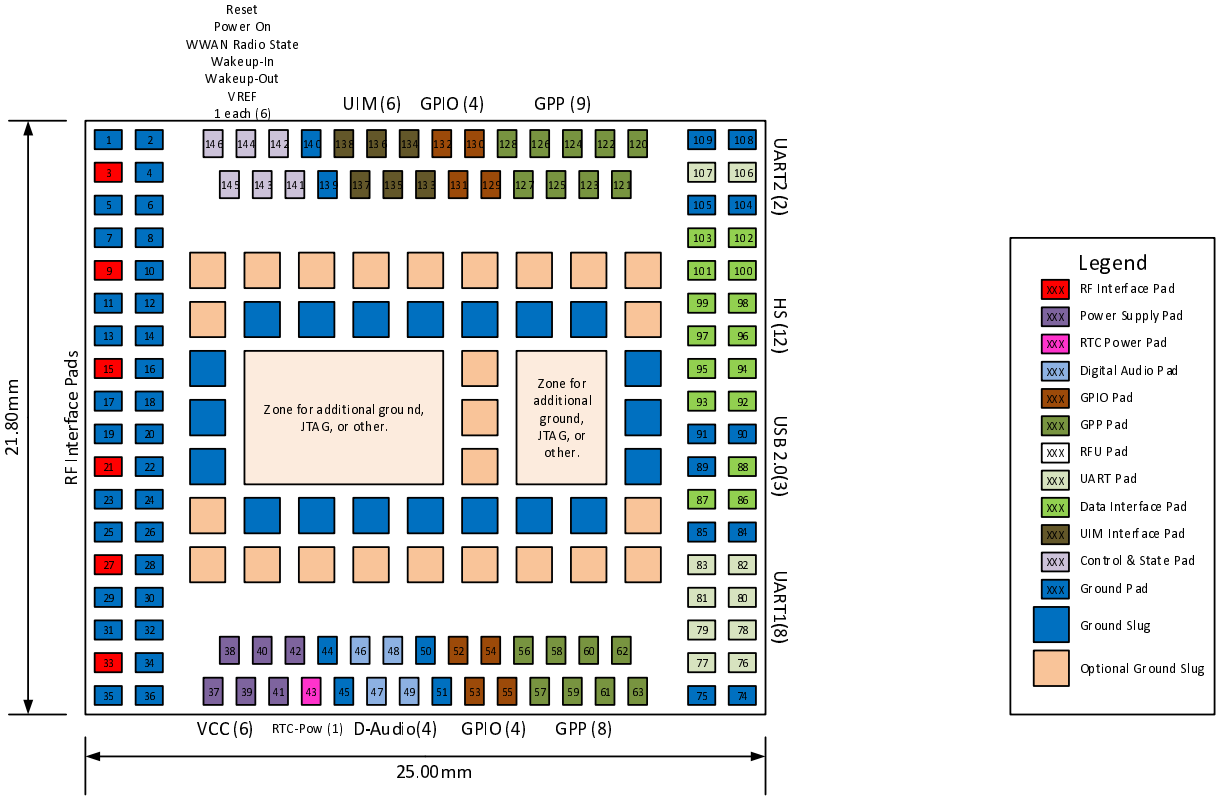

Figure 20: SMT2522 physical form factor (545 mm^2), dimensions, pad numbering and placement

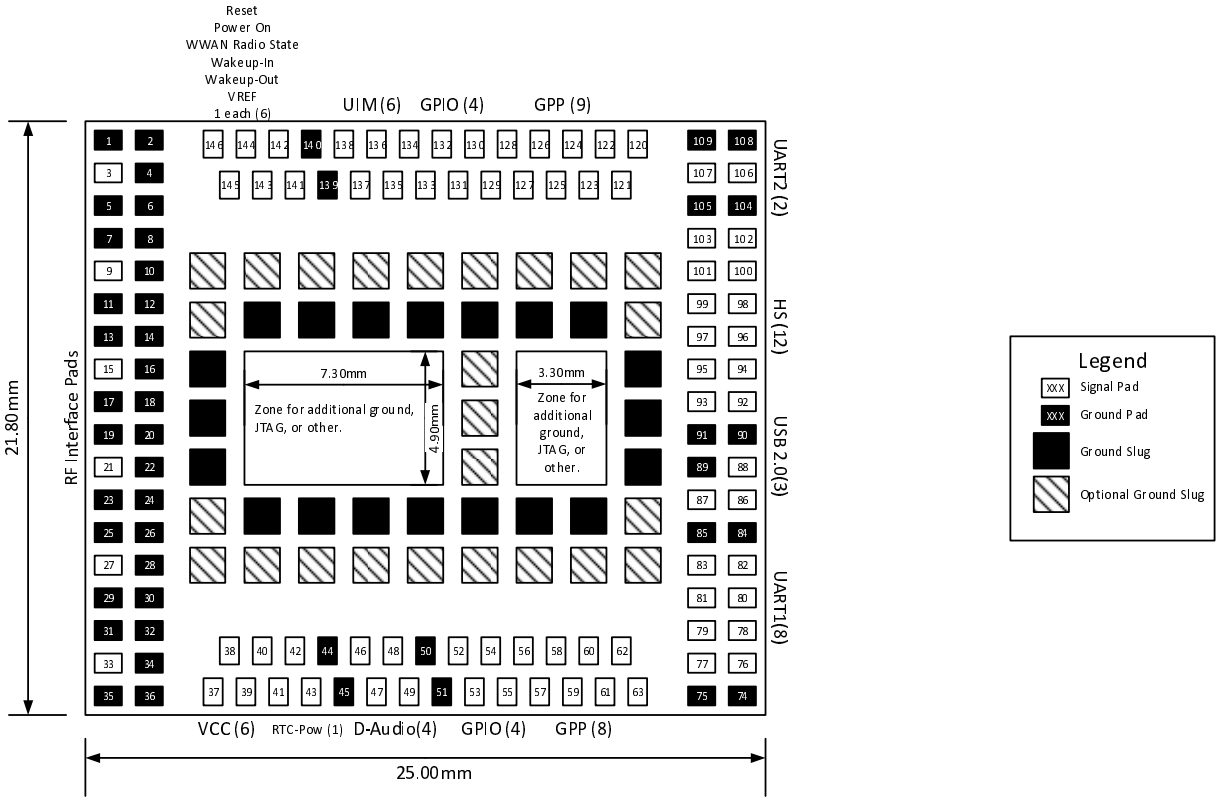

Figure 21: SMT2522 black and white physical form factor (545 mm^2), dimensions, pad numbering and placement

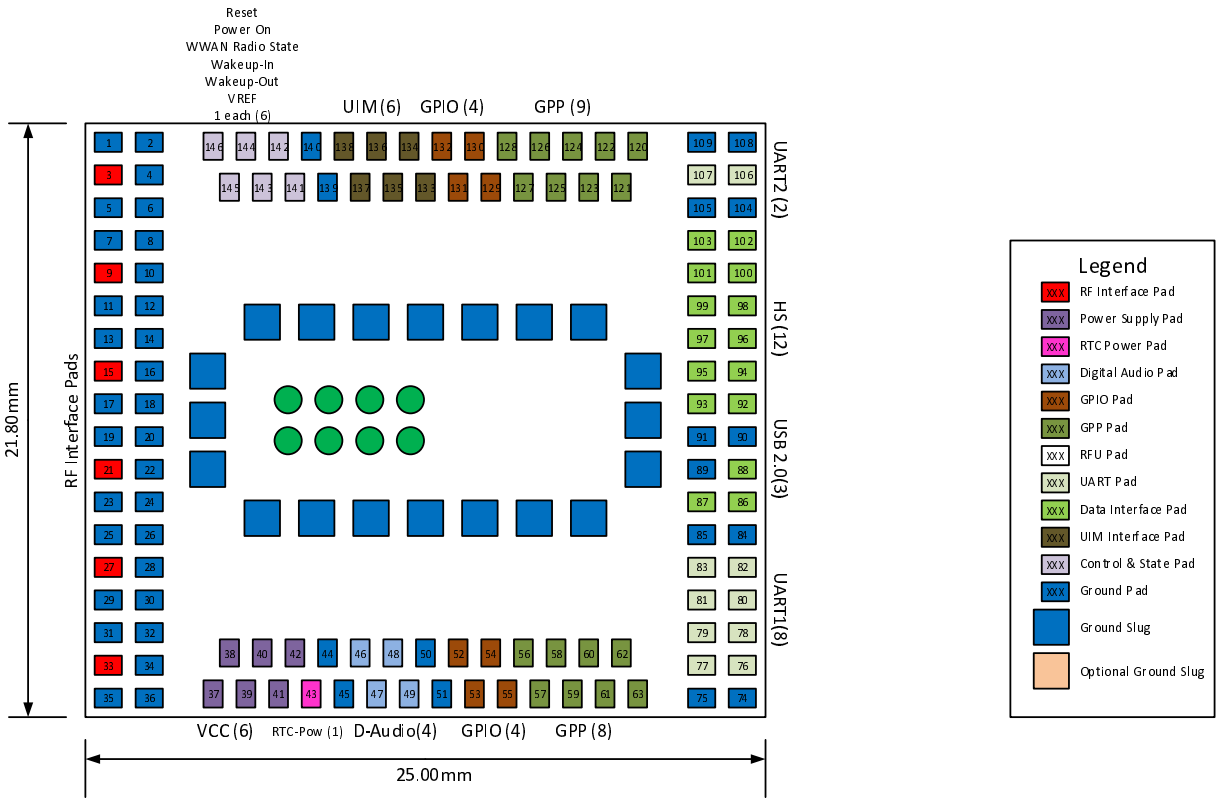

Figure 22: SMT2522 typical physical implementation (545 mm^2), dimensions, pad numbering and placement

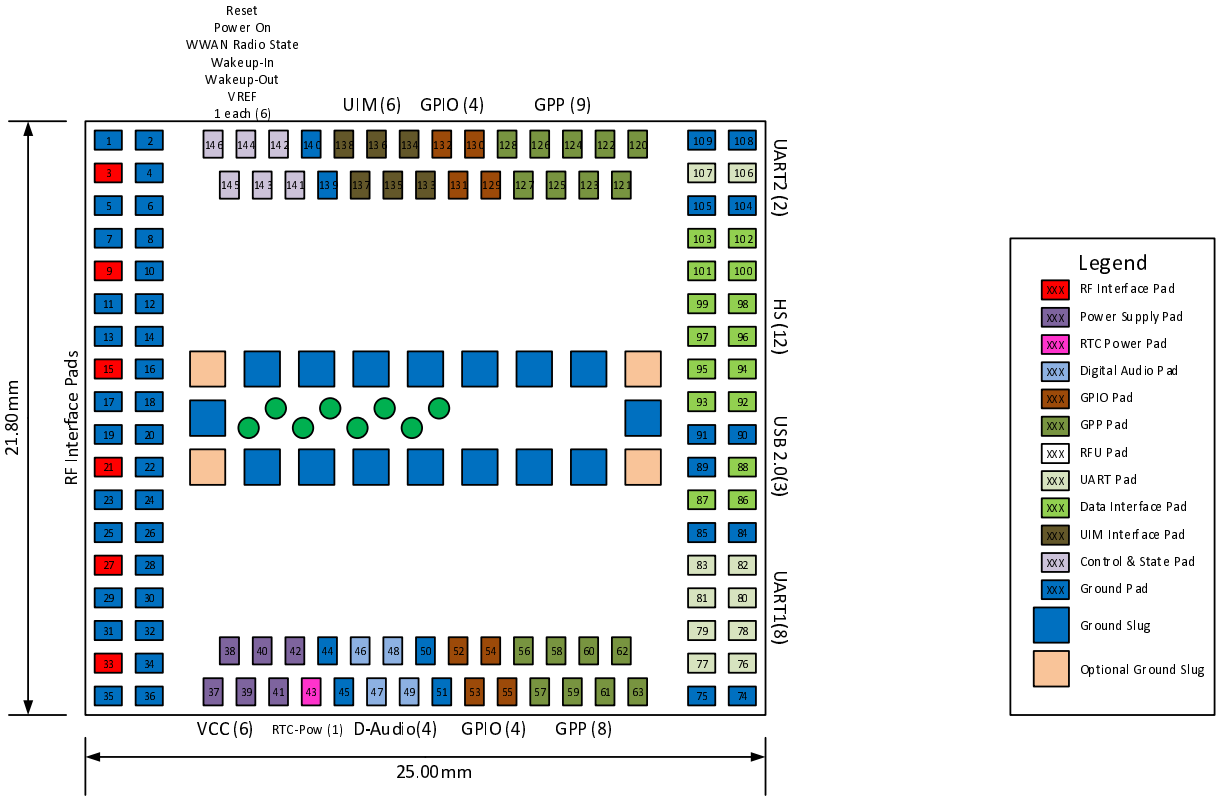

Figure 23: SMT2522 for nesting with a SMT2515

4.1.8 SMT2515 Module Mechanical properties

Figures 24, 25 and 26 specify the overall dimensions of the SMT2515 module form factor in millimetres. The form factor provides 102 pads which are numbered 7 through 30, 37 through 63, 80 through 103 and 120 through 146.

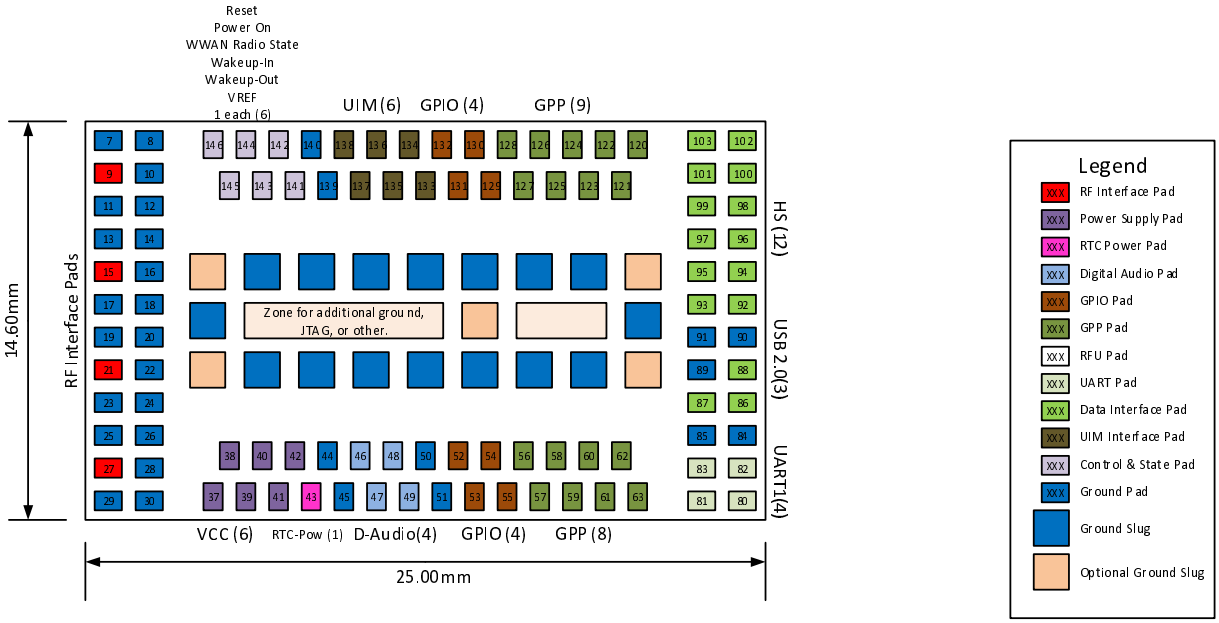

Figure 24: SMT2515 physical form factor (365 mm^2), dimensions, pad numbering and placement

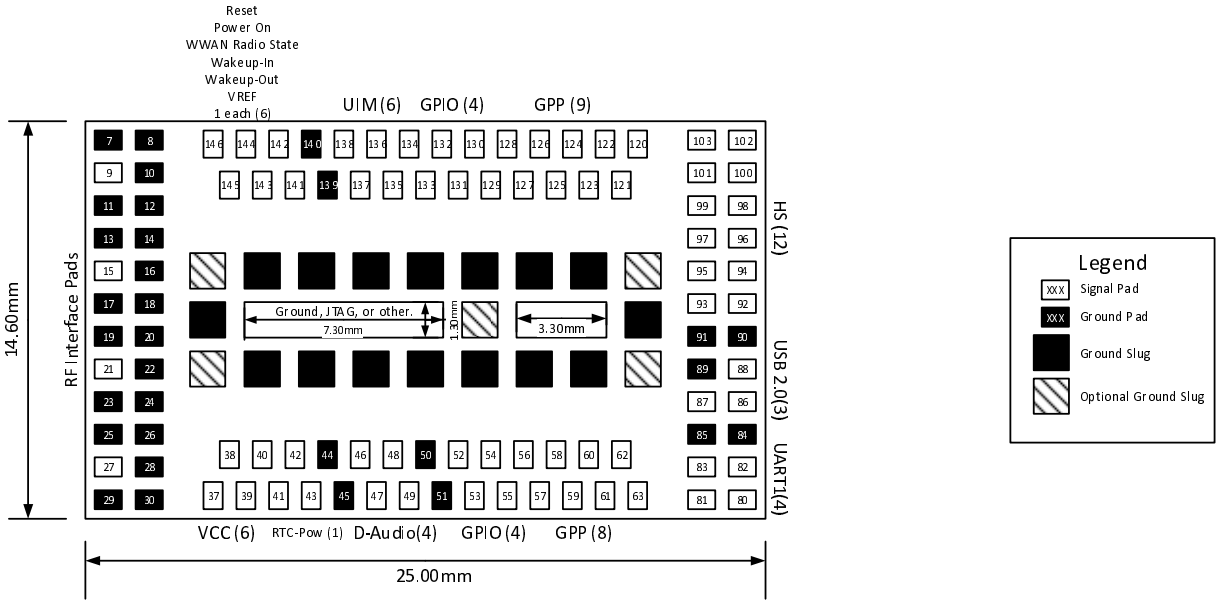

Figure 25: SMT2515 black and white physical form factor (365 mm^2), dimensions, pad numbering and placement

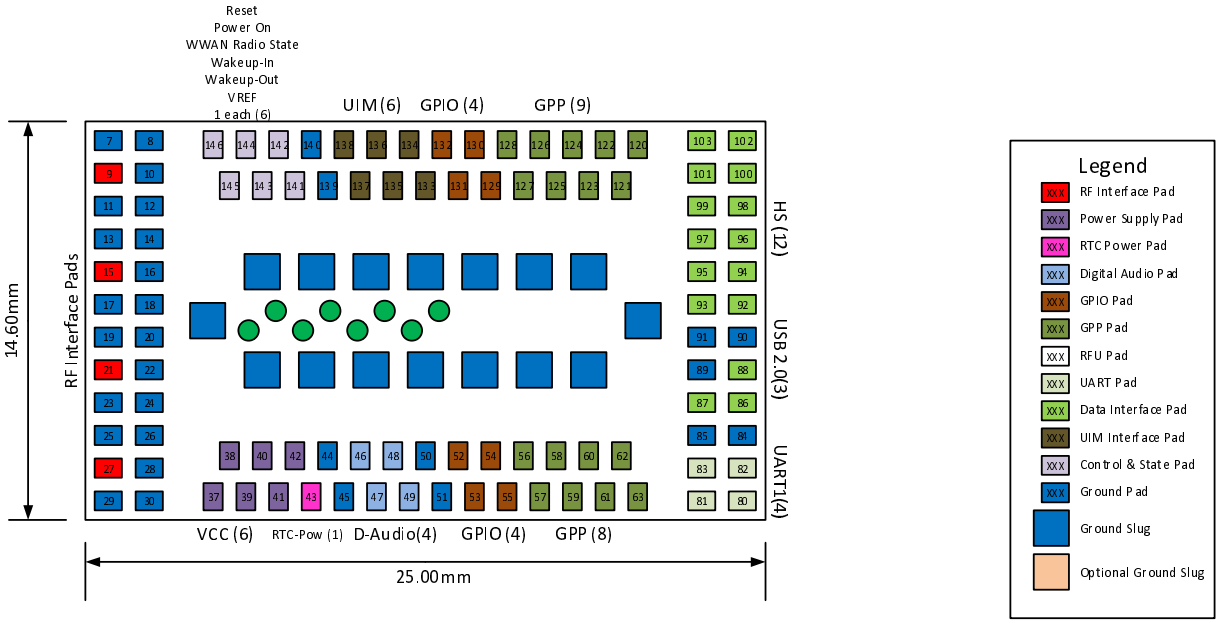

Figure 26: SMT2515 typical physical implementation (365 mm^2), dimensions, pad numbering and placement

4.1.9 SMT1922 Module Mechanical properties

Figures 27, 28 and 29 specify the overall dimensions of the SMT1922 module form factor in millimetres. The form factor provides a maximum number of 106 pads which are numbered 1 through 53, 74 through 109 and 130 through 146.

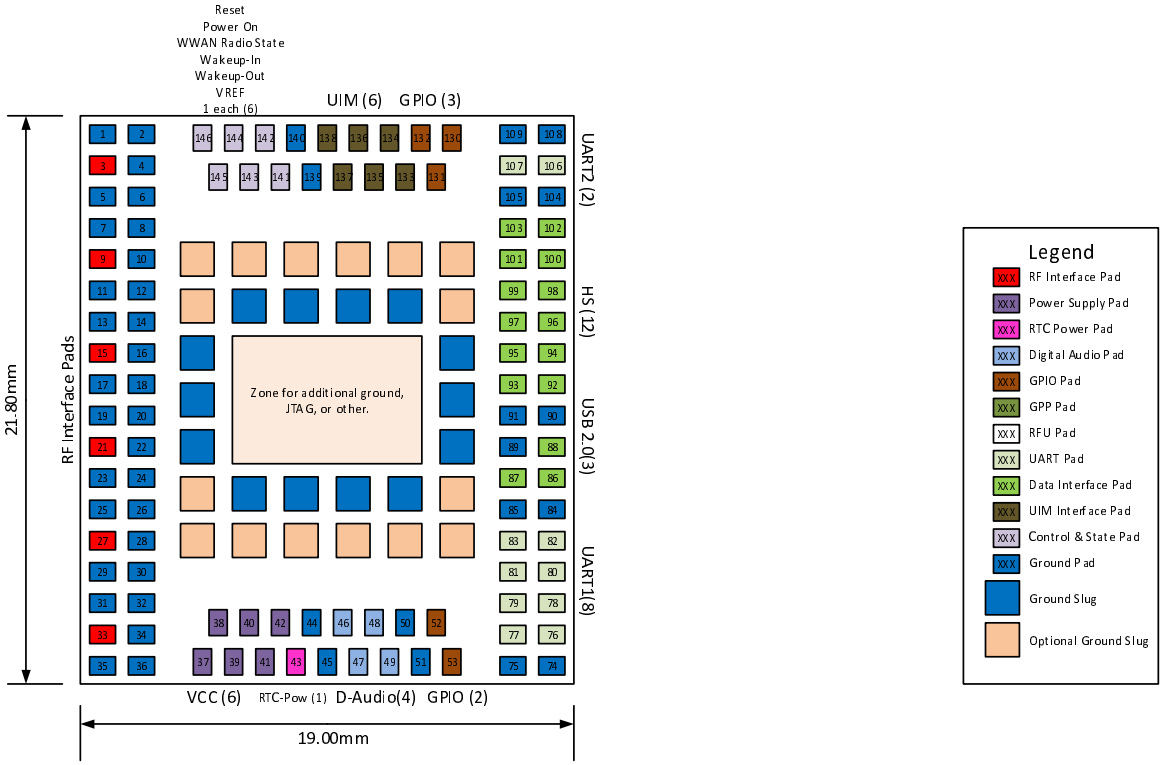

Figure 27: SMT1922 physical form factor (414 mm^2), dimensions, pad numbering and placement

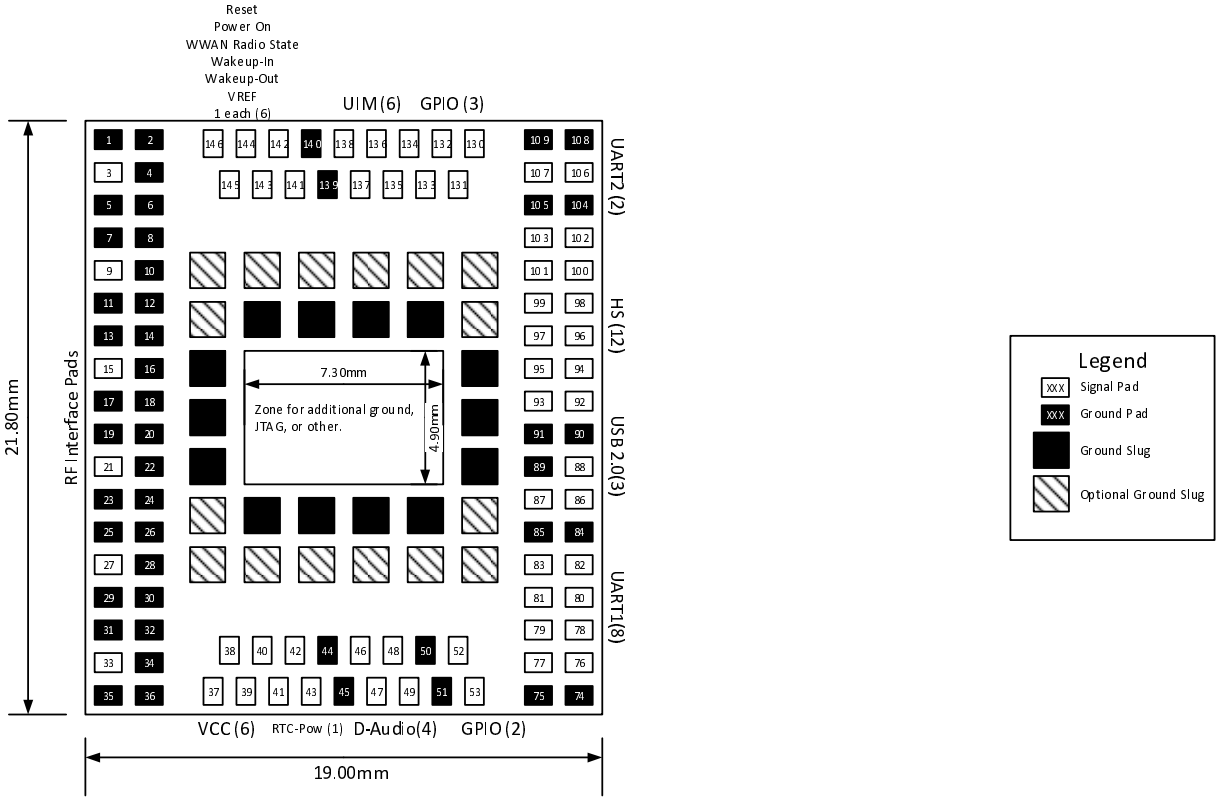

Figure 28: SMT1922 black and white physical form factor (414 mm^2), dimensions, pad numbering and placement

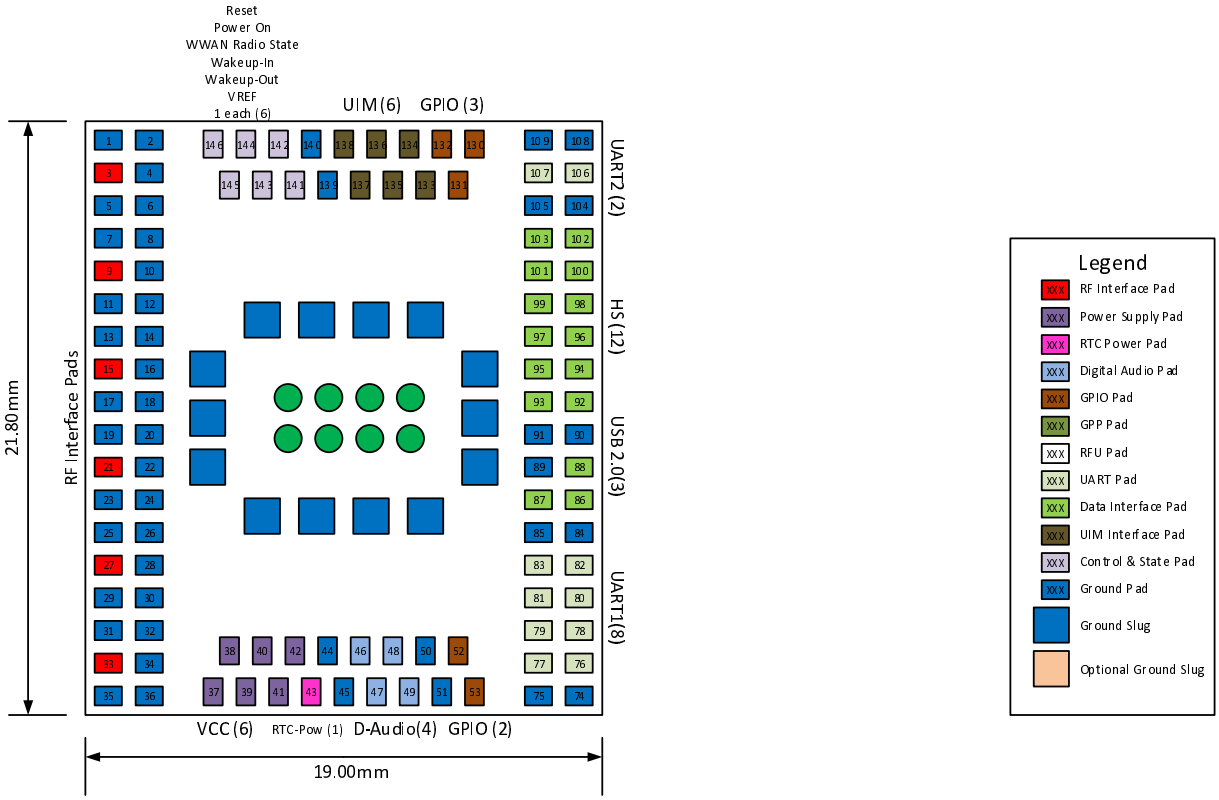

Figure 29: SMT1922 typical physical implementation (414 mm^2), dimensions, pad numbering and placement

4.1.10 SMT1915 Module Mechanical properties

Figures 30, 31 and 32 specify the overall dimensions of the SMT1915 module form factor in millimetres. The typical form factor provides 82 pads which are numbered 7 through 30, 37 through 53, 80 through 103 and 130 through 146. The minimal implementation supports 58 pads as shown in Figure 33.

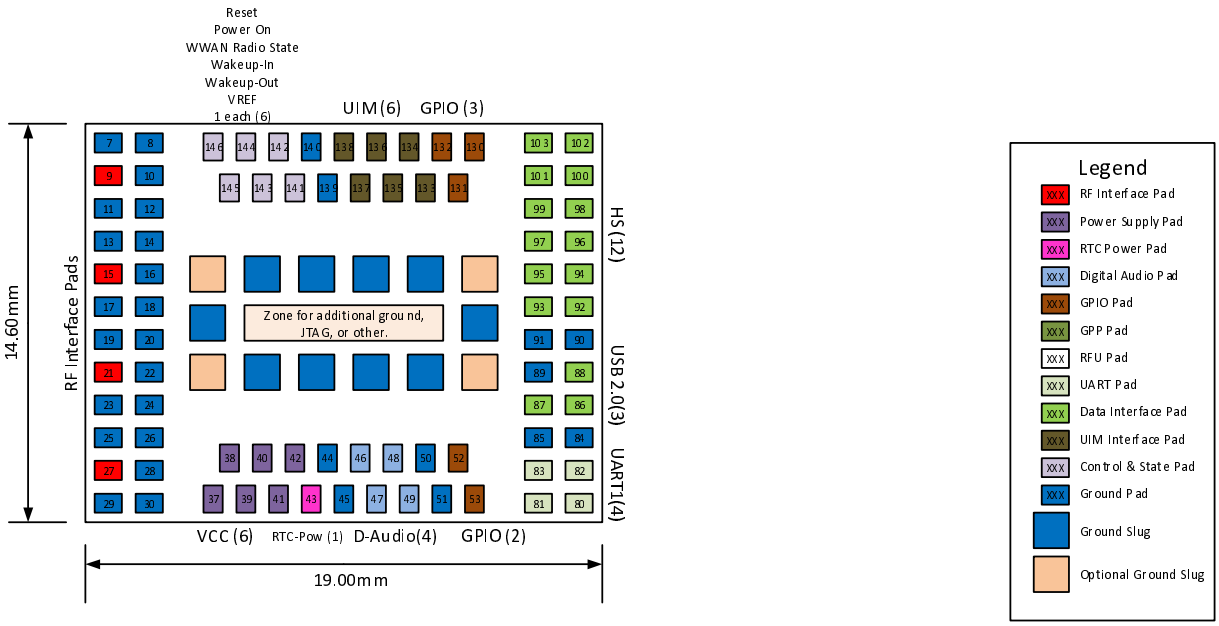

Figure 30: SMT1915 physical form factor (277 mm^2), dimensions, pad numbering and placement

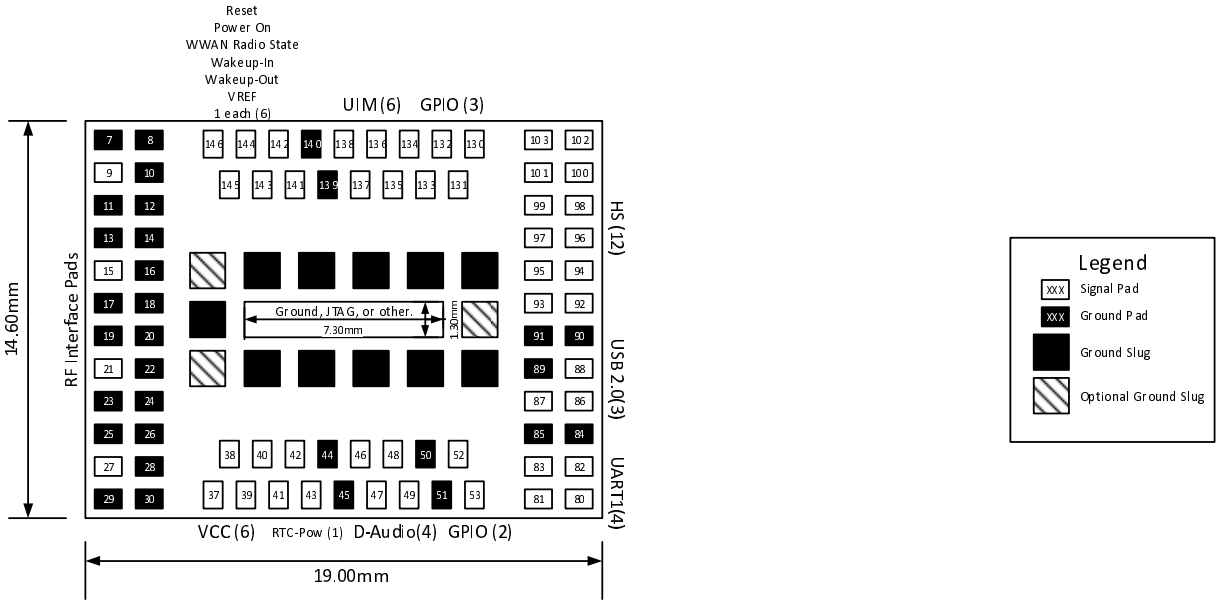

Figure 31: SMT1915 black and white physical form factor (277 mm^2), dimensions, pad numbering and placement

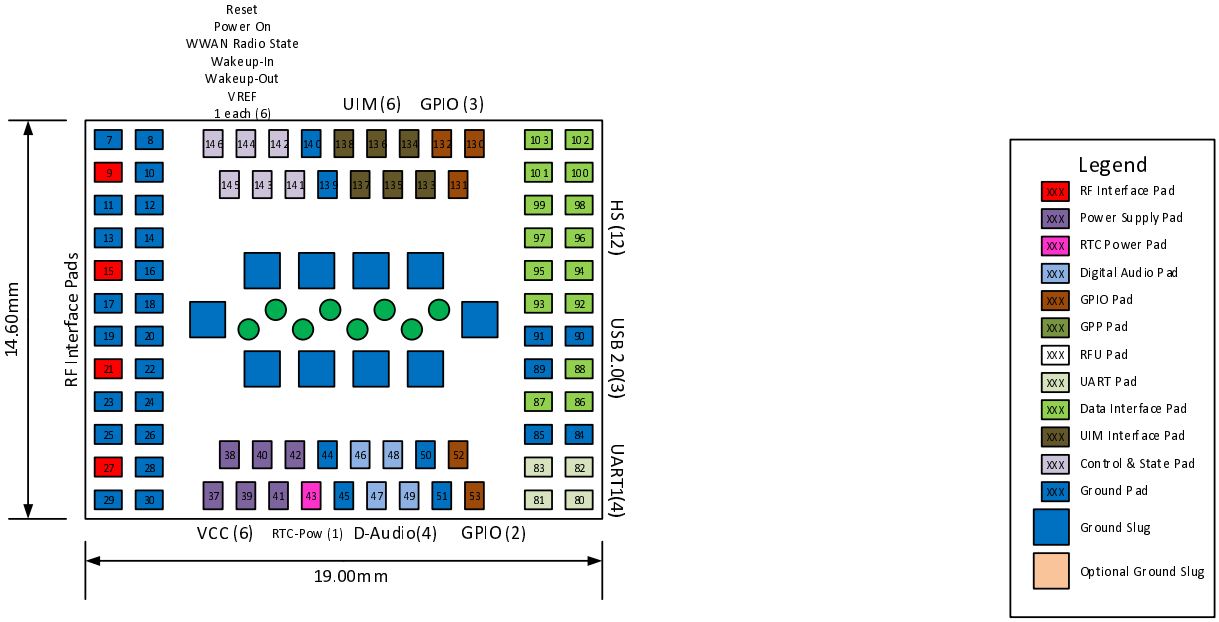

Figure 32: SMT1915 typical physical implementation (277 mm^2), dimensions, pad numbering and placement

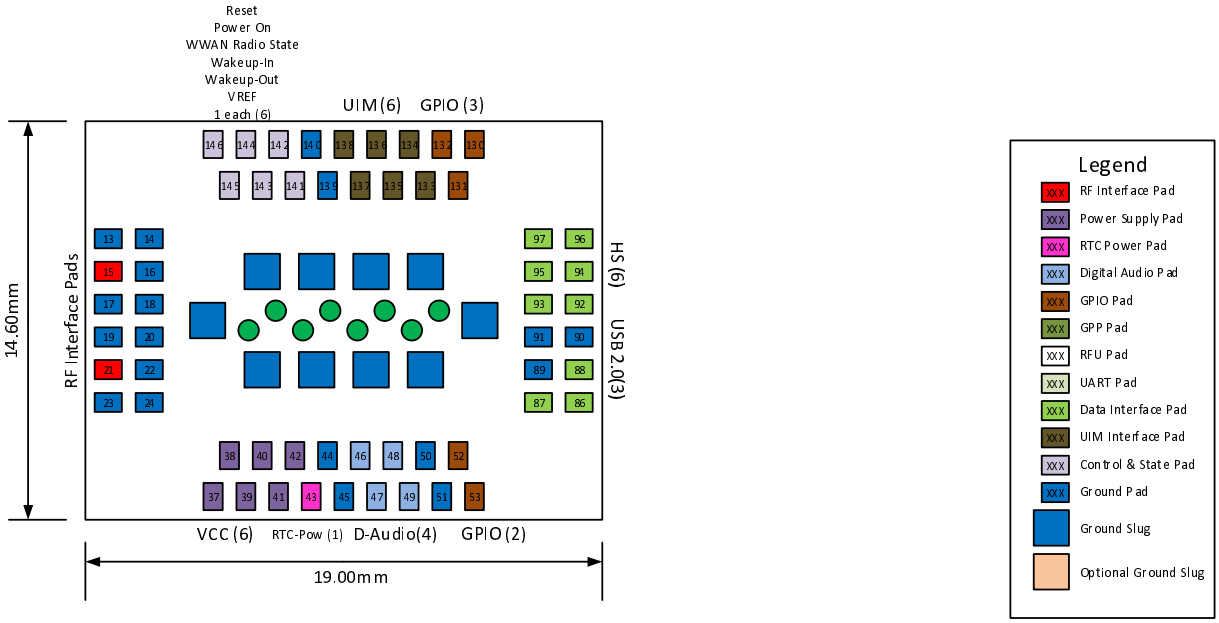

Figure 33: SMT1915 minimal pad implementation (277 mm^2), dimensions, pad numbering and placement

4.2 Pad Size and Spacing

Figures 34, 35 and 36 show the dimensions of the pads, the distance between pads and the distance between the pads and the edge of the module. The module is symmetric with respect to the placement of the pads on each side. All measurements are in mm.

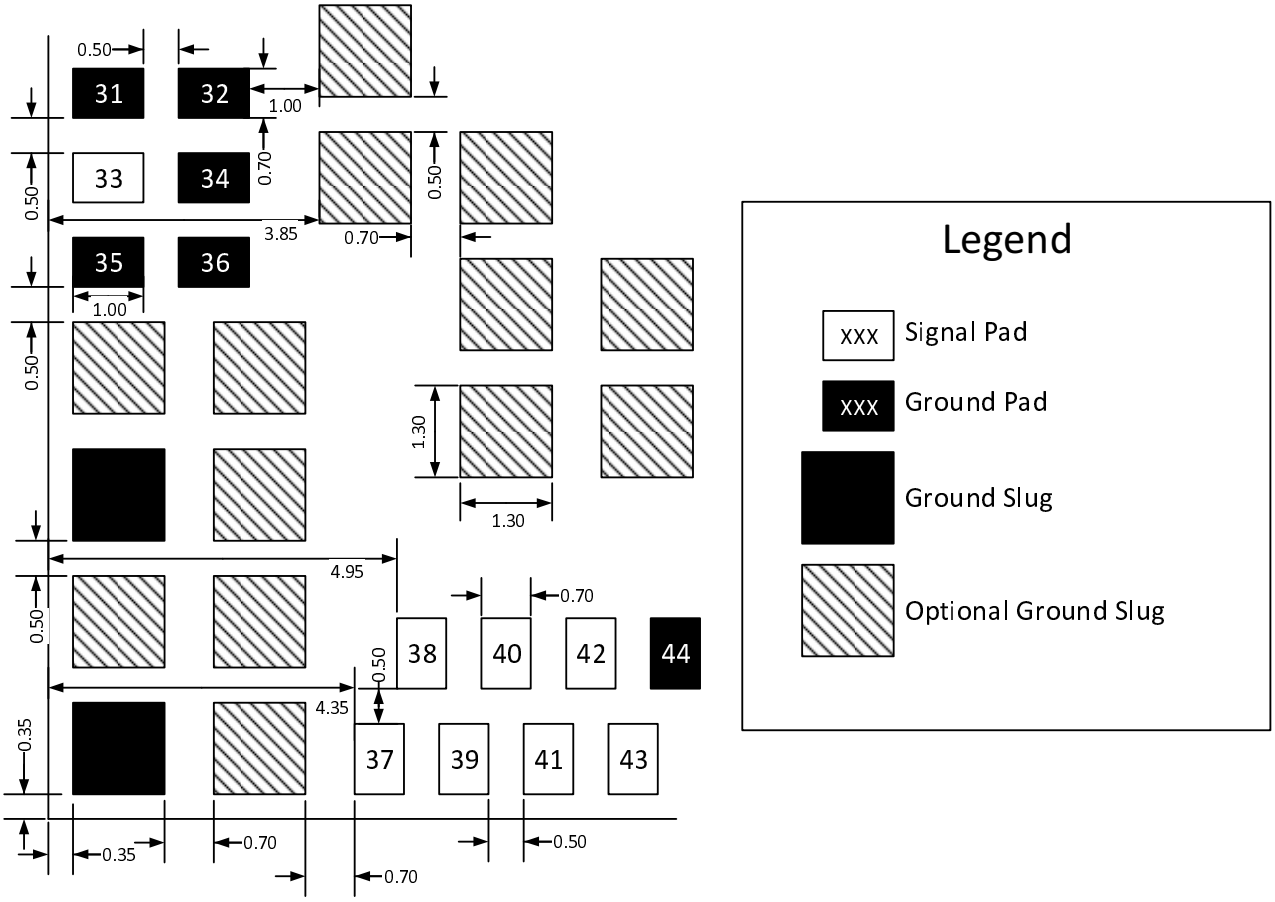

Figure 34: SMT3136 Pad Size and Spacing

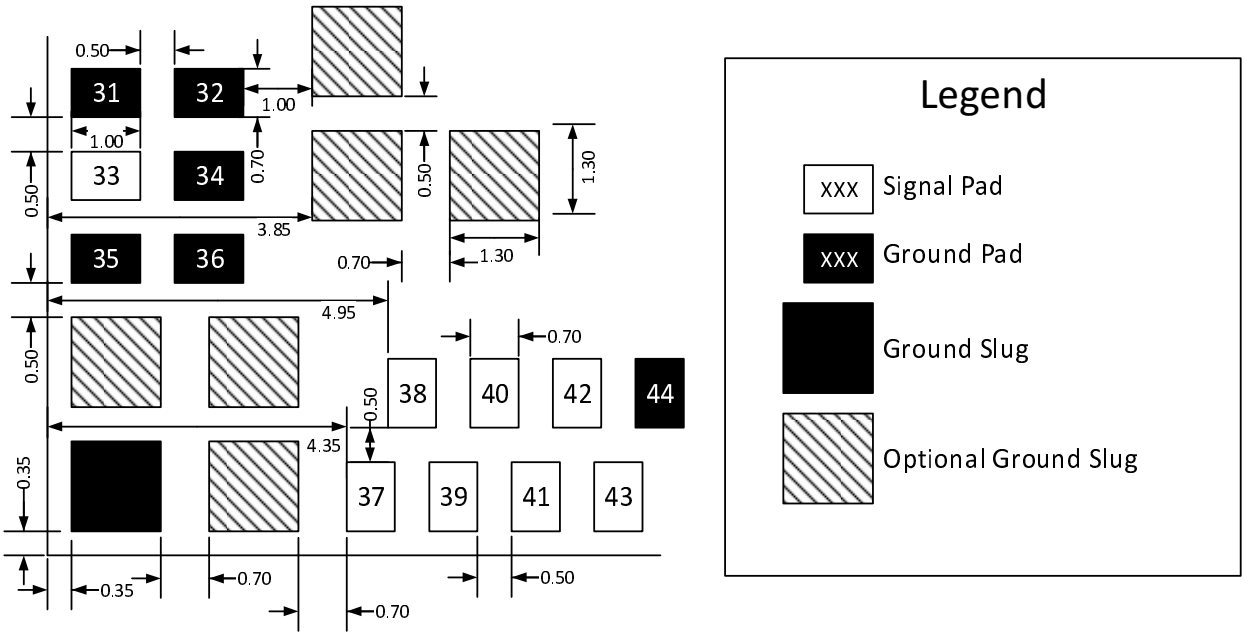

Figure 35: SMT3129, SMT3729 Pad Size and Spacing

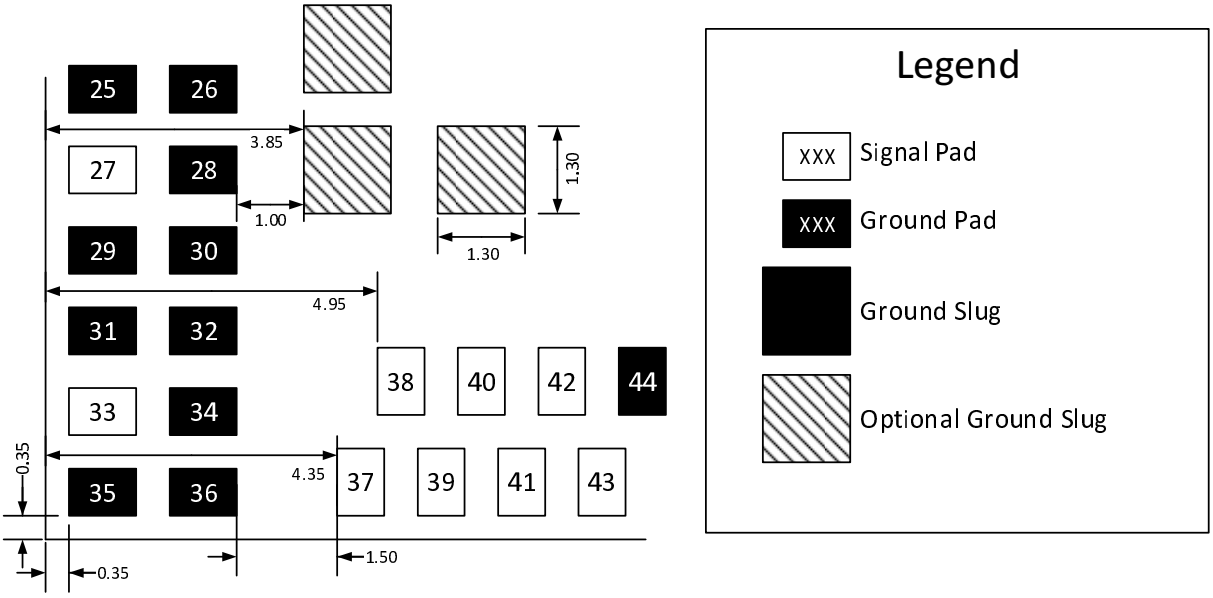

Figure 36: SMT3122, SMT3115, SMT3722, SMT2522, SMT2515, SMT1922 & SMT1915 Pad Size and Spacing

4.3 Pad Assignments

This clause specifies which interfaces are assigned to which pads. Each module in the present document leverages the same pad numbering assignment. The electrical characteristics of these interfaces are described in clause 5 of the present document.

Table 1: Common Pad Assignments

No. (see note 1)	Name	Description	Clause (see note 2)
1	GND	Ground	Clause 5.6.2
2	GND	Ground	Clause 5.6.2
3	RF_3	Antenna for diversity	Clause 5.1.1.3
4	GND	Ground	Clause 5.6.2
5	GND	Ground	Clause 5.6.2
6	GND	Ground	Clause 5.6.2
7	GND	Ground	Clause 5.6.2
8	GND	Ground	Clause 5.6.2
9	RF_GNSS	Antenna for a GNSS receiver	Clause 5.1.1.5
10	GND	Ground	Clause 5.6.2
11	GND	Ground	Clause 5.6.2
12	GND	Ground	Clause 5.6.2
13	GND	Ground	Clause 5.6.2
14	GND	Ground	Clause 5.6.2
15	RF_1	Main antenna	Clause 5.1.1.1
16	GND	Ground	Clause 5.6.2
17	GND	Ground	Clause 5.6.2
18	GND	Ground	Clause 5.6.2
19	GND	Ground	Clause 5.6.2
20	GND	Ground	Clause 5.6.2
21	RF_2	Antenna for diversity	Clause 5.1.1.2
22	GND	Ground	Clause 5.6.2
23	GND	Ground	Clause 5.6.2
24	GND	Ground	Clause 5.6.2
25	GND	Ground	Clause 5.6.2
26	GND	Ground	Clause 5.7.2
27	RF_AUX	Antenna for auxiliary RF(ex: Bluetooth®)	Clause 5.1.1.6
28	GND	Ground	Clause 5.6.2
29	GND	Ground	Clause 5.6.2
30	GND	Ground	Clause 5.6.2

No. (see note 1)	Name	Description	Clause (see note 2)
31	GND	Ground	Clause 5.6.2
32	GND	Ground	Clause 5.6.2
33	RF_4	Antenna for diversity	Clause 5.1.1.4
34	GND	Ground	Clause 5.6.2
35	GND	Ground	Clause 5.6.2
36	GND	Ground	Clause 5.6.2
37	VCC1	Power	Clause 5.6.1.1
38	VCC2	Power	Clause 5.6.1.1
39	VCC3	Power	Clause 5.6.1.1
40	VCC4	Power	Clause 5.6.1.1
41	VCC5	Power	Clause 5.6.1.1
42	VCC6	Power	Clause 5.6.1.1
43	RTC_POWER	Power Input for Real Time Clock	Clause 5.6.1.2
44	GND	Ground	Clause 5.6.2
45	GND	Ground	Clause 5.6.2
46	PCM_SYNC/I2S_WS/SLIM_CLK/GPIO46	PCM/I2S/SLIMBus/GPIO	Clauses 5.5 and 5.4.1
47	PCM_DIN/I2S_DIN/SLIM_DATA/GPIO47	PCM/I2S/SLIMBus/GPIO	Clauses 5.5 and 5.4.1
48	PCM_DOUT/I2S_DOUT/GPIO48	PCM/I2S/GPIO	Clauses 5.5 and 5.4.1
49	PCM_CLK/I2S_CLK/GPIO49	PCM/I2S/GPIO	Clauses 5.5 and 5.4.1
50	GND	Ground	Clause 5.6.2
51	GND	Ground	Clause 5.6.2
52	GPIO01	General Purpose Input / Output 1	Clause 5.6.1
53	GPIO02	General Purpose Input / Output 2	Clause 5.6.1
54	GPIO03	General Purpose Input / Output 3	Clause 5.6.1
55	GPIO04	General Purpose Input / Output 4	Clause 5.6.1
56	GPP01	General Purpose Pad 1	Clause 5.6.2
57	GPP02	General Purpose Pad 2	Clause 5.6.2
58	GPP03	General Purpose Pad 3	Clause 5.6.2
59	GPP04	General Purpose Pad 4	Clause 5.6.2
60	GPP05	General Purpose Pad 5	Clause 5.6.2
61	GPP06	General Purpose Pad 6	Clause 5.6.2
62	GPP07	General Purpose Pad 7	Clause 5.6.2
63	GPP08	General Purpose Pad 8	Clause 5.6.2
64	RFU	Reserved for Future Use	Clause 5.8
65	RFU	Reserved for Future Use	Clause 5.8
66	RFU	Reserved for Future Use	Clause 5.8
67	RFU	Reserved for Future Use	Clause 5.8
68	RFU	Reserved for Future Use	Clause 5.8
69	RFU	Reserved for Future Use	Clause 5.8
70	RFU	Reserved for Future Use	Clause 5.8
71	RFU	Reserved for Future Use	Clause 5.8
72	RFU	Reserved for Future Use	Clause 5.8
73	RFU	Reserved for Future Use	Clause 5.8
74	GND	Ground	Clause 5.6.2
75	GND	Ground	Clause 5.6.2
76	UART1_DTR (UART 1)	Data Terminal(Host)Ready-UART 1	Clause 5.2.1.8
77	UART1_RING (UART 1)	UART Ring Indicator-UART 1	Clause 5.2.1.7
78	UART1_DCD (UART 1)	Data Carrier Detect-UART 1	Clause 5.2.1.6
79	UART1_DSR (UART 1)	Data Set Ready on module-UART 1	Clause 5.2.1.5
80	UART1_CTS (UART 1)	Clear To Send for UART 1	Clause 5.2.1.4
81	UART1_RTS (UART 1)	Request To Send for UART 1	Clause 5.2.1.3
82	UART1_RX (UART 1)	Receive for UART 1	Clause 5.2.1.2
83	UART1_TX (UART 1)	Transmit for UART 1	Clause 5.2.1.1
84	GND	Ground	Clause 5.6.2
85	GND	Ground	Clause 5.6.2
86	USB_Dp	USB Data Positive	Clause 5.2.2.1
87	VBUS/GPIO87	USB Detect / GPIO	Clauses 5.2.2.3 and 5.5.1
88	USB_Dn	USB Data Negative	Clause 5.2.2.2
89	GND	Ground	Clause 5.6.2

No. (see note 1)	Name	Description	Clause (see note 2)
90	GND	Ground	Clause 5.6.2
91	GND	Ground	Clause 5.6.2
92	USB3_SSTXn/PCIe_Tn/MPHY_TX1_Dn/CPHY_LANE1_DATA_A/GPIO92	USB 3.0/PCIe/MIPI M-PHY/Lane 1 Data Line A/GPIO	Clauses 5.2.4.2, 5.2.5.4, 5.2.6.2, 5.2.7.1 and 5.4.1
93	PCIe_CLKREQ/MPHY_SB1/CPHY_SB1/UART3_TX (UART 3)/GPIO93	PCIe/MIPI M-PHY/C-PHY Sideband 1/Transmit for UART 3/GPIO	Clauses 5.2.5.8, 5.2.6.9, 5.2.7.10, 5.2.1.1 and 5.4.1
94	USB3_SSTXp/PCIe_Tp/MPHY_TX1_Dp/CPHY_LANE1_DATA_B/GPIO94	USB 3.0/PCIe/MIPI M-PHY/Lane 1 Data Line B/GPIO	Clauses 5.2.4.1, 5.2.5.3, 5.2.6.1, 5.2.7.2 and 5.4.1
95	PCIe_WAKE/MPHY_SB2/CPHY_SB2/UART3_RX (UART 3)/GPIO95	MIPI M-PHY/PCIe/C-PHY Sideband 2/Receive for UART 3/GPIO	Clauses 5.2.5.9, 5.2.6.10, 5.2.7.11, 5.2.1.2 and 5.4.1
96	USB3_SSRXn/PCIe_Rn/MPHY_RX1_Dn/CPHY_LANE1_DATA_C/GPIO96	USB 3.0/ PCIe/MIPI M-PHY/Lane 1 Data Line C/GPIO	Clauses 5.2.4.4, 5.2.5.2, 5.2.6.4, 5.2.7.3 and 5.4.1
97	PCIe_RST/MPHY_SB3/CPHY_SB3/UART3_RTS (UART 3)/GPIO97	PCIe/MIPI M-PHY/C-PHY Sideband 3/Request To Send for UART 3/GPIO	Clauses 5.2.5.7, 5.2.6.11, 5.2.7.12, 5.2.1.3 and 5.4.1
98	USB3_SSRXp/PCIe_Rp/MPHY_RX1_Dp/CPHY_LANE2_DATA_A/GPIO98	USB 3.0/ PCIe/MIPI M-PHY/Lane 2 Data Line A/GPIO	Clauses 5.2.4.3, 5.2.5.1, 5.2.6.3, 5.2.7.4 and 5.4.1
99	USB_STROBE/MPHY_SB4/CPHY_LANE2_DATA_B /UART3_CTS (UART 3)/GPIO99	HSIC USB/MIPI M-PHY/Lane 2 Data Line B /Clear To Send for UART 3/GPIO	Clauses 5.2.3.1, 5.2.6.12, 5.2.7.5, 5.2.1.4 and 5.4.1
100	USB_DATA/MPHY_TX2_Dn/CPHY_LANE2_DATA_C/GPIO100	HSIC USB/MIPI M-PHY/Lane 2 Data Line C/GPIO	Clauses 5.2.3.2, 5.2.6.6, 5.2.7.6 and 5.4.1
101	MPHY_TX2_Dp/CPHY_LANE3_DATA_A/GPIO101	MIPI M-PHY/Lane 3 Data Line A/GPIO	Clauses 5.2.6.5, 5.2.7.7 and 5.4.1
102	PCIe_REFCLKn/MPHY_RX2_Dn/CPHY_LANE3_DATA_B/GPIO102	PCIe/MIPI M-PHY/Lane 3 Data Line B/GPIO	Clauses 5.2.5.6, 5.2.6.8, 5.2.7.8 and 5.4.1
103	PCIe_REFCLKp/MPHY_RX2_Dp/CPHY_LANE3_DATA_C/GPIO103	PCIe/MIPI M-PHY/Lane 3 Data Line C/GPIO	Clauses 5.2.5.5, 5.2.6.7, 5.2.7.9 and 5.4.1
104	GND	Ground	Clause 5.6.2
105	GND	Ground	Clause 5.6.2
106	UART2_RX (UART 2)	Receive for UART 2	Clause 5.2.1.2
107	UART2_TX (UART 2)	Transmit for UART 2	Clause 5.2.1.1
108	GND	Ground	Clause 5.6.2
109	GND	Ground	Clause 5.6.2
110	RFU	Reserved for Future Use	Clause 5.8
111	RFU	Reserved for Future Use	Clause 5.8
112	RFU	Reserved for Future Use	Clause 5.8
113	RFU	Reserved for Future Use	Clause 5.8
114	RFU	Reserved for Future Use	Clause 5.8
115	RFU	Reserved for Future Use	Clause 5.8
116	RFU	Reserved for Future Use	Clause 5.8
117	RFU	Reserved for Future Use	Clause 5.8
118	RFU	Reserved for Future Use	Clause 5.8
119	RFU	Reserved for Future Use	Clause 5.8
120	GPP09	General Purpose Pad 9	Clause 5.4.2
121	GPP10	General Purpose Pad 10	Clause 5.4.2
122	GPP11	General Purpose Pad 11	Clause 5.4.2
123	GPP12	General Purpose Pad 12	Clause 5.4.2
124	GPP13	General Purpose Pad 13	Clause 5.4.2
125	GPP14	General Purpose Pad 14	Clause 5.4.2
126	GPP15	General Purpose Pad 15	Clause 5.4.2
127	GPP16	General Purpose Pad 16	Clause 5.4.2
128	GPP17	General Purpose Pad 17	Clause 5.4.2
129	GPIO05	General Purpose Input / Output 5	Clause 5.4.1

No. (see note 1)	Name	Description	Clause (see note 2)
130	GPIO06/vGPIO Data In	General Purpose Input / Output 6/vGPIO DataIn	Clauses 5.4.1 and 5.6.3
131	GPIO07/vGPIO Clock	General Purpose Input / Output 7/vGPIO Clock	Clauses 5.4.1 and 5.6.3
132	GPIO08/vGPIO Data Out	General Purpose Input / Output 8/vGPIO DataOut	Clauses 5.4.1 and 5.6.3
133	UIM_VCC	Power source for external UIM	Clause 5.1.2.1
134	UIM_DATA	Data in/out	Clause 5.1.2.2
135	UIM_CLK	Clock signal	Clause 5.1.2.3
136	UIM_RESET	Reset signal	Clause 5.1.2.4
137	UIM_DETECT	UIM Detect signal	Clause 5.1.2.5
138	UIM_SPU	Standard or Proprietary Use	Clause 5.1.2.6
139	GND	Ground	Clause 5.6.2
140	GND	Ground	Clause 5.6.2
141	WWAN_STATE	Wireless WAN Radio State	Clause 5.3.1
142	POWER_ON	Power On the module	Clause 5.3.2
143	WAKEUP_OUT/GPIO143	Module wakes up host OR GPIO	Clauses 5.3.3 and 5.4.1
144	WAKEUP_IN/GPIO144	Host wakes up module OR GPIO	Clauses 5.3.4 and 5.4.1
145	RESET	Reset the module	Clause 5.3.5
146	VREF	Reference Logic Voltage	Clause 5.3.6
147	RFU	Reserved for Future Use	Clause 5.8
148	RFU	Reserved for Future Use	Clause 5.8
149	RFU	Reserved for Future Use	Clause 5.8
150	RFU	Reserved for Future Use	Clause 5.8
151	RFU	Reserved for Future Use	Clause 5.8
152	RFU	Reserved for Future Use	Clause 5.8
153	RFU	Reserved for Future Use	Clause 5.8
154	RFU	Reserved for Future Use	Clause 5.8
155	RFU	Reserved for Future Use	Clause 5.8
156	RFU	Reserved for Future Use	Clause 5.8
157	RFU	Reserved for Future Use	Clause 5.8
158	RFU	Reserved for Future Use	Clause 5.8
159	RFU	Reserved for Future Use	Clause 5.8
160	RFU	Reserved for Future Use	Clause 5.8
161	RFU	Reserved for Future Use	Clause 5.8
162	RFU	Reserved for Future Use	Clause 5.8
163	RFU	Reserved for Future Use	Clause 5.8
164	RFU	Reserved for Future Use	Clause 5.8
165	RFU	Reserved for Future Use	Clause 5.8
166	RFU	Reserved for Future Use	Clause 5.8

NOTE 1: Number referring to the numbering in corresponding module figure.
NOTE 2: This column refers to the clause that defines the electrical characteristics of the interface provided by this pad.

5 Electrical Specifications

5.0 Electrical Interfaces and Interface Families

This clause defines the I/O interfaces that may be supported by the SMT module and their electrical characteristics.

Where clause 4 assigns any of the specified interfaces to specific pads, modules may leave these pads unimplemented inside the module. Host devices using this module with unimplemented interfaces may then either connect these unused pads to ground or leave them floating. This is to avoid possible interference conditions where a particular host device was designed for a particular interface to be present.

Table 2: Electrical Interfaces and Interface Families

Interface Family	Interface	Signal	Description	I/O
RF Interfaces		RF_1	Used in a system with 1 or more	I/O

Interface Family	Interface	Signal	Description	I/O
			antennae	
		RF_2	Used in a system with 2 or more antennae	I/O
		RF_3	Used in a system with 3 or more antennae	I/O
		RF_4	Used in a system with 4 or more antennae	I/O
		RF_GNSS	Antenna for GNSS	I
		RF_AUX	Antenna for additional peripheral	I/O
User Identity Module		UIM_VCC	Power source for external UIM	O
		UIM_DATA	Data in/out	I/O
		UIM_CLK	Clock signal	O
		UIM_RESET	Reset signal	O
		UIM_DETECT	UIM detect signal	I
		UIM_SPU	Standard or Proprietary Use	-
Data Interfaces	UART	UART_RTS	Module ready to send	O
		UART_TX	Module sending data	O
		UART_RX	Module receiving data	I
		UART_CTS	Clear to send	I
		UART_DSR	Data ready on module	O
		UART_DCD	Carrier detect	O
		UART_RING	Ring indication	O
		UART_DTR	Host ready	I
	USB 2.0	USB_Dp	USB 2.0 Data positive	I/O
		USB_Dn	USB 2.0 Data negative	I/O
		VBUS	USB 2.0 Signal detect	I
	HSIC USB	USB_STROBE	USB 2.0 HSIC Strobe	I/O
		USB_DATA	USB 2.0 HSIC Data	I/O
	USB 3.0	USB3_SSTXp	USB 3.0 SuperSpeed send positive	I/O
		USB3_SSTXn	USB 3.0 SuperSpeed send negative	I/O
		USB3_SSRXp	USB 3.0 SuperSpeed receive positive	I/O
		USB3_SSRXn	USB 3.0 SuperSpeed receive negative	I/O
	PCIe	PCIe_Rp	PCIe Receive positive	I
		PCIe_Rn	PCIe Receive negative	I
		PCIe_Tp	PCIe Transmit positive	O
		PCIe_Tn	PCIe Transmit negative	O
		PCIe_REFCLKp	Reference clock positive	I
		PCIe_REFCLKn	Reference clock negative	I
		PCIe_RST	PCIe Reset	I
		PCIe_CLKREQ	PCIe Clock request	I/O
		PCIe_WAKE	PCIe Wake	I/O
	MIPI M-PHY	MPHY-TX1-Dp	Transmit lane 1 - data positive	O
		MPHY_TX1-Dn	Transmit lane 1 - data negative	O
		MPHY_RX1-Dp	Receive lane 1 - data positive	I
		MPHY_RX1-Dn	Receive lane 1 - data negative	I
		MPHY_TX2-Dp	Transmit lane 2 - data positive	O
		MPHY_TX2-Dn	Transmit lane 2 - data negative	O
		MPHY_RX2-Dp	Receive lane 2 - data positive	I
		MPHY_RX2-Dn	Receive lane 2 - data negative	I
		MPHY_SB1	MIPI M-PHY Sideband #1	I/O
		MPHY_SB2	MIPI M-PHY Sideband #2	I/O
		MPHY_SB3	MIPI M-PHY Sideband #3	I/O
		MPHY_SB4	MIPI M-PHY Sideband #4	I/O

Interface Family	Interface	Signal	Description	I/O
	MIPI C-PHY	CPHY_LANE1_DATA_A	Lane 1, Data Line A	I/O
		CPHY_LANE1_DATA_B	Lane 1, Data Line B	I/O
		CPHY_LANE1_DATA_C	Lane 1, Data Line C	I/O
		CPHY_LANE2_DATA_A	Lane 2, Data Line A	I/O
		CPHY_LANE2_DATA_B	Lane 2, Data Line B	I/O
		CPHY_LANE2_DATA_C	Lane 2, Data Line C	I/O
		CPHY_LANE3_DATA_A	Lane 3, Data Line A	I/O
		CPHY_LANE3_DATA_B	Lane 3, Data Line B	I/O
		CPHY_LANE3_DATA_C	Lane 3, Data Line C	I/O
		CPHY_SB1	C-PHY Sideband 1	I/O
		CPHY_SB2	C-PHY Sideband 2	I/O
		CPHY_SB3	C-PHY Sideband 3	I/O
Module Control and State Interfaces		WWAN_STATE	WWAN radio state	O
		POWER_ON	Power on	I
		WAKEUP_OUT	Module wakes up host	O
		WAKEUP_IN	Host wakes up module	I
		RESET	Reset module	I
Power and Ground		VREF	Voltage Reference Output	O
		VCC	Main Power	I
		GROUND	Ground	I
		RTC_POWER	Power for an internal Real Time Clock	I
General Purpose		GPIO	Digital I/O	I/O
		GPP	General Purpose Pad	I/O
	Virtual GPIO	VGPIO_DIN	vGPIO Data In	I
		VGPIO_DOUT	vGPIO Data Out	O
		VGPIO_CLK	vGPIO Clock	I/O
Digital Audio	PCM	PCM_SYNC	Synchronization signal	O
		PCM_DIN	Data In	I
		PCM_DOUT	Data Out	O
		PCM_CLK	Clock	O
	I2S	I2S_WS	I2S Word Select	I/O
		I2S_DIN	I2S Data In	I
		I2S_DOUT	I2S Data Out	O
		I2S_CLK	I2S Clock	I/O
	SLIMBus	SLIM_CLK	SLIMBus Clock Line	I/O
		SLIM_DATA	SLIMBus Data Line	I/O
RFU	RFU	RFU	Reserved For Future Use	-
Test and Debug		JTAG	Defined by manufacturer	-

5.1 RF and UIM

5.1.1 Electrical Characteristics of RF Interfaces

5.1.1.1 RF_1

An antenna pad to be used in a system that uses 1 or more antennae.

The nominal RF impedance shall be 50 Ohms.

5.1.1.2 RF_2

An antenna pad to be used in a system that uses 2 or more antennae.

The nominal RF impedance shall be 50 Ohms.

5.1.1.3 RF_3

An antenna pad to be used in a system that uses 3 or more antennae.

The nominal RF impedance shall be 50 Ohms.

5.1.1.4 RF_4

An antenna pad to be used in a system that uses 4 antennae.

The nominal RF impedance shall be 50 Ohms.

5.1.1.5 RF_GNSS

An antenna pad to be used for GNSS. This signal is typically an input signal only.

The nominal RF impedance shall be 50 Ohms.

5.1.1.6 RF_AUX

An antenna pad for an additional peripheral.

The nominal RF impedance shall be 50 Ohms.

5.1.2 User Identity Module

5.1.2.0 UIM Interface Introduction

If an external UIM is used in the design then the module shall provide the following interfaces to support an external User Interface Module compliant with [1]. For further reference also see [2].

5.1.2.1 UIM_VCC

A power source output to an external UIM.

5.1.2.2 UIM_DATA

Data in/out for an external UIM.

5.1.2.3 UIM_CLK

An output clock signal to an external UIM.

5.1.2.4 UIM_RESET

An output reset signal to an external UIM.

5.1.2.5 UIM_DETECT

An input signal used to detect an external UIM.

5.1.2.6 UIM_SPU

The module may provide this interface for forward looking standard or proprietary use.

ETSI ISG SMT has defined that this pad will be used for UICC-CLF (NFC communications) when the standards support the use case. The pad would be connected to UICC contact C6 when used.

5.2 Data Interfaces

5.2.0 Data Interfaces Introduction

Data interfaces are those interfaces that enable the exchange of data between the module and the host. Module control functions (for example AT Commands, MBIM or other APIs) are typically included over one or more data interfaces. Physical form factors defined in clause 4 may provide dedicated pad locations for some data interfaces while other data interfaces may be allocated to shared pad locations.

5.2.1 Universal Asynchronous Receiver-Transmitter

5.2.1.0 2-wire, 4-wire, and 8-wire UART Configurations

The Universal Asynchronous Receiver-Transmitter (UART) interface has the following electrical characteristics:

- A 2-wire UART consists of the UART_TX and UART_RX interfaces.
- A 4-wire UART consists of the UART_RTS, UART_CTS, UART_TX and UART_RX interfaces.
- An 8-wire UART consists of all interfaces defined in this clause.

5.2.1.1 UART_TX

This is a module output for transmitting data (Tx). This signal maps to the UART Rx interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 2-wire, 4-wire, or 8-wire UART interface.

5.2.1.2 UART_RX

This is a module input for receiving data (Rx). This signal maps to the UART Tx interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 2-wire, 4-wire, or 8-wire UART interface.

5.2.1.3 UART_RTS

This is a module output for the Ready To Send (RTS) signal used for host flow control. This signal maps out to the UART CTS interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 4-wire or 8-wire UART interface.

5.2.1.4 UART_CTS

This is a module input for the Clear To Send (CTS) signal. This signal originates from the UART RTS interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 4-wire or 8-wire UART interface.

5.2.1.5 UART_DSR

Data Set Ready on module. This is an output from the module. This interface is only included on an 8-wire UART interface.

5.2.1.6 UART_DCD

Data Carrier Detect. This is an output from the module. This interface is only included on an 8-wire UART interface.

5.2.1.7 UART_RING

UART Ring indication is an output from the module. This interface is only included on an 8-wire UART interface. It may serve a similar function as the WAKEUP_OUT interface to alert the host upon an event occurrence within the module such as an incoming call received, SMS received, etc. This is an active low signal.

5.2.1.8 UART_DTR

Data Terminal Ready (also known as host ready) is an input to the module. This interface is only included on an 8-wire UART interface.

5.2.2 Universal Serial Bus 2.0

5.2.2.0 USB 2.0 Introduction

The USB 2.0 interface provides data transfer, communication, debugging and communication to and from external peripherals and host devices. For the electrical characteristics of the USB 2.0 interface please refer to [3].

5.2.2.1 USB_Dp

USB 2.0 Data positive.

5.2.2.2 USB_Dn

USB 2.0 Data negative.

5.2.2.3 VBUS

The VBUS is a USB 2.0 Signal detection and is an input to the module to detect that the host is present. If the USB 2.0 interface is utilized the implementation of this pad is optional. If this pad is not used for the purpose described in this clause this pad may instead be used as a GPIO interface.

5.2.3 Universal Serial Bus 2.0 High-Speed Inter-Chip

5.2.3.0 USB 2.0 HSIC Introduction

For the electric characteristics of the Universal Serial Bus 2.0 High-Speed Inter-Chip (USB 2.0 HSIC) please refer to [3].

5.2.3.1 USB_STROBE

USB 2.0 HSIC Strobe.

5.2.3.2 USB_DATA

USB 2.0 HSIC Data.

5.2.4 Universal Serial Bus 3.0 SuperSpeed Interfaces

5.2.4.0 USB 3.0 SuperSpeed Introduction

For the electric characteristics of the Universal Serial Bus 3.0 (USB 3.0) SuperSpeed interface please refer to [5].

5.2.4.1 USB3_SSTXp

USB 3.0 SuperSpeed send positive is an output from the module.

5.2.4.2 USB3_SSTXn

USB 3.0 SuperSpeed send negative is an output from the module.

5.2.4.3 USB3_SSRXp

USB 3.0 SuperSpeed receive positive is an input to the module.

5.2.4.4 USB3_SSRXn

USB 3.0 SuperSpeed receive negative is an input to the module.

5.2.5 Peripheral Component Interconnect Express

5.2.5.0 PCIe Introduction

For the electric characteristics of the Peripheral Component Interconnect Express (PCIe) please refer to [6].

5.2.5.1 PCIe_Rp

PCIe Receive positive.

5.2.5.2 PCIe_Rn

PCIe Receive negative.

5.2.5.3 PCIe_Tp

PCIe Transmit positive.

5.2.5.4 PCIe_Tn

PCIe Transmit negative.

5.2.5.5 PCIe_REFCLKp

Reference clock positive.

5.2.5.6 PCIe_REFCLKn

Reference clock negative.

5.2.5.7 PCIe_RST

PCIe Reset.

5.2.5.8 PCIe_CLKREQ

PCIe Clock request.

5.2.5.9 PCIe_WAKE

PCIe Wake.

5.2.6 MIPI M-PHY

5.2.6.0 MIPI M-MPHY Introduction

For the electric characteristics of the MIPI M-PHY interface please refer to [7].

The MIPI Low Latency Interface (LLI), SuperSpeed Inter-Chip (SSIC) interface or Mobile PCIe can be provided over the MIPI M-PHY interface. Two transmit and two receive lanes and four sidebands are provided for implementing any of these protocols.

5.2.6.1 MPHY_TX1-Dp

Transmit lane 0 - data positive.

5.2.6.2 MPHY_TX1-Dn

Transmit lane 0 - data negative.

5.2.6.3 MPHY_RX1-Dp

Receive lane 0 - data positive.

5.2.6.4 MPHY_RX1-Dn

Receive lane 0 - data negative.

5.2.6.5 MPHY_TX2-Dp

Transmit lane 1 - data positive.

5.2.6.6 MPHY_TX2-Dn

Transmit lane 1 - data negative.

5.2.6.7 MPHY_RX2-Dp

Receive lane 1 - data positive.

5.2.6.8 MPHY_RX2-Dn

Receive lane 1 -data negative.

5.2.6.9 MPHY_SB1

MIPI M-PHY Sideband #1.

5.2.6.10 MPHY_SB2

MIPI M-PHY Sideband #2.

5.2.6.11 MPHY_SB3

MIPI M-PHY Sideband #3.

5.2.6.12 MPHY_SB4

MIPI M-PHY Sideband #4.

5.2.7 MIPI C-PHY

5.2.7.0 MIPI C-PHY Introduction

For the electric characteristics of the MIPI C-PHY interface please refer to [14].

The MIPI CSI (Camera Serial Interface) or Display Serial Interface (DSI) can be provided over the MIPI C-PHY interface. Three data lanes and three sidebands are provided for implementing any of these protocols.

5.2.7.1 CPHY_LANE1_DATA_A

Lane 1, Data Line A.

5.2.7.2 CPHY_LANE1_DATA_B

Lane 1, Data Line B.

5.2.7.3 CPHY_LANE1_DATA_C

Lane 1, Data Line C.

5.2.7.4 CPHY_LANE2_DATA_A

Lane 2, Data Line A.

5.2.7.5 CPHY_LANE2_DATA_B

Lane 2, Data Line B.

5.2.7.6 CPHY_LANE2_DATA_C

Lane 2, Data Line C.

5.2.7.7 CPHY_LANE3_DATA_A

Lane 3, Data Line A.

5.2.7.8 CPHY_LANE3_DATA_B

Lane 3, Data Line B.

5.2.7.9 CPHY_LANE3_DATA_C

Lane 3, Data Line C.

5.2.7.10 CPHY_SB1

C-PHY Sideband #1.

5.2.7.11 CPHY_SB2

C-PHY Sideband #2.

5.2.7.12 CPHY_SB3

C-PHY Sideband #3.

5.3 Module Control and State Functions

5.3.0 Module Control and State Functions Introduction

Module control and state function interfaces support various core operating functions of the module. For details of the electrical specification for each interface in this sub-clause see clause 5.6.4 where electrical details of digital logic levels for different voltage platforms are defined.

5.3.1 WWAN_STATE

The WWAN_STATE pad may support an LED signal to provide radio state indications to users. The signal is active high and intended to drive a system-mounted LED indicator.

OFF - Radio is incapable of transmitting. This state is indicated when the radio is not powered or when the radio is disabled by software.

ON - Radio is capable of transmitting. The signal should remain ON even if the radio is not actually transmitting. For example, the signal remains ON during temporary radio disablements performed by the module of its own volition to do scanning, switching radios/bands, power management, etc. If the module is in a state where it is possible that radio can begin transmitting without the system user performing any action, this signal should remain ON.

A recommended external hardware circuit for an LED is show in figure 37.

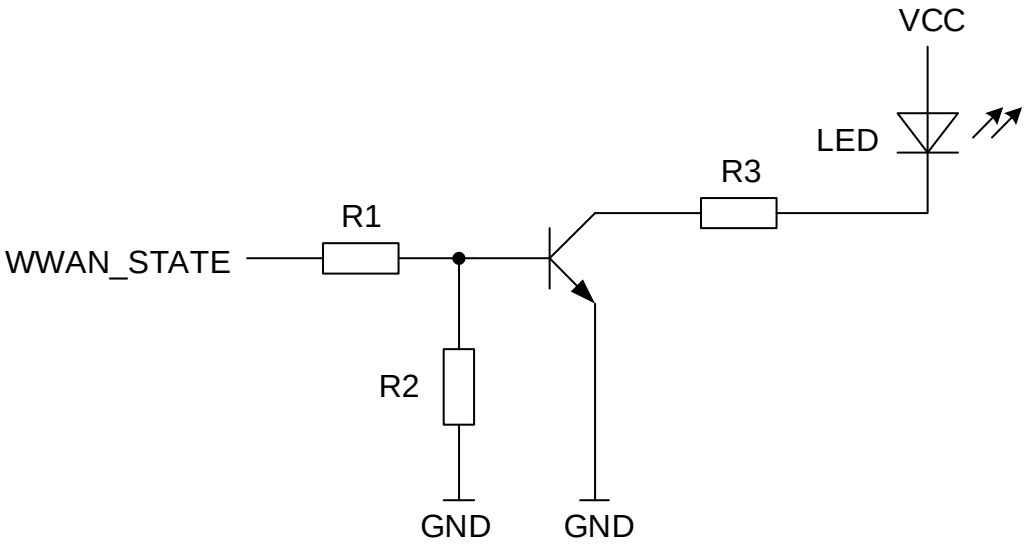

Figure 37: A recommended external hardware LED circuit

The present document also allows user programmable states for this signal for more exotic state methods as described in clause B.4 of Annex B.

5.3.2 POWER_ON

The POWER_ON pad is an input signal used to control whether the module is in the Module Enabled or Module Disabled state.

There are three possible states the module can be in:

- Module Off - VCC is not present.

- Module Enabled - VCC is supplied and the module is enabled.
- Module Disabled - VCC is supplied and the module is disabled.

The state transitions are defined as follows:

- When voltage is applied to VCC the module shall enter the Module Disabled state.
- An input to the POWER_ON pad shall trigger the transition from the Module Disabled to the Module Enabled state.
- An input to the POWER_ON pad shall trigger the transition from the Module Enabled to the Module Disabled state.

Example implementations for the input to the POWER_ON pad are described here:

- The POWER_ON signal can be Active High (VIH for VREF) or Active Low (VIL for VREF) and behave either as a State Request (Active represents Enabled, Non-Active represents Disabled) or a Change of State Request (Enabled to Disabled or Disabled to Enabled).

Here are some examples of possible designs using the POWER_ON interface.

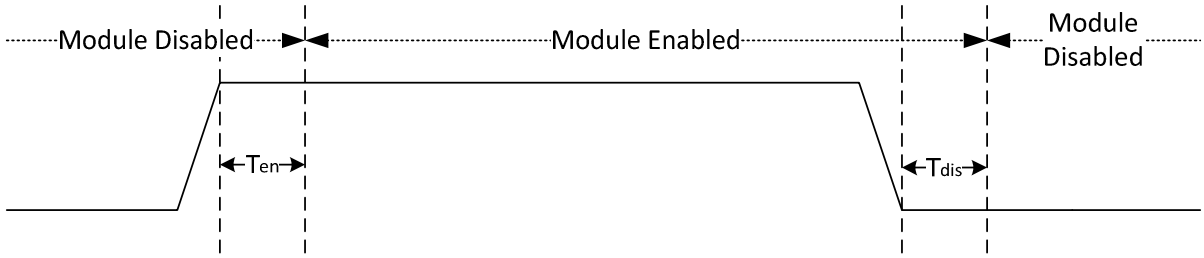

Figure 38: State Request, Active High, Ten = Enable Timer, Tdis = Disable Timer

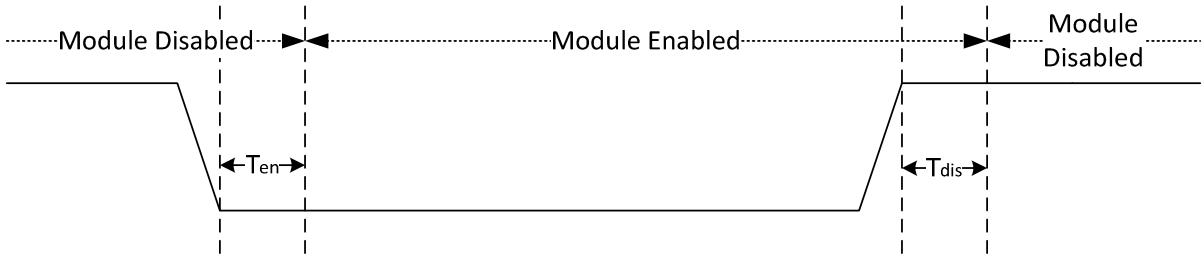

Figure 39: State Request, Active Low, Ten = Enable Timer, Tdis = Disable Timer

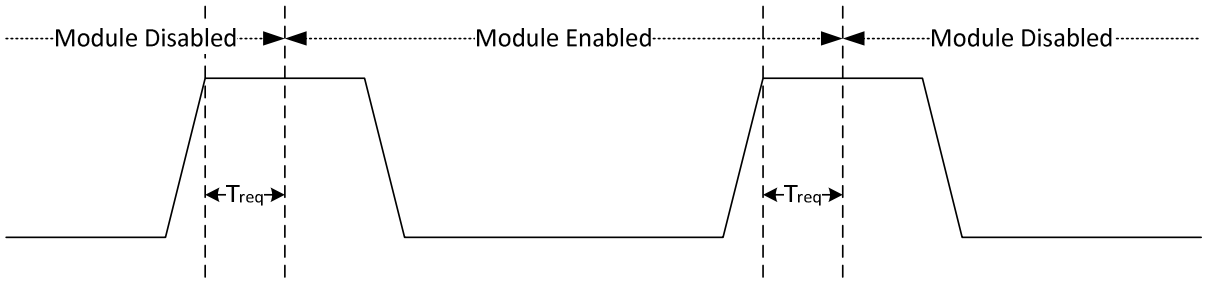

Figure 40: Change of State Request, Active High (Initial State = Disabled), Treq = Request Timer

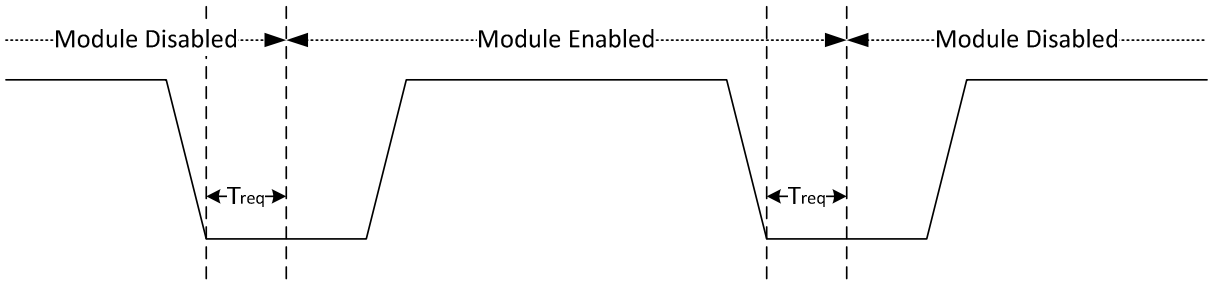

Figure 41: Change of State Request, Active Low (Initial State = Enabled), Treq = Request Timer

Host side implementation for the POWER_ON interface is to be defined by the Module provider (including timing diagrams, operation sequencing, etc.) as the actual implementation is module specific.

NOTE: For 3GPP compliant modules it is required that the module is kept ON for at least 2 seconds after a command to power down the module has been issued to ensure that there is time for the module to shut down properly. The shutdown behaviour towards the SIM and network should comply with 3GPP requirements, please refer to [8].

5.3.3 WAKEUP_OUT

The WAKEUP_OUT pad is an output signal which allows the module to alert the host of a trigger event within the module. When the module intends to wake up the host this interface shall be set high.

If the defined pad for the module is not used for the WAKEUP_OUT function then it may be used as a GPIO.

This interface should conform to the VREF Digital Logic Levels for most modules.

5.3.4 WAKEUP_IN

The WAKEUP_IN pad is an input signal which allows the host device to wake up the module from a state such as a low power mode. When the host intends to wake up the module this interface shall be set high.

If the defined pad for the module is not used for the WAKEUP_IN function then it may be used as a GPIO.

This interface should conform to the VREF Digital Logic Levels for most modules.

5.3.5 RESET

An input to the RESET pad will immediately place the module in a Power On reset condition.

When this interface is set to low for a minimum period of time the module will reset.

Care should be taken not to activate this pad unless there is a critical failure and all other methods of regaining control and/or communication with the module have failed.

See clause B.5 of Annex B for recommended implementation guidelines for the RESET pad.

5.3.6 VREF

VREF is a reference voltage output supplied from the module to provide a logic reference for digital interfaces. See clause 5.6.3 Reference Voltage and Digital Logic Levels.

5.4 General Purpose

5.4.0 GPP and GPIO Introduction

Where clause 4 does not assign the interface to specific pads, implementations may provide the interface over General Purpose Pads (GPP) or General Purpose I/O (GPIO) pads.

5.4.1 General Purpose Input/Output (GPIO)

The General Purpose Input/Output pad is a digital I/O which control and usage shall be defined by the module developer.

This interface should conform to the VREF Digital Logic Levels.

5.4.2 General Purpose Pad (GPP)

The General Purpose Pads are pads that have variable use cases. See Annex A.

5.4.3 Virtual GPIO (vGPIO)

The module may provide a virtual GPIO (vGPIO) interface to increase the number of supported GPIO signals. This interface is to be module defined (Under standardization efforts in MIPI).

5.5 Digital Audio

5.5.0 General Digital Audio Introduction

The present document allows multiple digital audio formats to be supported. Any unused Digital Audio pads may be used as a GPIO interface.

5.5.1 Pulse Code Modulation

5.5.1.0 PCM Introduction

The module may support a Pulse Code Modulation interface to communicate narrowband, monotonic audio (typically voice) to external peripherals.

5.5.1.1 PCM_SYNC

PCM synchronization signal, an output.

5.5.1.2 PCM_DIN

PCM data in, an input.

5.5.1.3 PCM_DOUT

PCM data out, an output.

5.5.1.4 PCM_CLK

PCM clock signal, an output.

5.5.2 Integrated Inter Chip Sound

5.5.2.0 I2S Introduction

The module may support an Integrated Inter Chip Sound interface for digital audio.

5.5.2.1 I2S_WS

I2S Word Select. This interface is an input if the I2S pads are used as a digital audio input in conjunction with I2S_DIN. This interface is an output if the I2S pads are used as a digital audio output in conjunction with I2S_DOUT.

5.5.2.2 I2S_DIN

I2S data input if I2S is used as a digital audio input.

5.5.2.3 I2S_DOUT

I2S data output if I2S is used as a digital audio output.

5.5.2.4 I2S_CLK

I2S Serial Clock. This interface is an input if the I2S pads are used as a digital audio input in conjunction with I2S_DIN. This interface is an output if the I2S pads are used as a digital audio output in conjunction with I2S_DOUT.

5.5.3 SLIMBus

5.5.3.0 SLIMBus Introduction

The module may support a SLIMBus interface for digital audio. For the electrical characteristics of the SLIMBus interface please refer to [9].

5.5.3.1 SLIM_CLK

SLIMBus Clock Line.

5.5.3.2 SLIM_DATA

SLIMBus Data Line.

5.6 Power, Ground and Digital Logic Levels

5.6.1 Power Supply

5.6.1.1 VCC Pads 1 ~ 6

VCC is a 3,8 Volt raw power supply input to the module.

For modules designed to operate on a raw voltage of 3,8 Volts all designs shall be able to operate on a power supply that meets the following requirements. Module designs may exceed these specifications.

Table 3: VCC

Name	Min	Typ	Max
VCC	3,4 V	3,8 V	4,2 V

The present document has defined six VCC pads with a size of 7 mm^2 each (total area of 4,2 mm^2) to enable high continuous current if required and assumes a maximum current of 1 A per 1 mm^2 of VCC pad surface area.

The present document is intended to support multiple technologies and configurations, therefore to specify current draw for the power supply is beyond the scope of the present document.

5.6.1.2 RTC_POWER

This pad is intended to provide an external power supply input for the internal clock so that it may be maintained when VCC is not present at the module.

Table 4: RTC_POWER

Name	Min	Typ	Max
RTC_POWER	2,0 V	3,0 V	3,25 V

5.6.2 Ground

All ground pads on the module are designed to be connected to ground on the host implementation.

5.6.3 Reference Voltage and Digital Logic Levels

5.6.3.1 VREF

VREF is a reference voltage output supplied from the module to provide a logic reference for the following interfaces:

- UART1, UART2, & UART3 - see clause 5.2.1.
- WWAN Radio State - see clause 5.3.1.
- POWER_ON - see clause 5.3.2.
- Wakeup Out - see clause 5.3.3.
- Wake-up In - see clause 5.3.4.
- RESET - see clause 5.3.5.
- GPIO (unless otherwise indicated) - see clause 5.4.1.

This clause describes the electrical characteristics utilized based upon the VREF from the module.

Table 5: Electrical characteristics - Generic Voltage Reference I/O

Parameter	Description	Minimum	Typical	Maximum	Unit	Condition
V_{IL}	Low-level input voltage	-0,3	0	0,30 × VREF	V	
V_{IH}	High-level input voltage	0,70*VREF	VREF	VREF + 0,3	V	V_{IH} Maximum shall be a minimum level supported.
V_{OL}	Low-level output voltage	0	0	0,45	V	IOL varies by pad definition
V_{OH}	High-level output voltage	VREF - 0,45	VREF	VREF	V	IOH varies by pad definition
I_{OH}	High-level output current			1 to 8	mA	Maximum varies by pad definition
I_{OL}	Low-level output current			-1 to -8	mA	

Table 6: Electrical characteristics - An example of a 1,8 V type (1V8) digital I/O

Parameter	Description	Minimum	Typical	Maximum	Unit	Condition
V_{IL}	Low-level input voltage	-0,3 V	0 V	0,54 V	V	
V_{IH}	High-level input voltage	1,26 V	1,8 V	2,1 V	V	
V_{OL}	Low-level output voltage	0,0 V	0,0 V	0,45 V	V	IOL varies by pad definition
V_{OH}	High-level output voltage	1,35 V	1,8 V	1,8 V	V	IOH varies by pad definition
I_{OH}	High-level output current			1 to 8 mA	mA	Maximum varies by pad definition
I_{OL}	Low-level output current			-1 to -8 mA	mA	

5.7 Test and Debug Interface

For the electrical characteristics of the IEEE 1149.1 (Joint Test Action Group, or JTAG) interface for testing and debugging please refer to IEEE 1149.1 [10].

Implementation and location of the JTAG interface are optional.

5.8 Reserved for Future Use (RFU)

It is expected that the Reserved for Future Use pads shall be physically present but not connected internally to the surface mount module. These pads are reserved for definition in future revisions of the present document. Non-standard use of these pads may result in incompatibilities in solutions aligned with the future revisions.

Annex A (informative): Interfaces that may be provided over General Purpose I/O (GPIO) or General Purpose Pads (GPP)

A.0 GPIO and GPP Interfaces Introduction

Where clauses 4 and 5 do not assign an interface to specific pads implementations may provide the interface over General Purpose I/O (GPIO) or General Purpose Pads (GPP) pads.

A.1 Additional Interfaces

A.1.0 Additional Interfaces Introduction

The interfaces defined in this clause are considered to be important for select module implementations. They may be implemented on pads designated as either GPIO or GPP on the module. Alternately a pad designated as GPP may be used to provide additional GPIO functions.

A.1.1 Module State Functions

A.1.1.0 Additional Module Control and State Functions Introduction

The electrical characteristics of interfaces to signal the state of various module aspects is the following:

Interface	Description	I/O	Electrical characteristics
RF_DISABLE	Radio Enable/Disable	I	
GPS_STATE	GPS radio state	O	
PER1_STATE	Peripheral radio state	O	
TX_ON	Module transmitting	O	
READY	Module ready for I/O	O	

A.1.1.1 RF_DISABLE

The Radio Enable/Disable interface can be used to enable and disable the transmitting capabilities of the module and properly deregister the module from the network without powering the module down. One application for this interface is to support "flight mode" for consumer electronics.

A.1.1.2 GNSS_STATE

The GPS State pad can be used as an indication to the host device of whether the module has obtained a valid GPS fix or not.

A.1.1.3 PER1_STATE

The PER1 State pad can be used as an indication to the host device of whether the module has a valid registration on the peripheral radio interface or not.

A.1.1.4 TX_ON

The TX ON pad can be used as an indication to the host device of whether the module is actively transmitting over the cellular network or not.

A.1.1.5 READY

The READY pad can be used as an indication to the host device of whether the module is in a state when it is ready to start receiving commands from the host device.

A.1.2 Analog Interfaces

A.1.2.0 Analog Interfaces Introduction

The module may support analog interfaces other than RF such as analog audio (clause A.1.2.1) and an analog-digital converter (clause A.1.2.2). If these interfaces are supported, care should be taken with their placement on the module so as to a avoid interference with digital interfaces. The electrical characteristics of an analog audio interface are as follows:

Interface	Description	I/O	Electrical characteristics
MICp	Microphone positive	I	Module defined
MICn	Microphone negative	I	
SPKp	Speaker positive	O	
SPKn	Speaker negative	O	
ADCI	A/D Converter input	I	
DACO	D/A Converter output	O	

A.1.2.1 Analog Audio

The module may provide an analog audio interface for providing speaker and microphone access for devices are unable to support a digital audio interface.

A.1.2.2 A/D Converter

The module may support an A/D converter for taking raw analog input data and converting it into digital logic levels. Care should be taken to ensure that the allowable input voltage range on this interface is clearly specified.

A.1.2.3 D/A Converter

The module may support a D/A converter for taking digital logic level input data and converting it into an analog output.

A.1.3 Host interface select

The module may provide an interface to allow the host to select a data interface if the module supports several such interfaces. This is a logical interface representing a binary number: an *n* line interface allows the host to choose between 2^n interfaces:

Interface	Description	I/O	Electrical characteristics
HOST_IO_SEL1	*n*-bit binary logic signal	I	Module defined
HOST_IO_SEL2		I	
…		…	
HOST_IO_SEL*n*		I	

A.1.4 Antenna control

The module may support an interface for antenna control. Such an interface would typically have up to 4 lines:

Interface	Description	I/O	Electrical characteristics
RF_CTRL1	Generic interface for antenna control		Undefined
RF_CTRL2			
RF_CTRL3			
RF_CTRL4			

A.1.5 Real Time Clock

The module may provide an interface for the host to provide a 32 kHz clock signal to the module or an interface for the host to provide power for the real time clock of the module:

Interface	Description	I/O	Electrical characteristics
RTC_IN	Real time clock in	I	Module defined

A.1.6 Pulse Width Modulation

The module may provide a Pulse Width Modulation (PWM) interface to modulate acoustic and visual signals.

A.1.7 Timer Interface

The module may provide a timer interface.

A.1.8 Interrupt

The module may provide an interrupt interface.

A.1.9 Dynamic Power Reduction

The module may provide a Dynamic Power Reduction (DPR) interface to allow hardware control for Specific Absorption Rates (SAR) adherence.

Interface	Description	I/O	Electrical characteristics
DPR	Dynamic Power Reduction	I	Module defined

A.1.10 Virtual GPIO (vGPIO)

The module may provide a virtual GPIO (vGPIO) interface to increase the number of supported GPIO signals.

Interface	Description	I/O	Electrical characteristics
VGPIO_DIN	vGPIO Data In	I	Module defined (Under standardization efforts in MIPI)
VGPIO_DOUT	vGPIO Data Out	O	
VGPIO_CLK	vGPIO Clock	I/O	

A.2 Peripheral Interfaces

A.2.0 Peripheral Interfaces Introduction

Peripheral interfaces are interfaces that support the exchange of data and control information between the module and peripheral devices.

A.2.1 Secure Digital Input Output Interface

Secure Digital Input Output (SDIO) is mostly used for storage or WLAN but can be also used for high speed data exchange in general. A device can be an SDIO master or slave. The electrical characteristics of the SDIO interface are as follows:

Interface	Description	I/O	Electrical characteristics
SDIO_CLK	SDIO clock signal	I/O	Please refer to [11]. On an SDIO slave the SDIO_CLK and SDIO_CMD interfaces are inputs (I). On an SDIO master the SDIO_CLK and SDIO_CMD interfaces are outputs (O).
SDIO_CMD	SDIO command	I/O	
SDIO_DATA1	Data line	I/O	
SDIO_DATA2	Data line	I/O	
SDIO_DATA3	Data line	I/O	
SDIO_DATA4	Data line	I/O	

A.2.2 Inter Integrated Circuit Interface

The module may provide an Inter Integrated Circuit (I2C) interface to control off-board peripherals such as an accelerometer, camera or touch screen display.

Interface	Description	I/O	Electrical characteristics
I2C_CLK	I2C clock signal		Module defined
I2C_DATA	I2C data interface	I/O	

Note that if I2C is supported, the module will act as master to the peripheral.

A.2.3 Serial Peripheral Interface

The module may provide a Serial Peripheral Interface (SPI), for connecting external display equipment or to control off-board devices such as ZigBee® and Bluetooth®:

Interface	Description	I/O	Electrical characteristics
SPI_CLK	SPI clock signal	O	Module defined
SPI_MOSI	SPI master out slave in	O	
SPI_MISO	SPI master in slave out	I	
SPI_SS	SPI slave select	O	

Note that the module may act as a master or slave to the peripheral.

A.2.4 Controller Area Network Bus

The module may support a Controller Area Network (CAN) Bus interface, which is mostly used for automotive applications: For the electrical characteristics of the CANBUS interface please refer to ISO 11898-1:2003 [13].

Interface	Description	I/O	Electrical characteristics
CAN_RX	CAN Bus receive data	I	
CAN_TX	CAN Bus send data	O	

Annex B (informative): Design guidelines and recommendations

B.1 Recommendations from ETSI ISG SMT on how to use the present document

The reader of the present document will find many well-known interfaces and functionalities targeted to cover the majority of use cases for embedded wireless modules. The reader will also discover that not every pad or function is fully characterized thus leaving room for custom flexibility and future functionalities through the use of unassigned general purpose pads and pads reserved for future use.

When a host device manufacturer elects to build to and order modules according to the present document it is necessary to agree with target module suppliers which aspects of the specification are required, optional or not required for the products being ordered.

Module suppliers may select which interfaces, capabilities, and configuration they intend to supply based on the speculation of market demand. There is no guarantee of interoperability across different modules adherent to the present document. The present document makes no attempt to define the software control interface to the module.

For interfaces that are not fully specified in other fora, some electrical and functional behaviour may be specified in the present document. If it is not specified in other fora or the present document, then the module OEM can define it as is needed.

The present document assumes an LGA footprint is used for mechanical mounting purposes however, this does not explicitly exclude the use of other methods.

B.2 Host PCB Pad Layouts

B.2.0 Host PCB Pad Layouts Introduction

This clause provides possible printed circuit board (PCB) pad layouts for modules defined in the present document. The mechanical drawings for the host PCB footprints are as they would be seen looking downward toward the PCB. The recommended mechanical tolerances for PCB pad placement should allow for a variance of ± 0,02 mm from the dimensions defined. The present document indicates a minimum 0,35 mm overhang from any module outside pad to the outer edge of the module. Host PCB designs are recommended to take into consideration any overhang variance.

B.2.1 SMT3136 Module PCB Pad Layout

Figure B.1 specifies host PCB pads for the SMT3136 module form factor. The form factor provides 146 pads which are numbered 1 through 146.

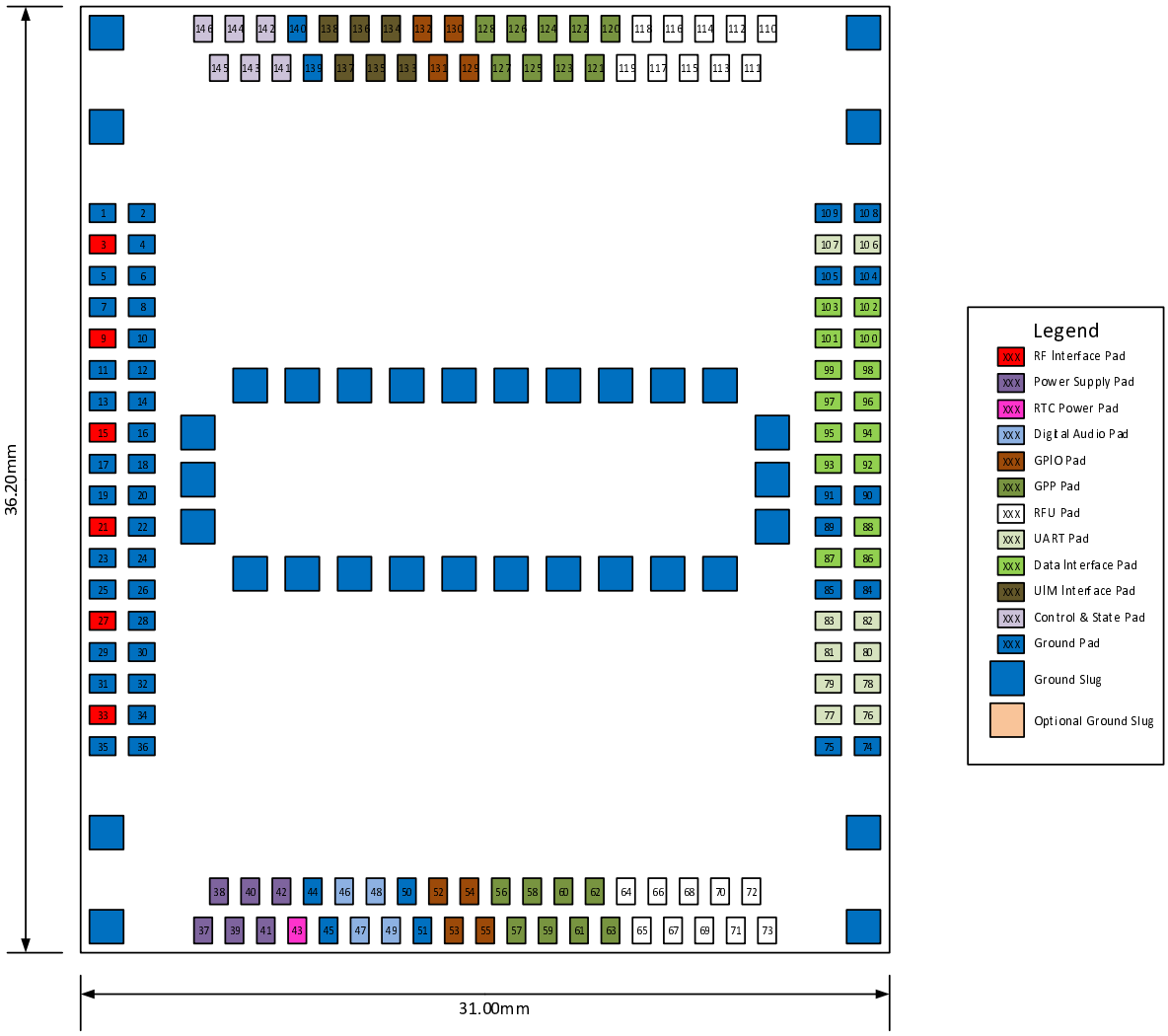

Figure B.1: SMT3136 Module PCB Pad Layout

B.2.2 SMT3129 Module PCB Pad Layout

Figure B.2 specifies host PCB pads for the SMT3129 module form factor. The form factor provides 146 pads which are numbered 1 through 146.

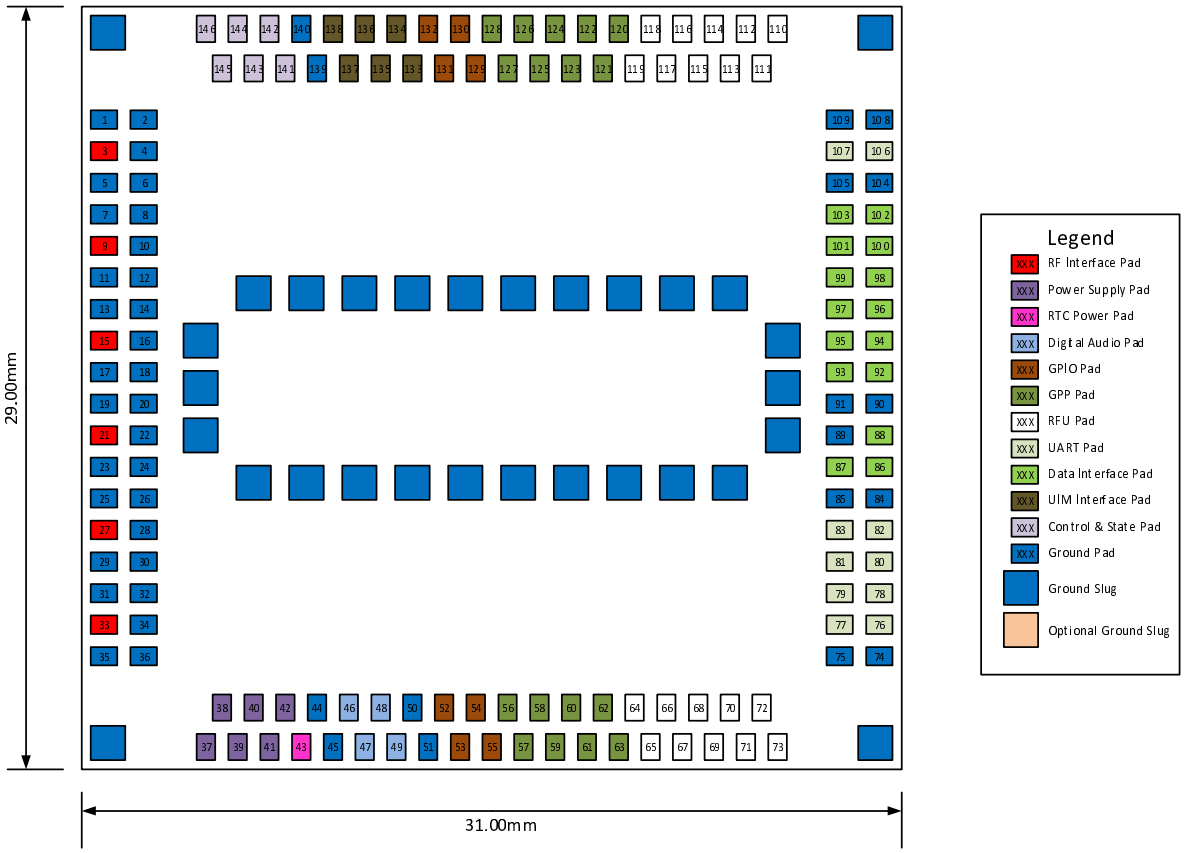

Figure B.2: SMT3129 Module PCB Pad Layout

B.2.3 SMT3122 Module PCB Pad Layout

Figure B.3 specifies host PCB pads for the SMT3122 module form factor. The form factor provides 146 pads which are numbered 1 through 146.

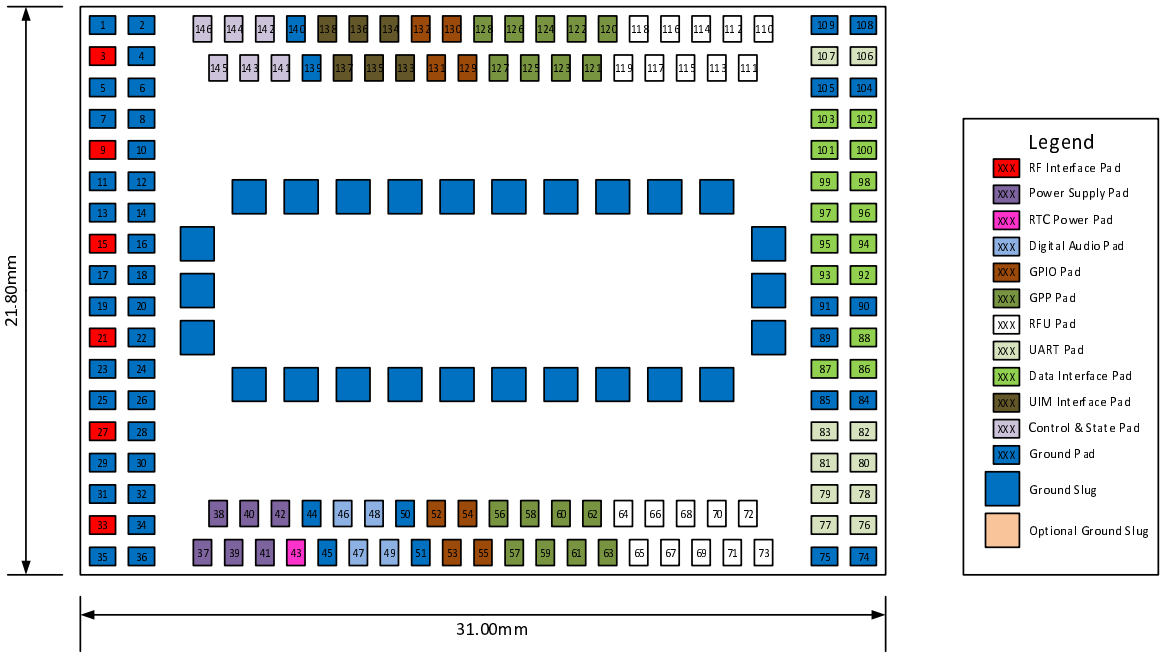

Figure B.3: SMT3122 Module PCB Pad Layout

B.2.4 MT3115 Module PCB Pad Layout

Figure B.4 specifies host PCB pads for the SMT3115 module form factor. The form factor provides 122 pads which are numbered 1 through 73, 80 through 103 and 110 through 146.

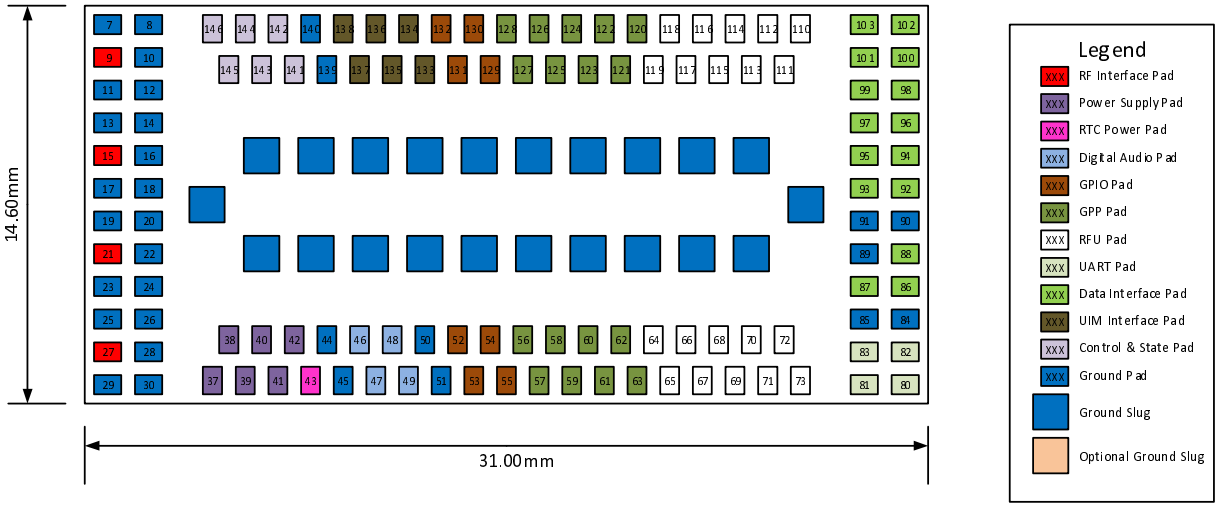

Figure B.4: SMT3115 Module PCB Pad Layout

B.2.5 SMT3729 Module PCB Pad Layout

Figure B.5 specifies host PCB pads for the SMT3729 module form factor. The form factor provides 166 pads which are numbered 1 through 166.

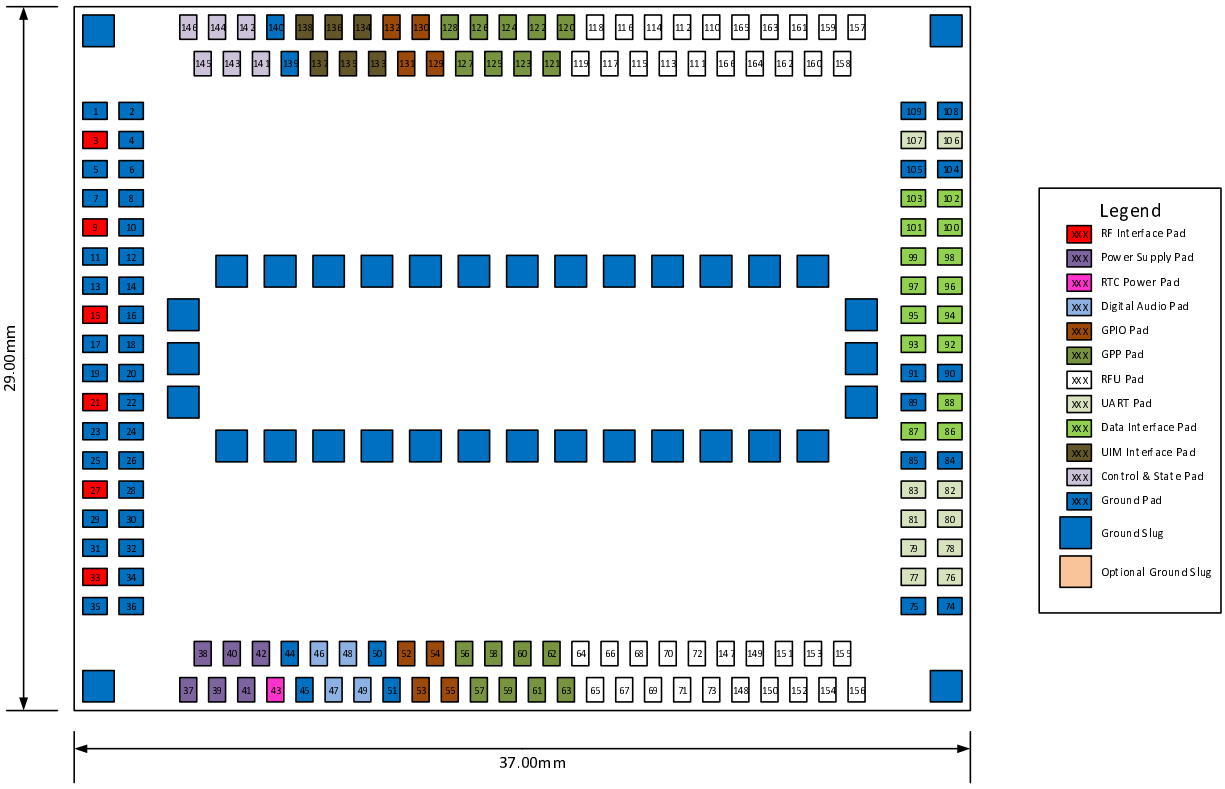

Figure B.5: SMT3729 Module PCB Pad Layout

B.2.6 SMT3722 Module PCB Pad Layout

Figure B.6 specifies host PCB pads for the SMT3722 module form factor. The form factor provides 166 pads which are numbered 1 through 166.

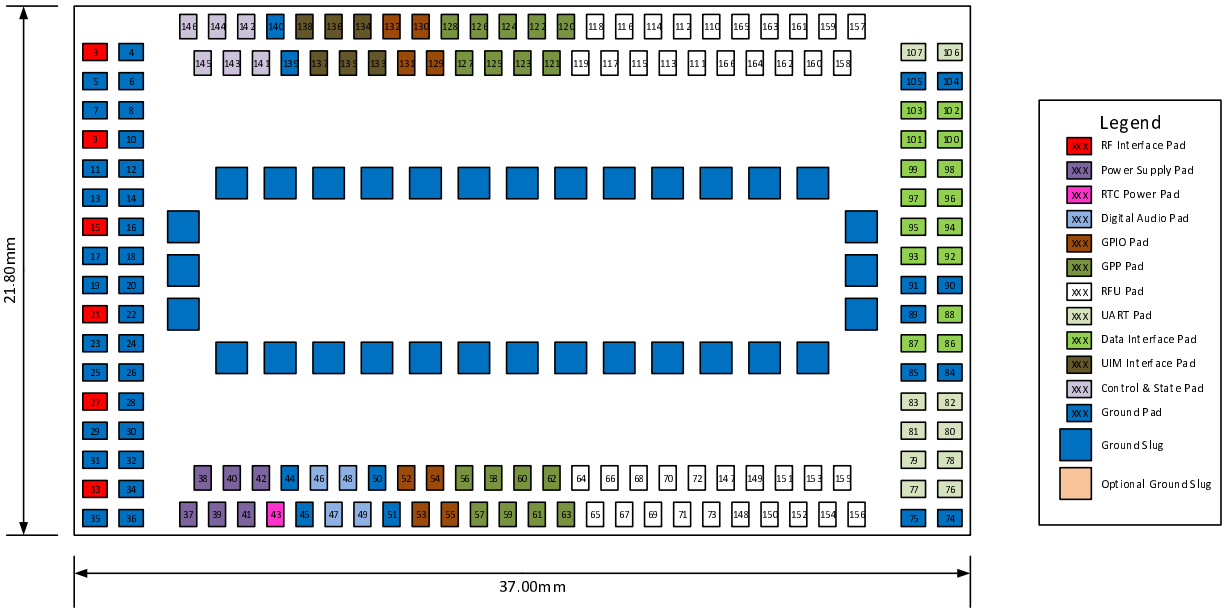

Figure B.6: SMT3722 Module PCB Pad Layout

B.2.7 SMT2522 Module PCB Pad Layout

Figure B.7 specifies host PCB pads for the SMT2522 module form factor. The form factor provides 126 pads which are numbered 1 through 63, 74 through 109, and 120 through 146.

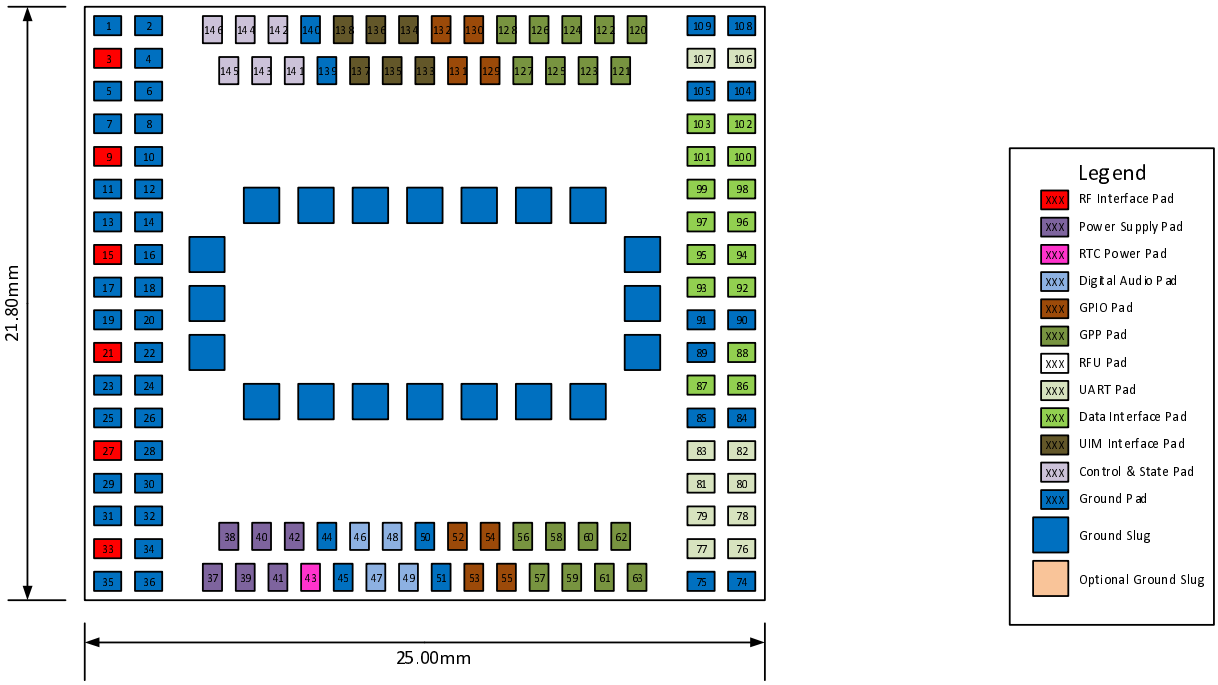

Figure B.7: SMT2522 Module PCB Pad Layout

B.2.8 SMT2515 Module PCB Pad Layout

Figure B.8 specifies host PCB pads for the SMT2515 module form factor. The form factor provides 102 pads which are numbered 7 through 30, 37 through 63, 80 through 103, and 120 through 146.

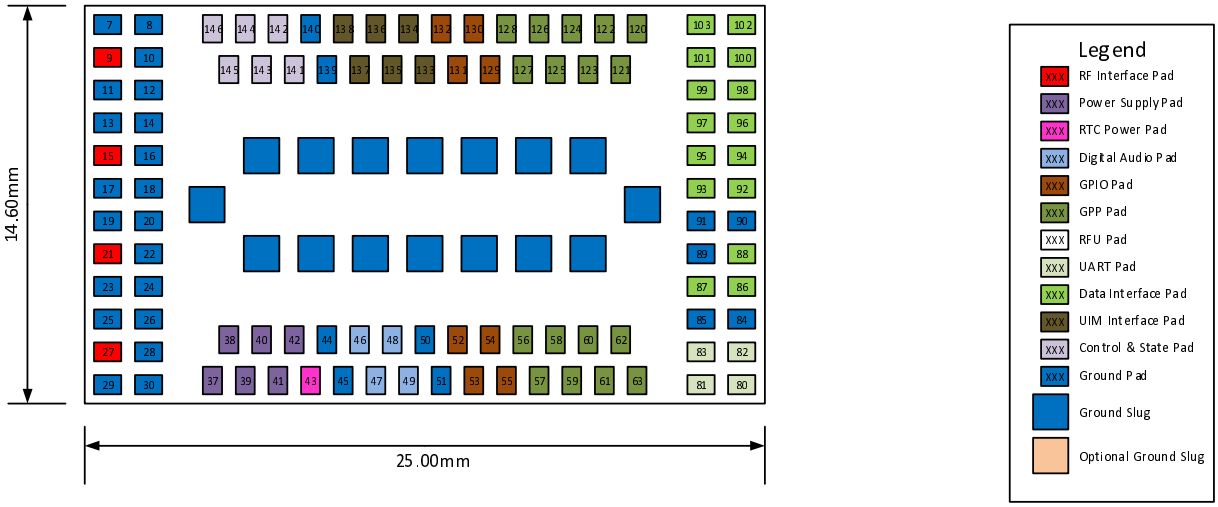

Figure B.8: SMT2515 Module PCB Pad Layout

B.2.9 SMT1922 Module PCB Pad Layout

Figure B.9 specifies host PCB pads for the SMT1922 module form factor. The form factor provides 106 pads which are numbered 1 through 53, 74 through 109, and 130 through 146.

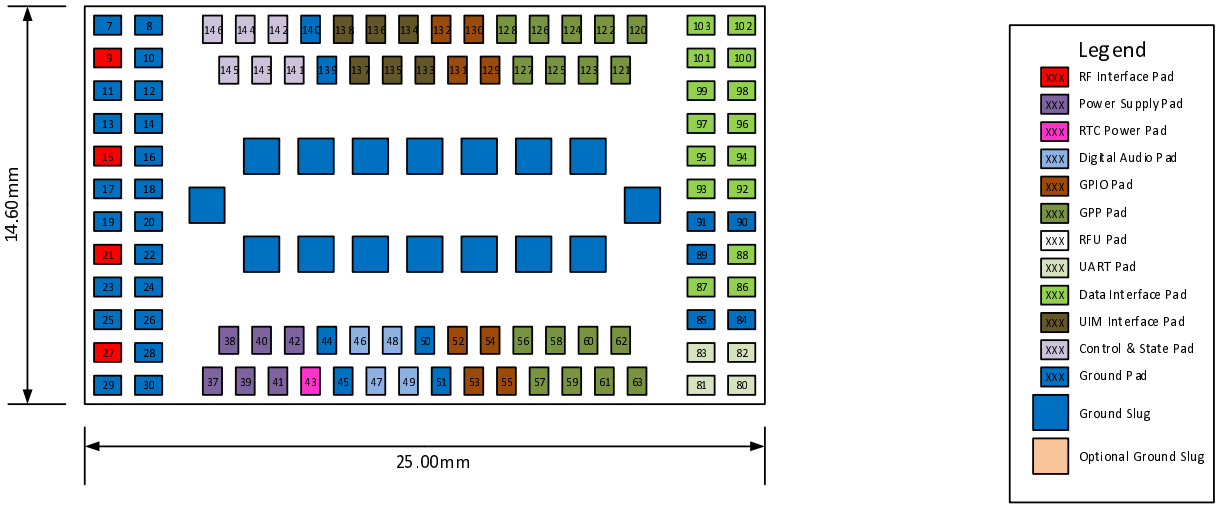

Figure B.9: SMT1922 Module PCB Pad Layout

B.2.10 SMT1915 Module PCB Pad Layout

Figure B.10 specifies host PCB pads for the SMT1915 module form factor. The form factor provides 82 pads which are numbered 7 through 30, 37 through 53, 80 through 103, and 130 through 146.

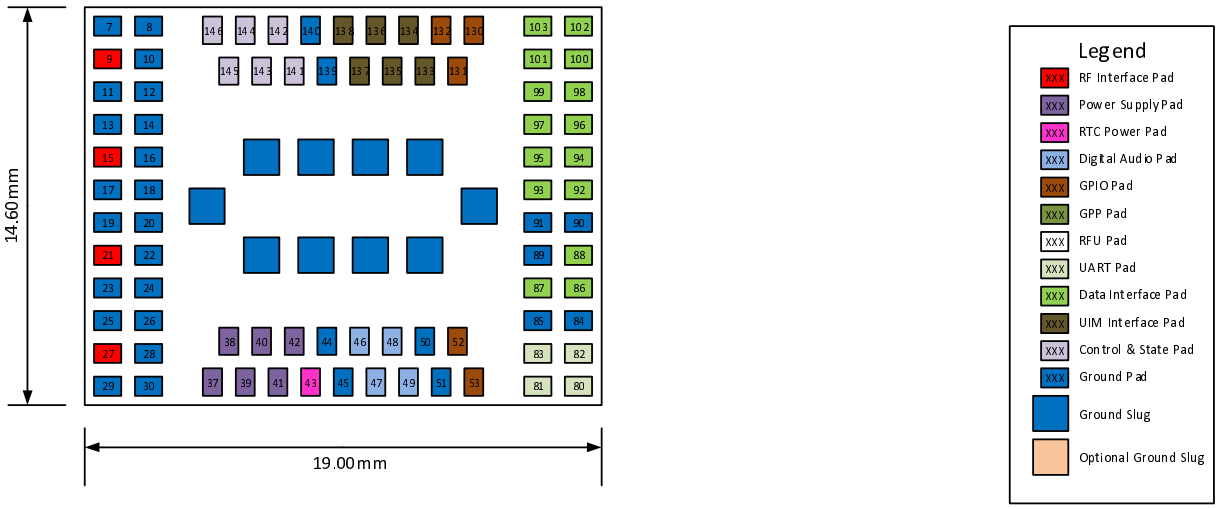

Figure B.10: SMT1915 Module PCB Pad Layout

B.2.11 SMT3136, SMT3129, and SMT3122 Common PCB Pad Layout

Figure B.11 specifies host PCB pads for a board which can accommodate the SMT3136, SMT3129 and SMT3122 module form factors on a common PCB.

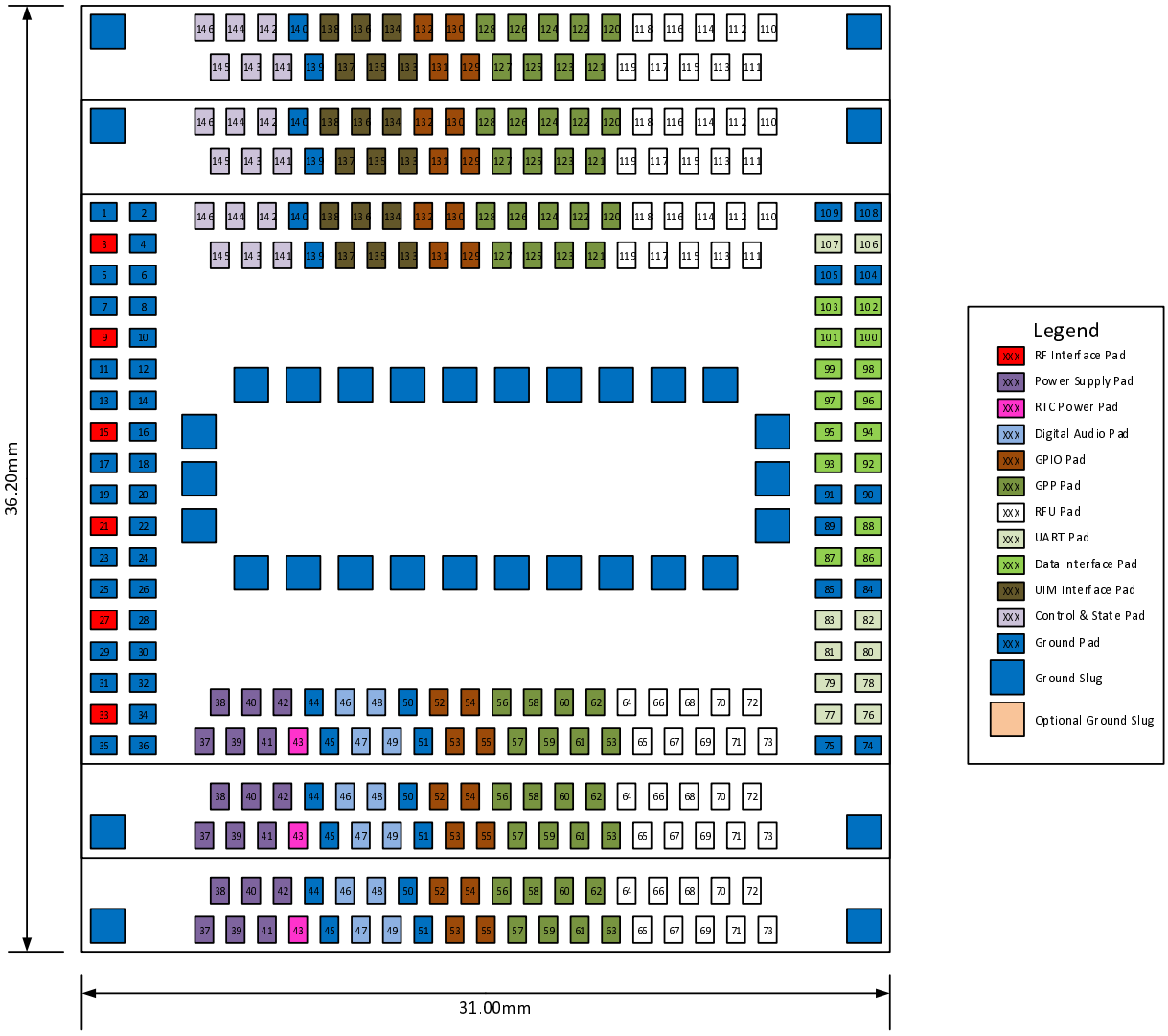

Figure B.11: SMT3136, SMT3129 and SMT3122 Common PCB Pad Layout

B.2.12 SMT3729 and SMT3722 Common PCB Pad Layout

Figure B.12 specifies host PCB pads for a board which can accommodate the SMT3729 and SMT3722 module form factors on a common PCB.

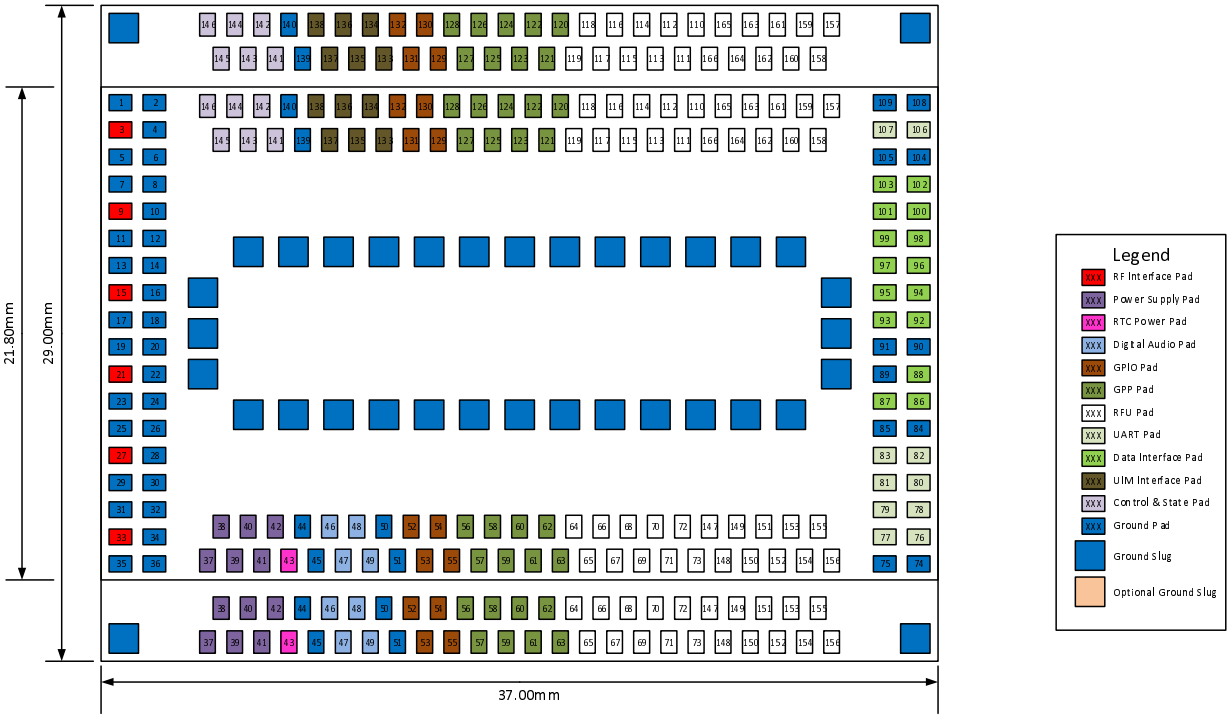

Figure B.12: SMT3729 and SMT3722 Common PCB Pad Layout

B.2.13 SMT2522 and SMT2515 Common PCB Pad Layout

Figure B.13 specifies host PCB pads for a board which can accommodate the SMT2522 and SMT2515 module form factors on a common PCB.

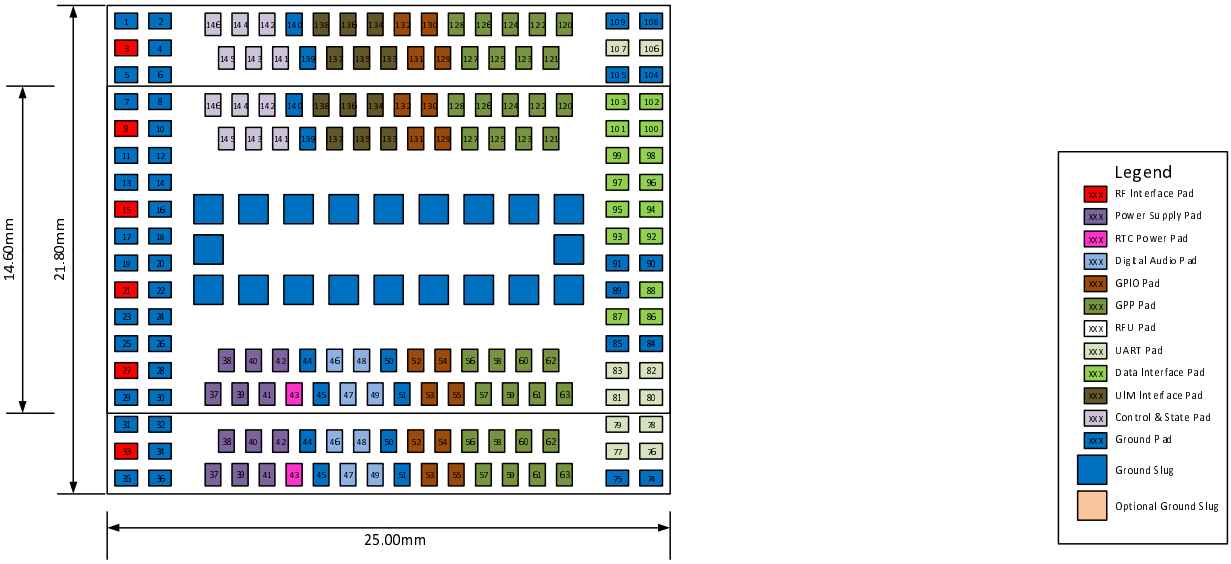

Figure B.13: SMT2522 and SMT2515 Common PCB Pad Layout

B.2.14 Minimal SMT1915 and SMT2515 Common PCB Pad Layout

Figure B.14 specifies host PCB pads for a board which can accommodate the Minimal SMT1915 and SMT2515 module form factors on a common PCB.

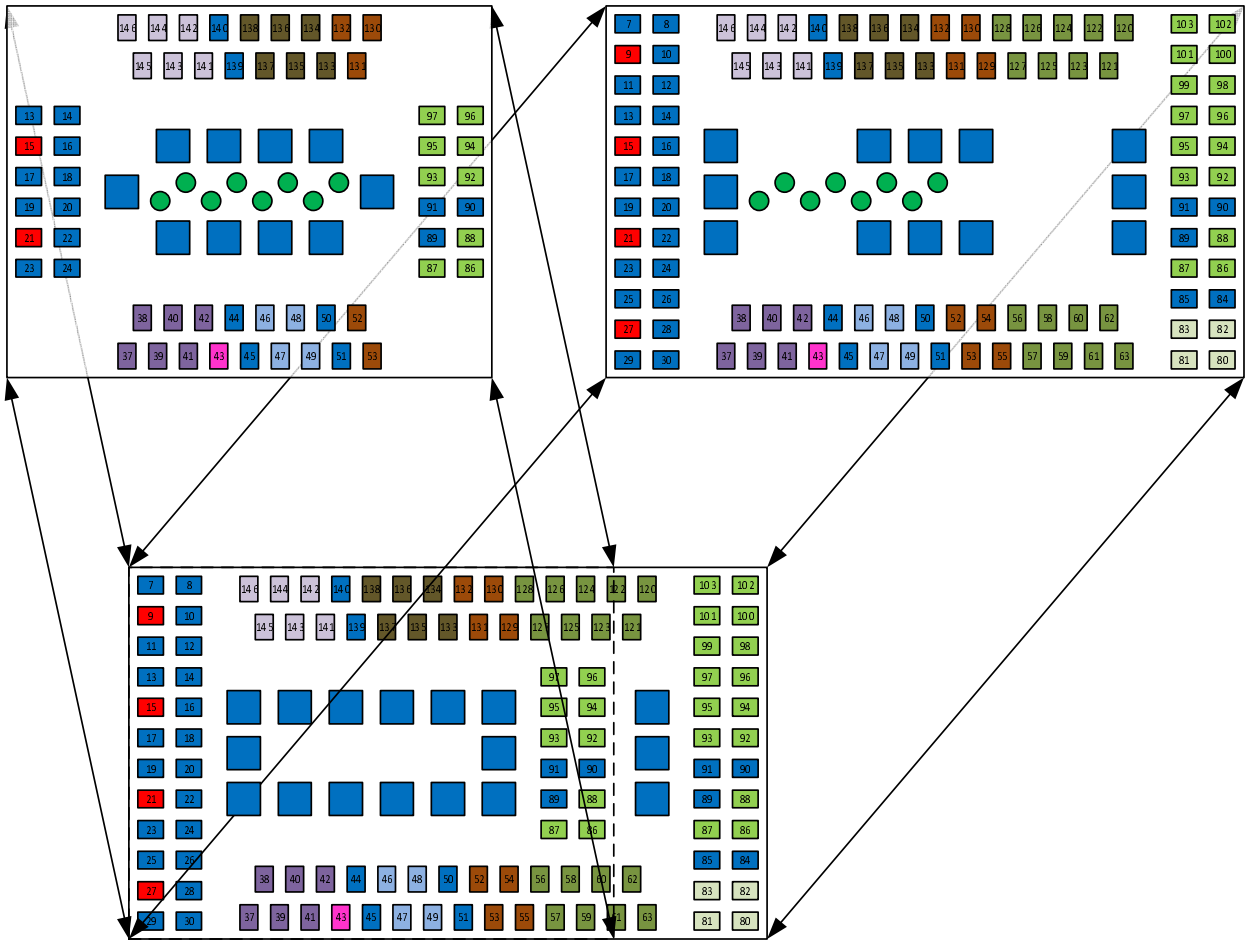

Figure B.14: Minimal SMT1915 and SMT2515 Common PCB Pad Layout

B.2.15 Minimal SMT1915, Minimal SMT2515, and SMT3115 Common PCB Pad Layout

Figure B.15 specifies host PCB pads for a board which can accommodate the Minimal SMT1915, Minimal SMT2515, and SMT3115 module form factors on a common PCB.

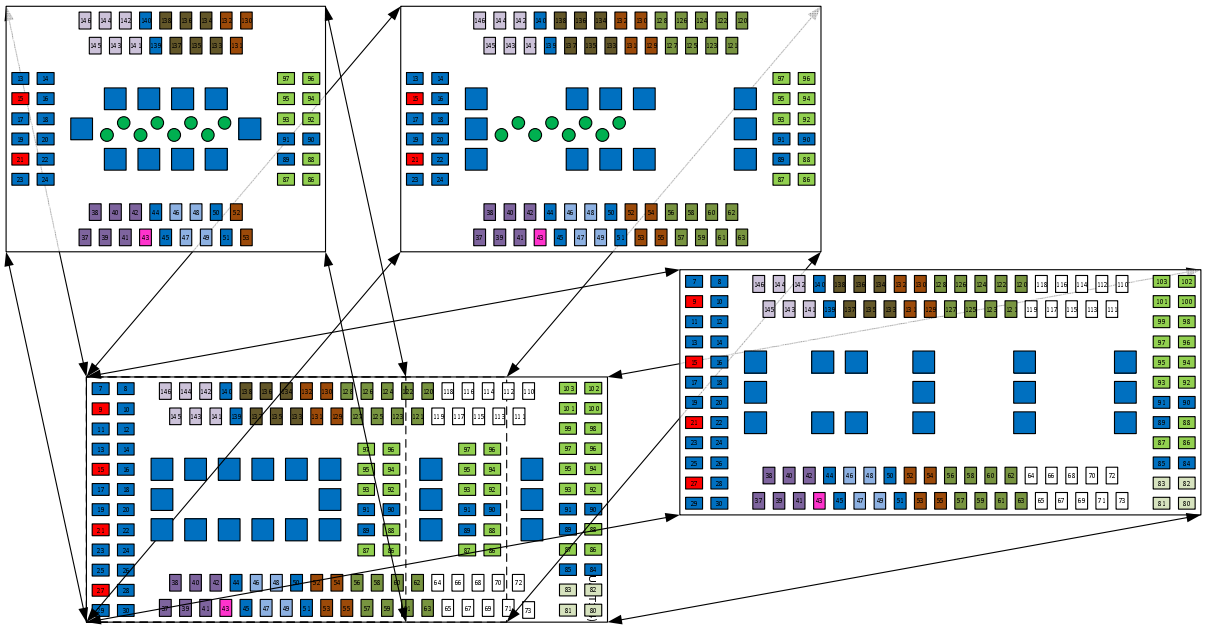

Figure B.15: Minimal SMT1915, Minimal SMT2515 and SMT3115 Common PCB Pad Layout

B.3 Reserved for Future Use (RFU) Pads on Host PCB

It is expected that the Reserved for Future Use pads should be physically connected for mechanical stability, but not electrically connected to anything on the host PCB. These pads are reserved for definition in future revisions of the present document. Non-standard use of these pads may result in incompatibilities in solutions aligned with the future revisions.

B.4 Advanced Indicator Protocols for WWAN_STATE

More advanced indicator protocols are allowed. Advanced features might include use of blinking or intermittent ON states which can be used to indicate radio operations such as scanning, associating, or data transfer activity. The implementation of blinking states may also be useful in reducing LED power consumption.

An example of a more advanced protocol:

Signal Off	Module off
Signal Fast blinking	network searching, not registered, turning off
Signal Slow blinking	Registered full service, In call
Signal On	No defined states

B.5 Recommendations for RESET Implementation

The minimum timing to hold the RESET pad low for a hardware reset is recommended at 50 ms with a typical time of 100 ms.

In good design it is recommended that the host provides a high impedance (~100 k Ohm) external pull-up resistor connected to the high digital reference voltage to avoid an accidental low state on the pad.

Annex C (informative): Bibliography

GSM Association: "Embedded Mobile Surface Mount Technology, Technical Requirements" Version 1.0 September 29th, 2011.

History

Document history		
V1.1.1	October 2014	Publication
V2.1.1	June 2015	Publication